STRUCTURE	Silicon Monolithic Integrated Circuit
TYPE	Regulator IC for Memory termination
PRODUCT SERIES	**BD3533HFN**
FEATURES	・Incorporates a push-pull power supply for termination (VTT)
	・Incorporates a reference voltage circuit(VREF)
	・Compatible with Dual Channel (DDR-Ⅱ)

○ ABSOLUTE MAXIMUM RATINGS (Ta=100℃)

Parameter	Symbol	Limit	Unit
Input Voltage	VCC	7 *1*2	V
Enable Input Voltage	VEN	7 *1*2	V
Termination Input Voltage	VTT_IN	7 *1*2	V
VDDQ Reference Voltage	VDDQ	7 *1*2	V
Output Current	ITT	1	A
Power Dissipation1	Pd1	630 *3	mW
Power Dissipation2	Pd2	1350 *4	mW
Power Dissipation3	Pd3	1750 *5	mW
Operating Temperature Range	Topr	-30～+100	℃
Storage Temperature Range	Tstg	-55～+150	℃
Maximum Junction Temperature	Tjmax	+150	℃

*1 Should not exceed Pd.
*2 Instantaneous surge voltage, back electromotive force and voltage under less than 10% duty cycle.
*3 With Ta≧25℃ when mounting a 70mm × 70mm × 1.6mm glass-epoxy substrate 1-layer board (copper foil density 0.2%) θja=198.4℃/W
*4 With Ta≧25℃ when mounting a 70mm × 70mm × 1.6mm glass-epoxy substrate 1-layer board (copper foil density 7%) θja=92.4℃/W
*5 With Ta≧25℃ when mounting a 70mm × 70mm × 1.6mm glass-epoxy substrate 1-layer board (copper foil density 65%) θja=71.4℃/W

○ RECOMMENDED OPERATING CONDITIONS (Ta=25℃)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Input Voltage	VCC	2.7	5.5	V
Termination Input Voltage	VTT_IN	1.0	5.5	V
VDDQ Reference Voltage	VDDQ	1.0	2.75	V
Enable Input Voltage	VEN	-0.3	5.5	V

★ No radiation-resistant design is adopted for the present product.

The Japanese version of this document is the official specification.
This translated version is intended only as a reference, to aid in understanding the official version.
If there are any differences between the original and translated versions of this document, the official Japanese language version takes priority.

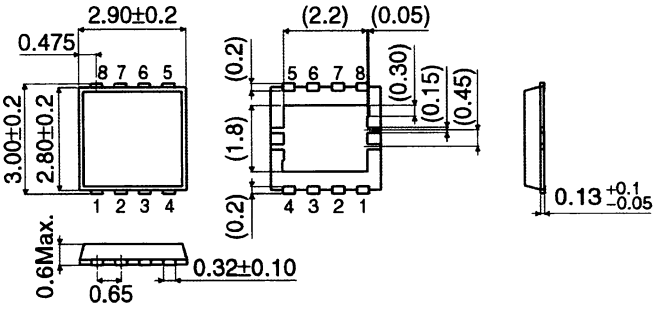
○ ELECTRICAL CHARACTERISTICS

(Unless otherwise specified,Ta=25℃ VCC=3.3V VEN=3V VDDQ=1.8V VTT_IN=1.8V)

PARAMETER	SYMBOL	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
Standby Current	IST	-	0.5	1.0	mA	VEN=0V
Bias Current	ICC	-	2	4	mA	VEN=3V
[Enable]						
High Level Enable Input Voltage	VENHIGH	2.3	-	5.5	V	
Low Level Enable Input Voltage	VENLOW	-0.3	-	0.8	V	
Enable Pin Input Current	IEN	-	7	10	uA	VEN=3V
[Termination]						
Termination Output Voltage 1	VTT1	VREF-30m	VREF	VREF+30m	V	ITT=-1.0A to 1.0A Ta=0℃ to 100℃ *5
Termination Output Voltage 2	VTT2	VREF-30m	VREF	VREF+30m	V	VCC=5V, VDDQ=2.5V VTT_IN=2.5V ITT=-1.0A to 1.0A Ta=0℃ to 100℃ *5
Source Current	ITT+	1.0	-	-	A	
Sink Current	ITT-	-	-	-1.0	A	
Load Regulation	⊿VTT	-	-	50	mV	ITT=-1.0A to 1.0A
Line Regulation	Reg.I	-	20	40	mV	
Upper Side ON Resistance 1	HRON1	-	0.45	0.9	Ω	
Lower Side ON Resistance 1	LRON1	-	0.45	0.9	Ω	
Upper Side ON Resistance 2	HRON2	-	0.4	0.8	Ω	Vcc=5V, VDDQ=2.5V VTT_IN=2.5V
Lower Side ON Resistance 2	LRON2	-	0.4	0.8	Ω	Vcc=5V, VDDQ=2.5V VTT_IN=2.5V
[Input of Reference Voltage]						
Input Impedance	ZVDDQ	70	100	130	kΩ	
[Reference voltage]						
Output Voltage 1	VREF1	1/2×VDDQ -30m	1/2×VDDQ	1/2×VDDQ +30m	V	IREF=0mA
Output Voltage 2	VREF2	1/2×VDDQ -40m	1/2×VDDQ	1/2×VDDQ +40m	V	IREF=-10mA to 10mA Ta=0℃ to 100℃ *5
Output Voltage 3	VREF3	1/2×VDDQ -30m	1/2×VDDQ	1/2×VDDQ +30m	V	VCC=5V, VDDQ=2.5V VTT_IN=2.5V, IREF=0mA
Output Voltage 4	VREF4	1/2×VDDQ -40m	1/2×VDDQ	1/2×VDDQ +40m	V	VCC=5V, VDDQ=2.5V VTT_IN=2.5V ITT=-10mA to 10mA Ta=0℃ to 100℃ *5
Source Current	IREF+	20	-	-	mA	
Sink Current	IREF-	-	-	-20	mA	
[UVLO]						
UVLO OFF Voltage	VUVLO	2.40	2.55	2.70	V	VCC : sweep up
Hysteresis Voltage	⊿VUVLO	100	160	220	mV	VCC : sweep down

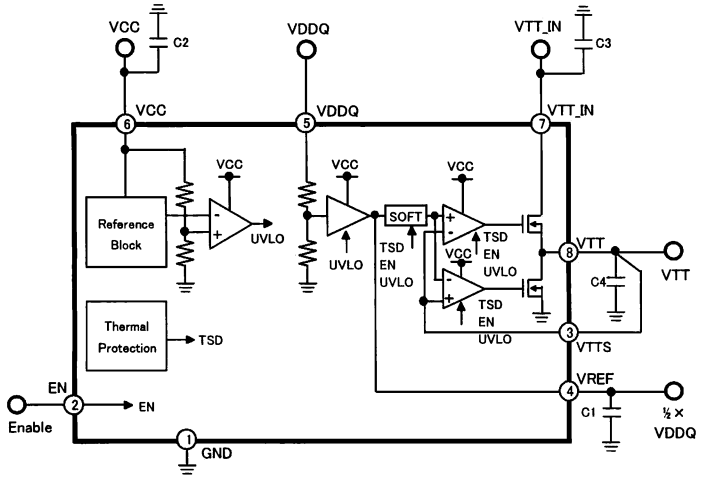
*6 Design Guarantee

O PHYSICAL DIMENSIONS



HSON8 (単位:mm)

O BLOCK DIAGRAM



O Pin number Pin name

Pin No.	Pin Name
1	GND
2	EN
3	VTTS
4	VREF
5	VDDQ
6	VCC
7	VTT_IN
8	VTT
FIN	—

ONOTES FOR USE

(1) Absolute maximum range
Although the quality of this product is rigorously controlled, and circuit operation is guaranteed within the operation ambient temperature range, the device may be destroyed when applied voltage or operating temperature exceeds its absolute maximum rating. Because the failure mode (such as short mode or open mode) cannot be identified in this instance, it is important to take physical safety measures such as fusing if a specific mode in excess of absolute rating limits is considered for implementation.

(2) Ground potential
Make sure the potential for the GND pin is always kept lower than the potentials of all other pins, regardless of the operating mode, including transient conditions.

(3) Thermal Design
Provide sufficient margin in the thermal design to account for the allowable power dissipation (Pd) expected in actual use.

(4) Using in the strong electromagnetic field
Use in strong electromagnetic fields may cause malfunctions.

(5) ASO
Be sure that the output transistor for this IC does not exceed the absolute maximum ratings or ASO value.

(6) Thermal shutdown circuit
The IC is provided with a built-in thermal shutdown (TSD) circuit. When chip temperature reaches the threshold temperature shown below, output goes to a cut-off (open) state. Note that the TSD circuit is designed exclusively to shut down the IC in abnormal thermal conditions. It is not intended to protect the IC per se or guarantee performance when extreme heat occurs. Therefore, the TSD circuit should not be employed with the expectation of continued use or subsequent operation once TSD is operated.

TSD ON temperature [℃] (typ.)	Hysteresis temperature [℃] (typ.)
175	15

(7) GND pattern
When both a small-signal GND and high current GND are present, single-point grounding (at the set standard point) is recommended, in order to separate the small-signal and high current patterns, and to be sure the voltage change stemming from the wiring resistance and high current does not cause any voltage change in the small-signal GND. In the same way, care must be taken to avoid wiring pattern fluctuations in any connected external component GND.

(8) Output Capacitor (C1)
Mount an output capacitor between VREF and GND for stability purposes. The VREF output capacitor is for the open loop gain phase compensation. If the capacitor value is not large enough, the output voltage may oscillate. A ceramic 1.0 - 10uF capacitor with minimal susceptibility to temperature is recommended. However, this stability depends on the characteristics of temperature and load. Please confirm operation across a variety of temperature and load conditions.

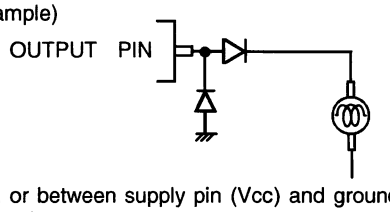
(9) Output Capacitor (C4)
Mount an output capacitor between VTT and GND for stability purposes. The output capacitor is for the open loop gain phase compensation and reduces the output voltage load regulation. If the capacitor value is not large enough, the output voltage may oscillate. And if the equivalent series resistance (ESR) is too large, the output voltage rise/drop increases during a sudden load change. A 47 - 220uF polymer capacitor is recommended. However, the stability depends on the characteristics of temperature and load conditions. And if a small ESR capacitor such as a ceramic capacitor is utilized, the output voltage may oscillate due to lack of phase margin. In this case, measures can be taken by adding a resistor in series with this capacitor. Please confirm operation across a variety of temperature and load conditions.

(10) Input Capacitor (C2, C3)
The input capacitor reduces the output impedence of the voltage supply source connected in the VCC and VTT_IN. If the output impedence of this power supply increases, the input voltage (VCC,VTT_IN) may become unstable. This may result in the output voltage oscillation or lowering ripple rejection. A low ESR 1uF capacitor in VCC and 10uF capacitor in VTT_IN with minimal susceptibility to temperature are preferable, but stability depends on power supply characteristics and the substrate wiring pattern (a parasitic capacitance and impedance). Please confirm operation across a variety of temperature and load conditions.

(11) Input (VCC, VDDQ, VTT_IN, EN)
The VCC, VDDQ, VTT_IN, and EN are isolated. The UVLO function is integrated to protect faulty operation due to low voltage levels of VCC. VTT output voltage starts up when VCC reaches the UVLO threshold level and EN reaches the threshold level respectively regardless of the start up order in those inputs. And also VREF output voltage starts up when VCC reaches the UVLO threshold level. When the VDDQ and VTT_IN has the same voltage and are supposed to connect each other, VDDQ pin voltage may change due to the voltage drop on the VTT_IN and VDDQ common wiring caused by VTT_IN input current change. This may result in the voltage change of the VTT output. Avoid drawing wiring pattern of VDDQ and VTT_IN so that they do not have common wiring. If the common wiring is inevitable due to limited PCB area, it is recommended that CR filter be added between VTT_IN and VDDQ.

(12) VTTS
VTTS is to improve load regulation of VTT output. For precise load regulation, VTTS is connected close by VTT to avoid common impedance.

(Example)



(13) Heat sink (FIN)
Since the heat sink (FIN) is connected with the Sub, short it to the GND.
It is possible to minimize the thermal resistance by soldering it to GND plane of PCB.

(14) Short-circuits between pins and and mounting errors
Do not short-circuit between output pin (Vo) and supply pin (Vcc) or ground (GND), or between supply pin (Vcc) and ground (GND). Mounting errors, such as incorrect positioning or orientation, may destroy the device.

(15) Please add a protection diode when a large inductance component is connected to the output terminal, and reverse-polarity power is possible at startup or in output OFF condition

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