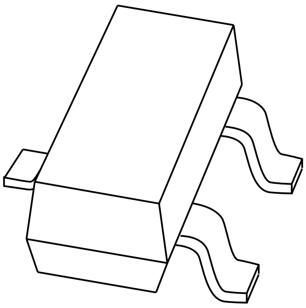
DATA SHEET



BSH102
N-channel enhancement mode MOS transistor

Product specification
Supersedes data of 1997 Jun 19
File under Discrete Semiconductors, SC13b

1997 Dec 08

Philips Semiconductors

PHILIPS

N-channel enhancement mode MOS transistor | BSH102

FEATURES

- Very low threshold
- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL etc.

APPLICATIONS

- Power management
- DC to DC converters
- Battery powered applications
- ‘Glue-logic’; interface between logic blocks and/or periphery
- General purpose switch.

DESCRIPTION

N-channel enhancement mode MOS transistor in a SOT23 SMD package.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

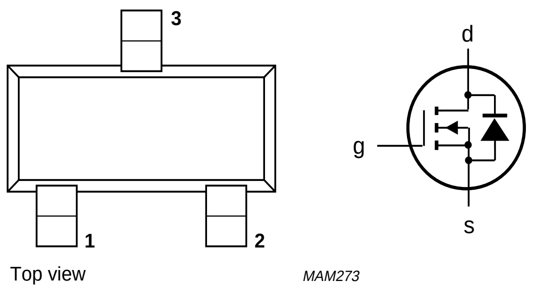


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.5 A	–	1	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	–	V
I_D	drain current (DC)	T_s = 80 °C	–	0.85	A
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 0.5 A	–	0.4	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	0.85	A
I_{DM}	peak drain current	note 2	–	3.4	A
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W
		T_{amb} = 25 °C; note 3	–	0.75	W
		T_{amb} = 25 °C; note 4	–	0.54	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	0.5	A
I_{SM}	peak pulsed source current	note 2	–	2	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

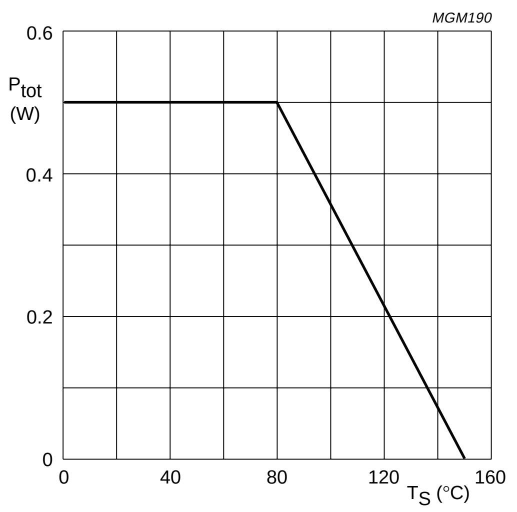
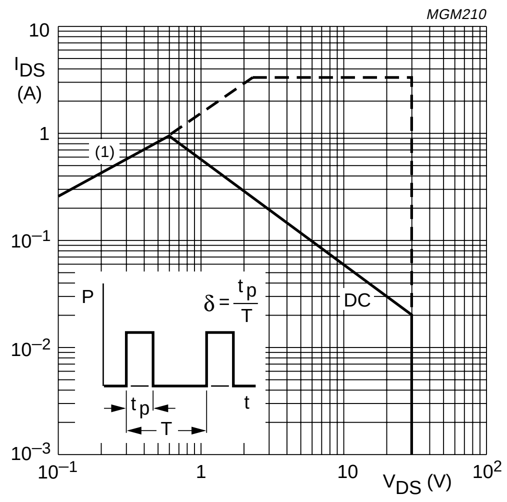


Fig.2 Power derating curve.



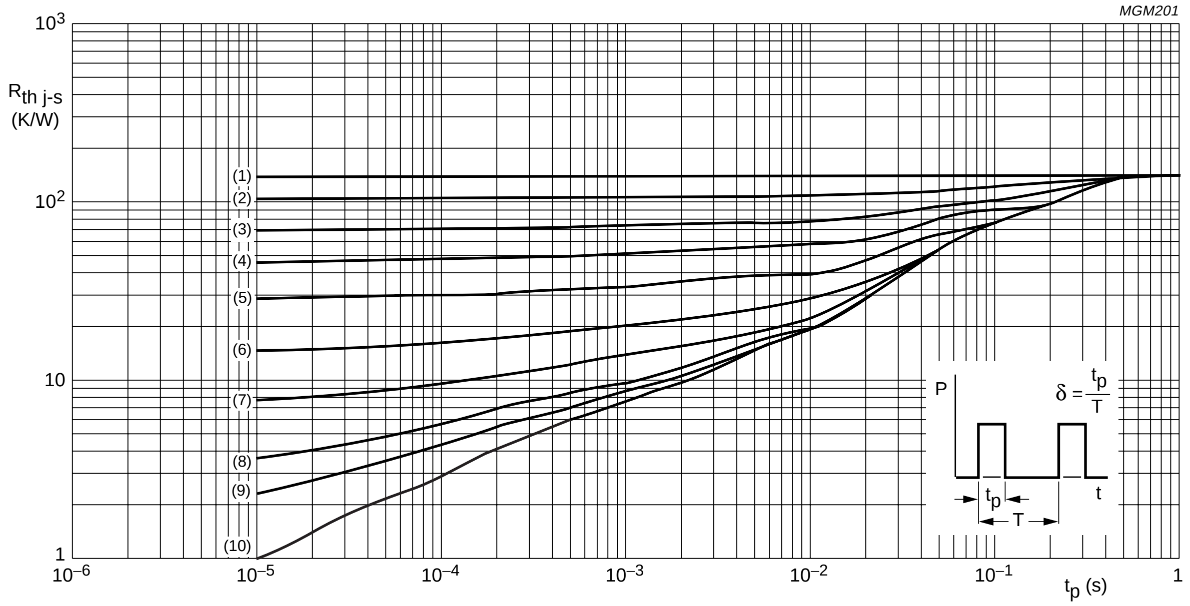
δ = 0.01; T_s = 80 °C.

(1) R_{DSon} limitation.

Fig.3 SOAR.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	140	K/W



(1) $\delta = 1$. (2) $\delta = 0.75$. (3) $\delta = 0.5$. (4) $\delta = 0.33$. (5) $\delta = 0.2$.
(6) $\delta = 0.1$. (7) $\delta = 0.05$. (8) $\delta = 0.02$. (9) $\delta = 0.01$. (10) $\delta = 0$.

Fig.4 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 µA	30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	1	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 0.5 A	–	–	0.4	Ω
		V_{GS} = 4.5 V; I_D = 0.25 A	–	–	0.6	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	67	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	27	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	13	–	pF
Q_G	total gate charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 0.5 A; T_{amb} = 25 °C	–	2290	–	pC
Q_{GS}	gate-source charge	V_{DD} = 15 V; I_D = 0.5 A; T_{amb} = 25 °C	–	150	–	pC
Q_{GD}	gate-drain charge	V_{DD} = 15 V; I_D = 0.5 A; T_{amb} = 25 °C	–	780	–	pC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	3.5	–	ns
t_f	fall time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	4	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	7.5	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	8	–	ns
t_r	rise time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	3	–	ns
t_{off}	turn-off switching time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	11	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.5 A	–	–	1	V
t_{rr}	reverse recovery time	I_S = 0.5 A; di/dt = –100 A/µs	–	25	–	ns

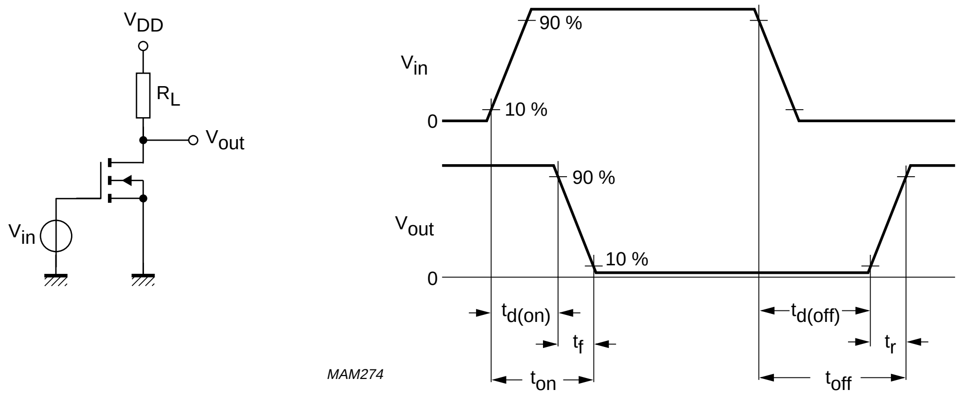
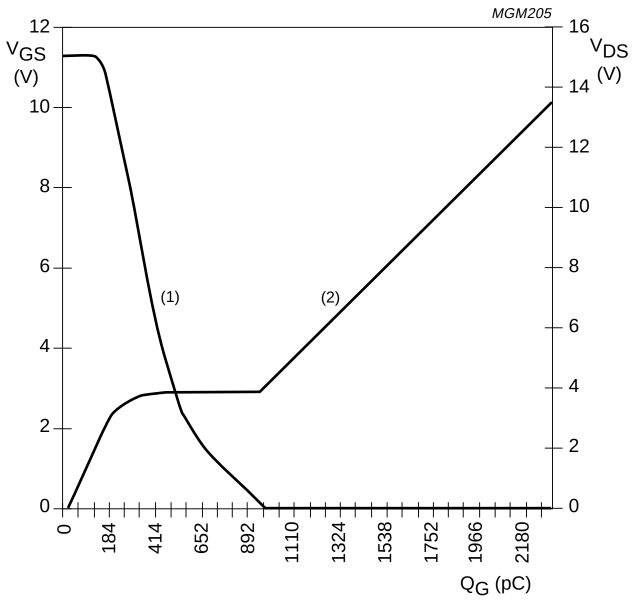


Fig.5 Switching times test circuit with input and output waveforms.

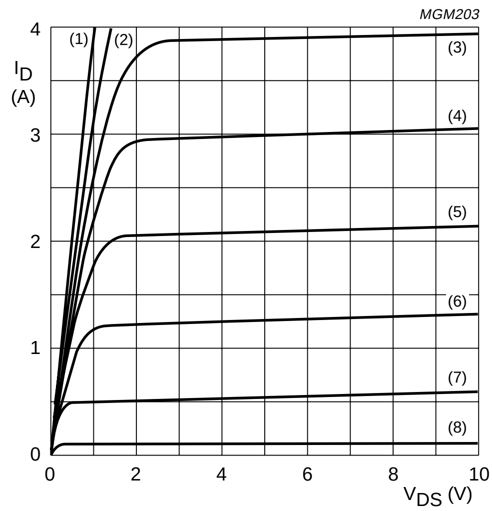


V_{DD} = 15 V; I_D = 0.5 A; T_{amb} = 25 °C.

(1) V_{DS}.

(2) V_{GS}.

Fig.6 Gate-source and drain-source voltages as functions of total gate charge; typical values.



T_{amb} = 25 °C; t_p = 300 µs; δ = 0.

(1) V_{GS} = 10 V.

(2) V_{GS} = 6 V.

(3) V_{GS} = 5 V.

(4) V_{GS} = 4.5 V.

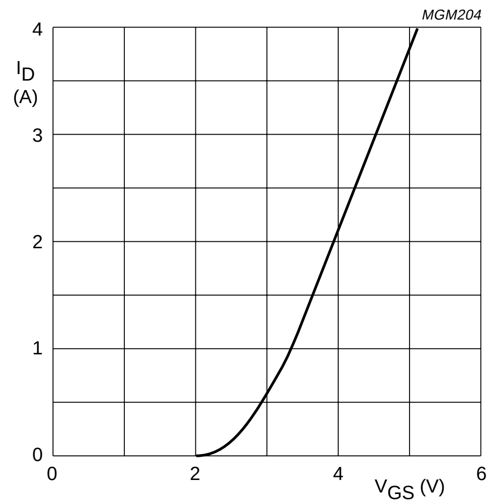
(5) V_{GS} = 4 V.

(6) V_{GS} = 3.5 V.

(7) V_{GS} = 3 V.

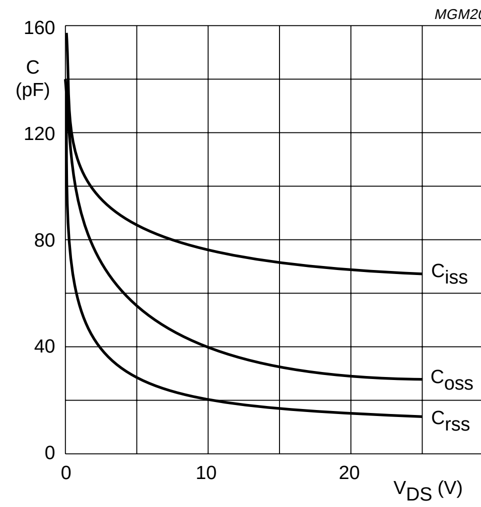
(8) V_{GS} = 2.5 V.

Fig.7 Output characteristics; typical values.



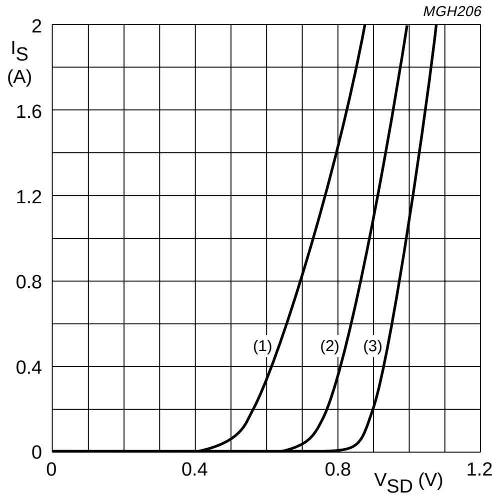
V_{DS} = 10 V; T_{amb} = 25 °C; t_p = 300 μs; δ = 0.

Fig.8 Transfer characteristic; typical values.



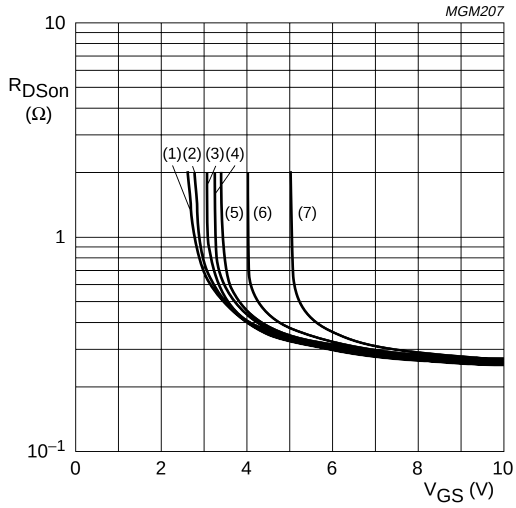
V_{GS} = 0 ; f = 1 MHz; T_{amb} = 25 °C.

Fig.9 Capacitance as a function of drain-source voltage; typical values.



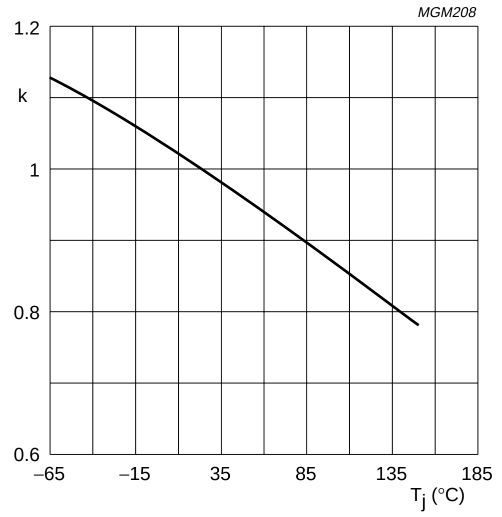
V_{GD} = 0.
(1) T_{amb} = 150 °C.
(2) T_{amb} = 25 °C.
(3) T_{amb} = −65 °C.

Fig.10 Source current as a function of source-drain diode forward voltage; typical values.



T_{amb} = 25 °C; t_p = 300 μs; δ = 0.
(1) I_D = 0.1 A.
(2) I_D = 0.25 A.
(3) I_D = 0.5 A.
(4) I_D = 0.75 A.
(5) I_D = 1 A.
(6) I_D = 2 A.
(7) I_D = 4 A.

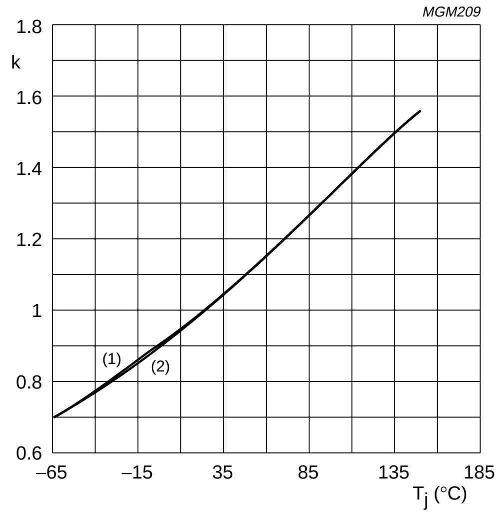
Fig.11 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25\,°C}$$

V_{GSth} at $V_{DS} = V_{GS}$; $I_D = 1$ mA.

Fig.12 Temperature coefficient of gate-source threshold voltage as a function of junction temperature; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\,°C}$$

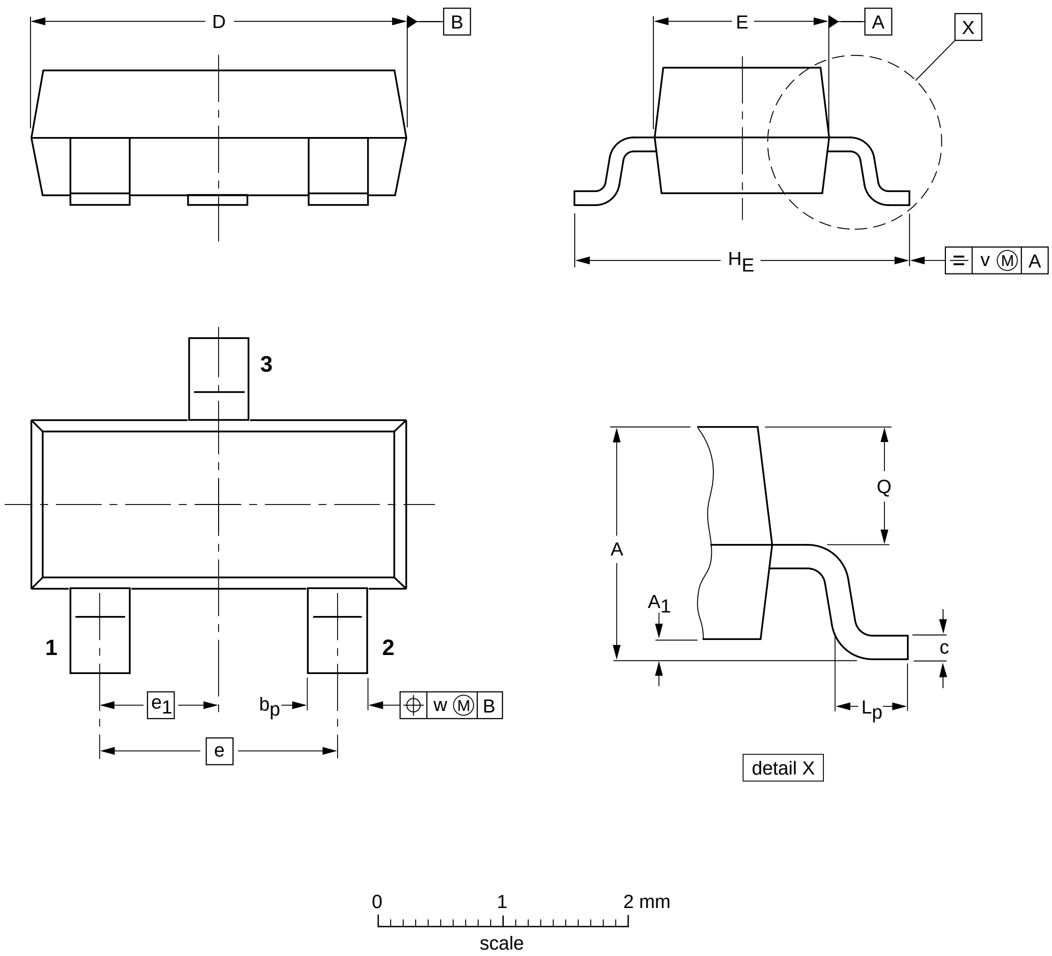
(1) R_{DSon} at $V_{GS} = 10$ V; $I_D = 0.5$ mA.

(2) R_{DSon} at $V_{GS} = 4.5$ V; $I_D = 0.25$ mA.

Fig.13 Temperature coefficient of drain-source on-resistance as a function of junction temperature; typical values.

PACKAGE OUTLINE

Plastic surface mounted package; 3 leads **SOT23**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max.	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT23						97-02-28

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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