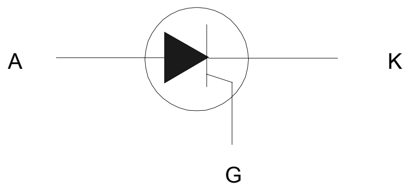
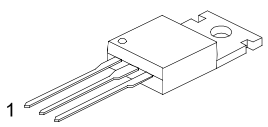
UTC BT150

SCRs

DESCRIPTION
Passivated thyristors in a plastic envelope, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

SYMBOL





TO-220

1: CATHODE 2: ANODE 3: GATE

ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	RATING	UNIT
Repetitive peak off-state voltages BT150-500 BT150-650 BT150-800	V_{DRM} , V_{RRM}	500* 650* 800	V
Average on-state current (half sine wave; T_{mb} ≤113 °C)	$I_{T(AV)}$	2.5	A
RMS on-state current (all conduction angles)	$I_{T(RMS)}$	4	A
Non-repetitive peak on-state current (half sine wave; T_j = 25 °C prior to surge) t = 10 ms t = 8.3 ms	I_{TSM}	35 38	A
I^2t for fusing (t = 10 ms)	I^2t	6.1	A^2s
Repetitive rate of rise of on-state current after triggering (I_{TM} = 10 A; I_G = 50 mA; dI_G /dt = 50 mA/ms)	dI_T /dt	50	A/μs
Peak gate current	I_{GM}	2	A
Peak gate voltage	V_{GM}	5	V
Peak reverse gate voltage	V_{RGM}	5	V
Peak gate power (over any 20 ms period)	P_{GM}	5	W
Average gate power	$P_{G(AV)}$	0.5	W
Storage temperature	T_{stg}	-40~150	℃
Operating junction temperature	T_j	125**	℃

*Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15A/μs.
** Note: operation above 110℃ may require the use of a gate to cathode resistor of 1kΩ or less.

THERMAL RESISTANCES

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Thermal resistance Junction to mounting base	$R_{th\ j\text{-}mb}$			2.5	K/W
Thermal resistance Junction to ambient In free air	$R_{th\ j\text{-}a}$		60		K/W

STATIC CHARACTERISTICS(T_j=25°C,unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Gate trigger current	I_{GT}	V_D = 12 V; I_T = 0.1 A		15	200	mA
Latching current	I_L	V_D = 12 V; I_{GT} = 0.1 A		0.17	10	mA
Holding current	I_H	V_D = 12 V; I_{GT} = 0.1 A		0.10	6	MA
On-state voltage	V_T	I_T = 5 A		1.23	1.8	V
Gate trigger voltage	V_{GT}	V_D = 12 V; I_T = 0.1 A V_D = VDRM(max) ; I_T = 0.1 A; T_j = 110 °C	 0.1	0.4 0.2	1.5	V
Off-state leakage current	I_D , I_R	V_D = $V_{DRM(max)}$; V_R = VRRM(max) ; T_j = 125 °C		0.1	0.5	mA

DYNAMIC CHARACTERISTICS(T_j=25°C,unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Critical rate of rise of off-state voltage	dV_D /dt	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 °C; exponential waveform; R_{GK} = 100 Ω		50		V/μs
Gate controlled turn-on time	t_{gt}	I_{TM} = 10 A; V_D = $V_{DRM(max)}$; I_G = 5mA; dI_G /dt = 0.2A/μs		2		μs
Circuit commutated Turn-off time	t_q	V_D = 67% $V_{DRM(max)}$; T_j = 125 °C; I_{TM} = 8A; V_R = 10V; dI_{TM} /dt = 10 A/μs; dV_D /dt = 2V/μs; R_{GK} = 1kΩ		100		μs

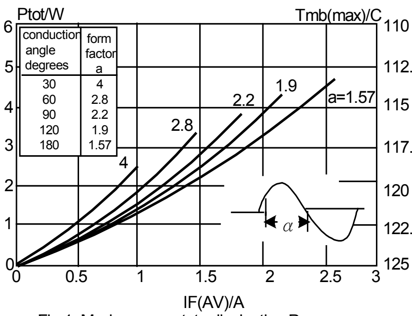


Fig.1. Maximum on-state dissipation,P_{tot},versus average on-state current,$I_{T(AV)}$,where a=form factor=$I_{T(RMS)}/I_{T(AV)}$.

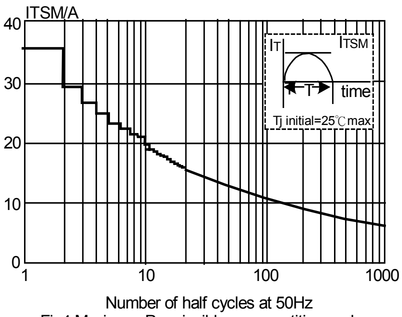


Fig4.Maximum Permissible non-repetitive peak on-state current I_{TSM},versus number of cycles,for sinusoidal currents,f=50Hz.

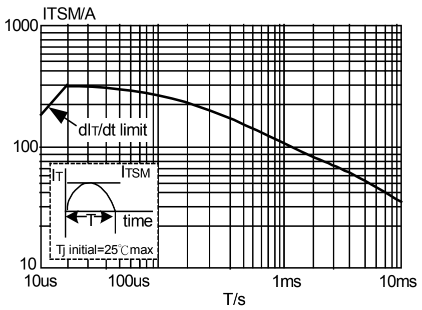


Fig.2.Maximum Permissible non-repetitive peak on-state Current I_{TSM},versus pulse width t_p, for sinusoidal currents,t_p≒10ms

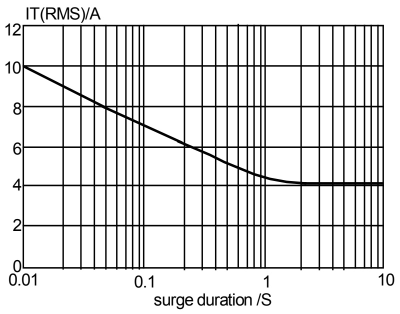


Fig. 5.Maximum permissible repetitive rms on-state current $I_{T(RMS)}$,versus surge duration,for sinusoidal currents,f=50Hz;T_{mb} ≦113℃

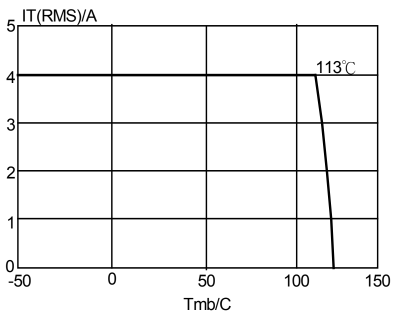


Fig.3. Maximum permissible rms current IT(RMS), versus mounting base temperature T_{mb}

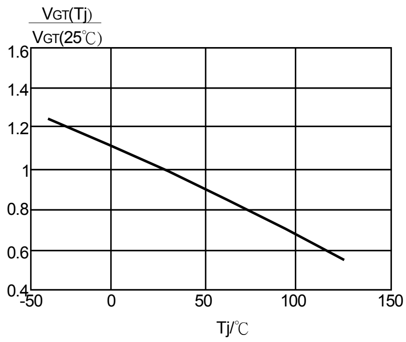


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}$(25℃,versus junction temperature T_j.

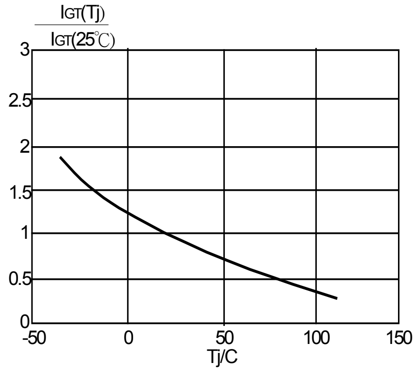


Fig. 7.Normalised gate trigger Current $I_{GT}(T_j)/I_{GT}(25℃)$,versus junction temperature T_j.

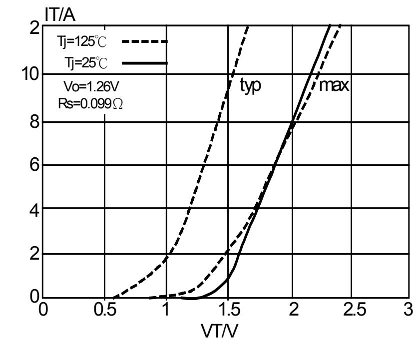


Fig.10.Typical and maximum on-state characteristic.

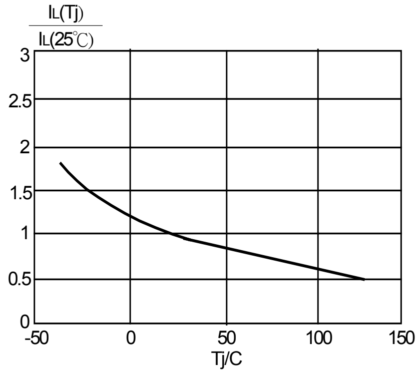


Fig.8.Normalised latching Current $I_L(T_j)/I_L(25℃)$, versus junction temperature T_j

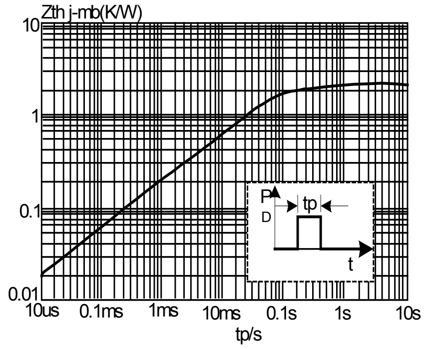


Fig.11.Transient thermal impedance $Z_{thj\text{-}mb}$,versus pulse width t_p.

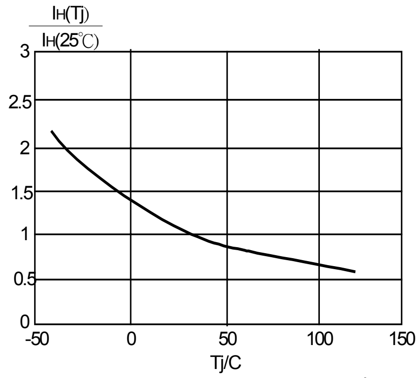


Fig. 9.Normalised holding current $I_H(T_j)/I_H(25℃)$, versus junction temperature T_j.

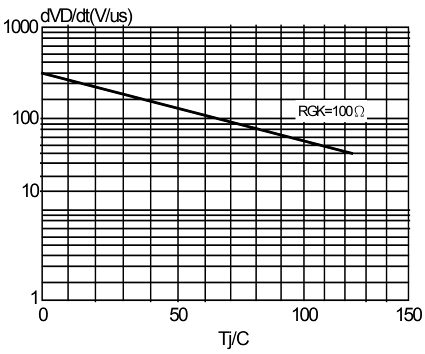


Fig.12.Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.