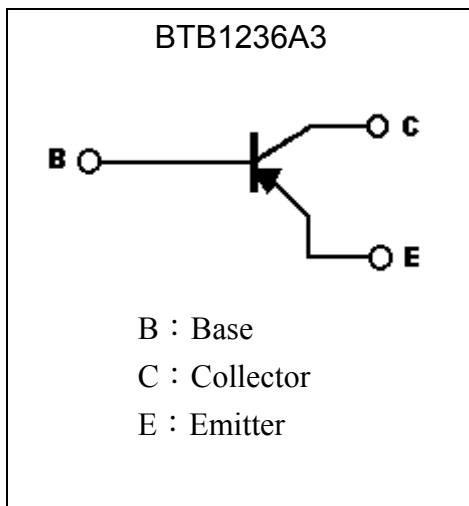
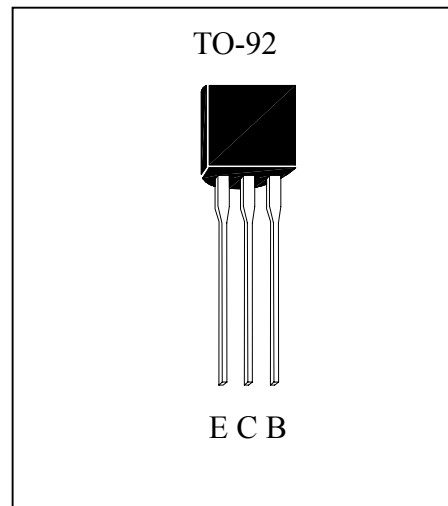


**Silicon PNP Epitaxial Planar Transistor**

# BTB1236A3

**Description**

- High  $BV_{CEO}$
- High current capability

**Symbol**

**Outline**

**Absolute Maximum Ratings** ( $T_a=25^{\circ}\text{C}$ )

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	$V_{CBO}$	-180	V
Collector-Emitter Voltage	$V_{CEO}$	-160	V
Emitter-Base Voltage	$V_{EBO}$	-5	V
Collector Current (DC)	$I_C$	-1.5	A
Collector Current (Pulse)	$I_{CP}$	-3	A
Base Current	$I_B$	0.5	A
Power Dissipation (Note)	$P_d$	900	mW
Junction Temperature	$T_j$	150	$^{\circ}\text{C}$
Storage Temperature	$T_{stg}$	-55~+150	$^{\circ}\text{C}$

Note : Transistor mounted on a printed-circuit board.

**Characteristics (Ta=25°C)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
$BV_{CBO}$	-180	-	-	V	$I_C=-50\mu A, I_E=0$
$BV_{CEO}$	-160	-	-	V	$I_C=-1mA, I_B=0$
$BV_{EBO}$	-5	-	-	V	$I_E=-50\mu A, I_C=0$
$I_{CBO}$	-	-	-1	$\mu A$	$V_{CB}=-160V, I_E=0$
$I_{EBO}$	-	-	-1	$\mu A$	$V_{EB}=-4V, I_C=0$
* $V_{CE(sat)}$	-	-	-0.6	V	$I_C=-1A, I_B=-100mA$
* $V_{BE(on)}$	-	-	-1.5	V	$V_{CE}=-5V, I_C=-150mA$
$h_{FE1}$	60	-	200	-	$V_{CE}=-5V, I_C=-100mA$
$h_{FE2}$	30	-	-	-	$V_{CE}=-5V, I_C=-500mA$
$f_T$	-	140	-	MHz	$V_{CE}=-5V, I_C=-150mA$
Cob	-	27	-	pF	$V_{CB}=-10V, I_E=0, f=1MHz$

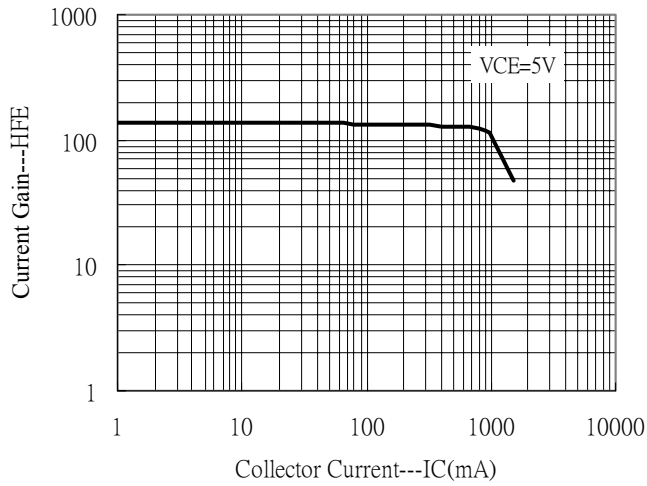
\*Pulse Test: Pulse Width  $\leq 380\mu s$ , Duty Cycle  $\leq 2\%$ **Classification of  $h_{FE} 1$** 

Rank	K	P	Q
Range	60~120	82~190	120~200

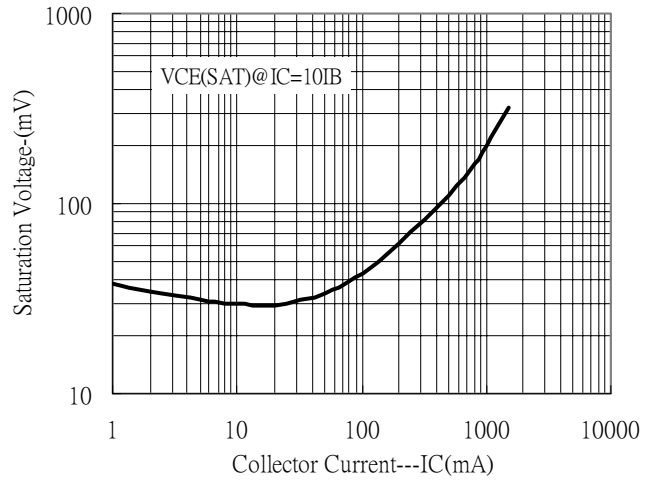


### Characteristic Curves

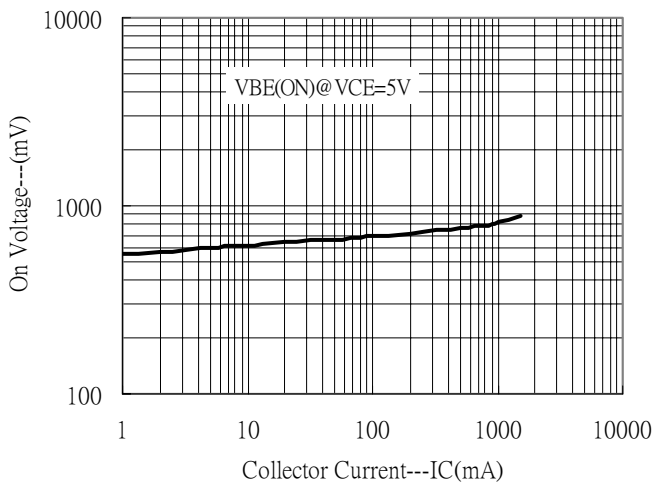
Current Gain vs Collector Current



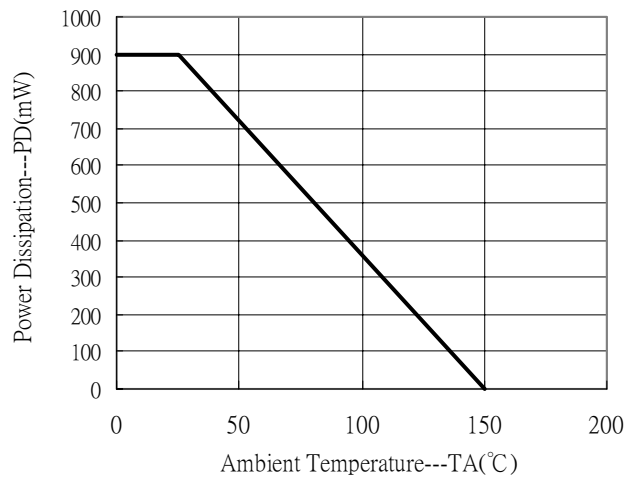
Saturation Voltage vs Collector Current



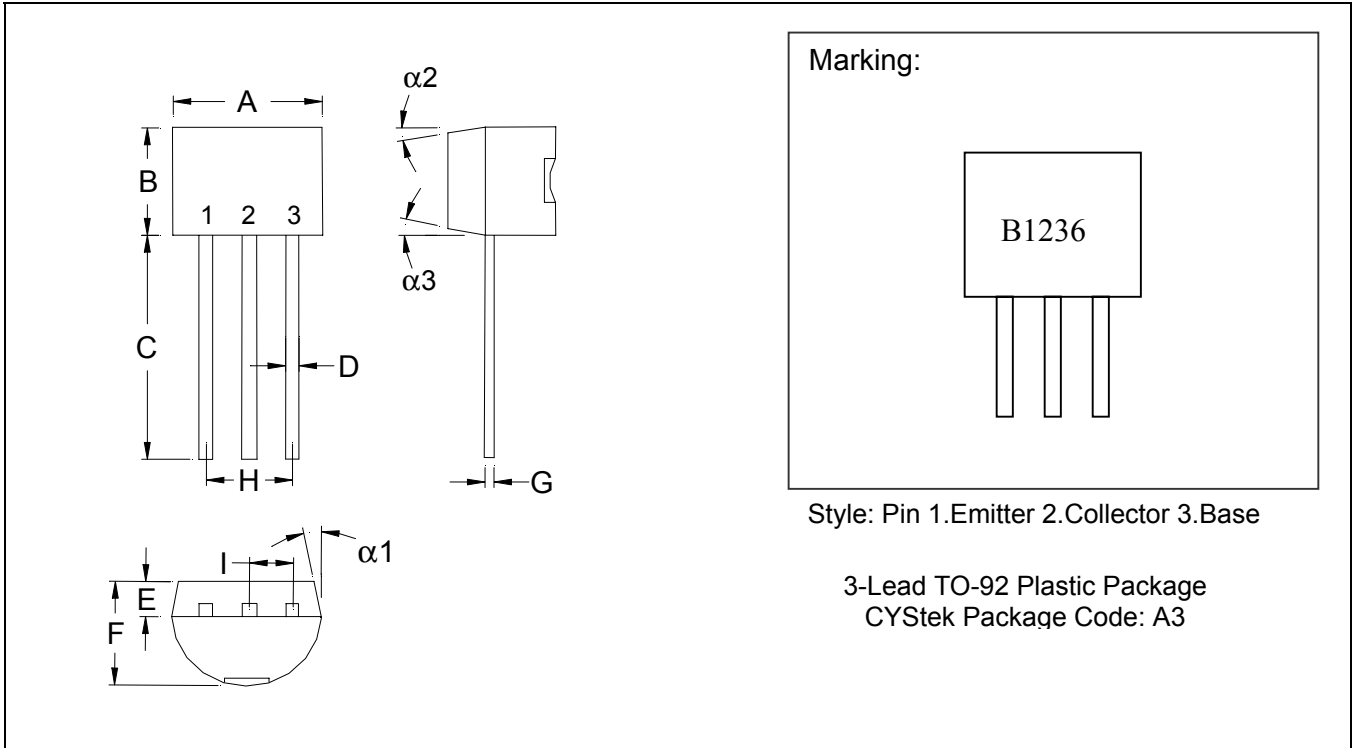
On Voltage vs Collector Current



Power Derating Curve



**TO-92 Dimension**



\*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1704	0.1902	4.33	4.83	G	0.0142	0.0220	0.36	0.56
B	0.1704	0.1902	4.33	4.83	H	-	*0.1000	-	*2.54
C	0.5000	-	12.70	-	I	-	*0.0500	-	*1.27
D	0.0142	0.0220	0.36	0.56	$\alpha 1$	-	*5°	-	*5°
E	-	*0.0500	-	*1.27	$\alpha 2$	-	*2°	-	*2°
F	0.1323	0.1480	3.36	3.76	$\alpha 3$	-	*2°	-	*2°

Notes: 1. Controlling dimension: millimeters.  
 2. Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3. If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead: 42 Alloy ; solder plating
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

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