

# BUK7222-55A

TrenchMOS™ standard level FET

Rev. 01 — 17 April 2001

Product specification

## 1. Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™<sup>1</sup> technology, featuring very low on-state resistance.

Product availability:

BUK7222-55A in SOT428 (D-PAK).

## 2. Features

- TrenchMOS™ technology
- Q101 compliant
- 175 °C rated
- Standard level compatible.

## 3. Applications

- Automotive and general purpose power switching:
  - ◆ 12 V and 24 V loads
  - ◆ Motors, lamps and solenoids.

## 4. Pinning information

Table 1: Pinning - SOT428 (D-PAK), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	<p style="text-align: center;">Top view <span style="margin-left: 50px;">MBK091</span></p> <p style="text-align: center;"><b>SOT428 (D-PAK)</b></p>	<p style="text-align: center;">MBB076</p>
2	drain (d)		
3	source (s)		
mb	drain (d)		

1. TrenchMOS is a trademark of Royal Philips Electronics.



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## 5. Quick reference data

**Table 2: Quick reference data**

Symbol	Parameter	Conditions	Typ	Max	Unit
$V_{DS}$	drain-source voltage (DC)		–	55	V
$I_D$	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V}$	–	48	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$	–	103	W
$T_j$	junction temperature		–	175	°C
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}$			
		$T_j = 25\text{ °C}$	19	22	mΩ
		$T_j = 175\text{ °C}$	–	44	mΩ

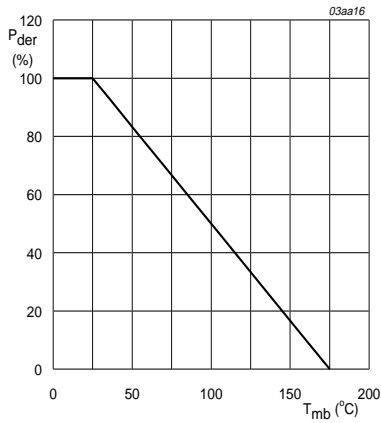
## 6. Limiting values

**Table 3: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

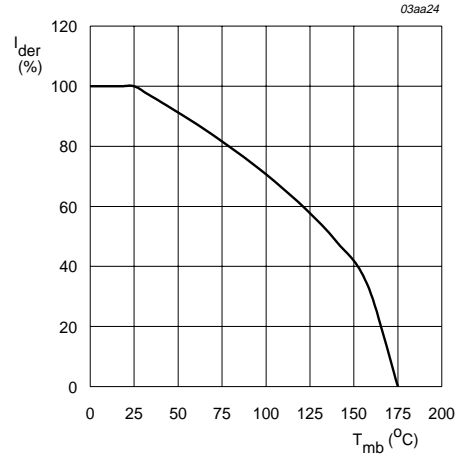
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage (DC)		–	55	V
$V_{DGR}$	drain-gate voltage (DC)	$R_{GS} = 20\text{ k}\Omega$	–	55	V
$V_{GS}$	gate-source voltage (DC)		–	±20	V
$I_D$	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ <b>Figure 2 and 3</b>	–	48	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 10\text{ V};$ <b>Figure 2</b>	–	34	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ <b>Figure 3</b>	[1]	193	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ <b>Figure 1</b>	–	103	W
$T_{stg}$	storage temperature		–55	+175	°C
$T_j$	operating junction temperature		–55	+175	°C
<b>Source-drain diode</b>					
$I_{DR}$	reverse drain current (DC)	$T_{mb} = 25\text{ °C}$	–	48	A
$I_{DRM}$	pulsed reverse drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s}$	–	193	A
<b>Avalanche ruggedness</b>					
$W_{DSS}$	non-repetitive avalanche energy	unclamped inductive load; $I_D = 48\text{ A};$ $V_{DS} \leq 55\text{ V}; V_{GS} = 10\text{ V}; R_{GS} = 50\text{ }\Omega;$ starting $T_j = 25\text{ °C}$	–	160	mJ

[1]  $I_{DM}$  is limited by chip, not package.



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

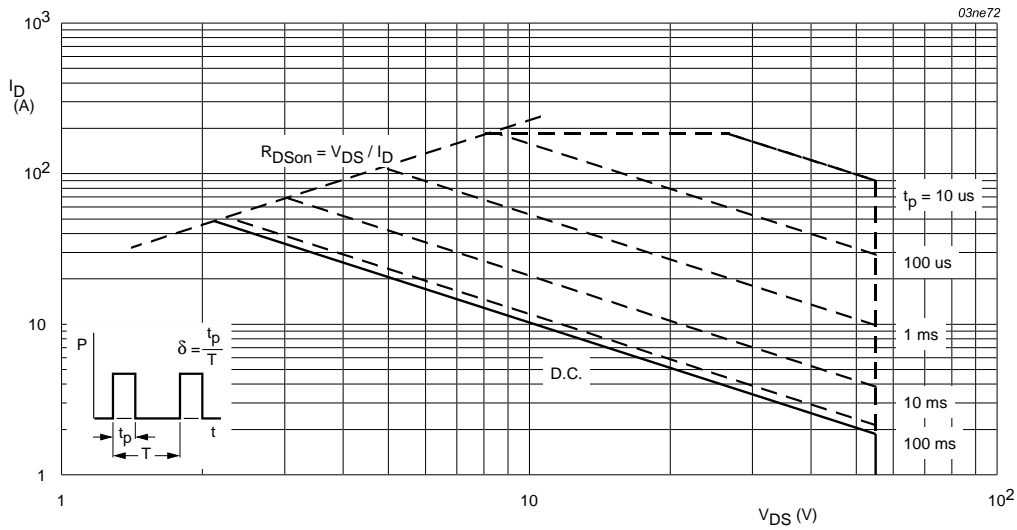
**Fig 1. Normalized total power dissipation as a function of mounting base temperature.**



$$V_{GS} \geq 4.5 \text{ V}$$

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

**Fig 2. Normalized continuous drain current as a function of mounting base temperature.**



T<sub>mb</sub> = 25 °C; I<sub>DM</sub> is single pulse.

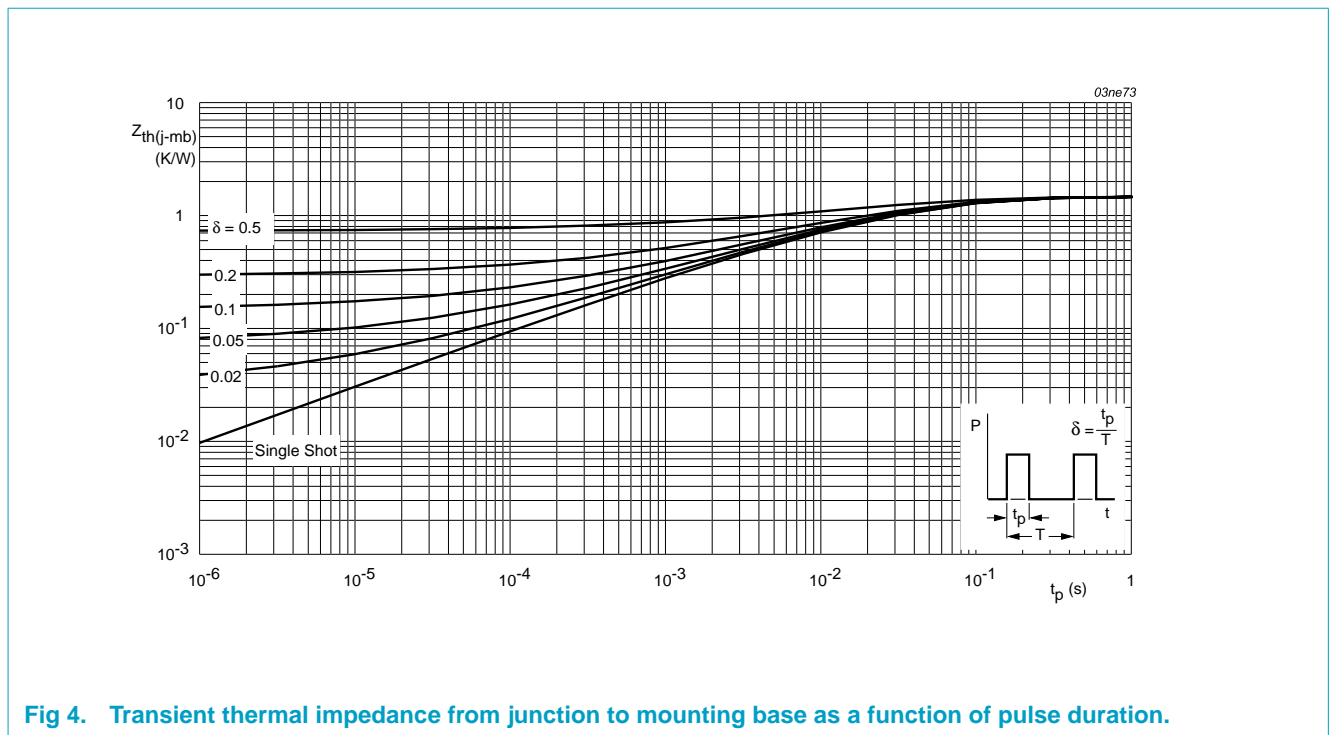
**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.**

## 7. Thermal characteristics

**Table 4: Thermal characteristics**

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint, FR4 board	71.4	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	1.5	K/W

### 7.1 Transient thermal impedance



**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.**

## 8. Characteristics

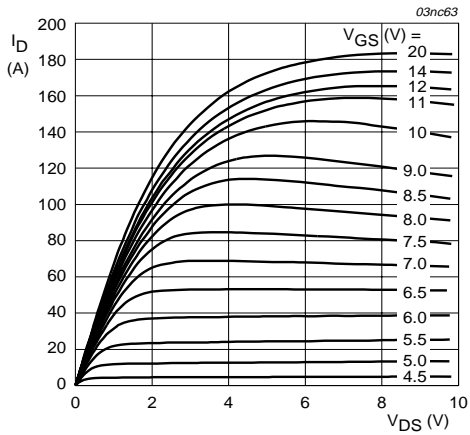
**Table 5: Characteristics**
*T<sub>j</sub> = 25 °C unless otherwise specified*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 0.25 mA; V <sub>GS</sub> = 0 V T <sub>j</sub> = 25 °C	55	–	–	V
		T <sub>j</sub> = –55 °C	50	–	–	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; Figure 9				
		T <sub>j</sub> = 25 °C	2	3	4	V
		T <sub>j</sub> = 175 °C	1	–	–	V
		T <sub>j</sub> = –55 °C	–	–	4.4	V
I <sub>DSS</sub>	drain-source leakage current	V <sub>DS</sub> = 55 V; V <sub>GS</sub> = 0 V T <sub>j</sub> = 25 °C	–	0.05	10	μA
		T <sub>j</sub> = 175 °C	–	–	500	μA
I <sub>GSS</sub>	gate-source leakage current	V <sub>GS</sub> = ±20 V; V <sub>DS</sub> = 0 V	–	2	100	nA
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; Figure 7 and 8				
		T <sub>j</sub> = 25 °C	–	19	22	mΩ
		T <sub>j</sub> = 175 °C	–	–	44	mΩ
<b>Dynamic characteristics</b>						
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V;	–	1200	1597	pF
C <sub>oss</sub>	output capacitance	f = 1 MHz; Figure 12	–	290	349	pF
C <sub>rss</sub>	reverse transfer capacitance		–	180	245	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DD</sub> = 30 V; R <sub>L</sub> = 1.2 Ω;	–	15	–	ns
t <sub>r</sub>	rise time	V <sub>GS</sub> = 10 V; R <sub>G</sub> = 10 Ω;	–	74	–	ns
t <sub>d(off)</sub>	turn-off delay time		–	70	–	ns
t <sub>f</sub>	fall time		–	40	–	ns
L <sub>d</sub>	internal drain inductance	measured from drain to centre of die	–	2.5	–	nH
L <sub>s</sub>	internal source inductance	measured from source lead to source bond pad	–	7.5	–	nH

**Table 5: Characteristics...continued**

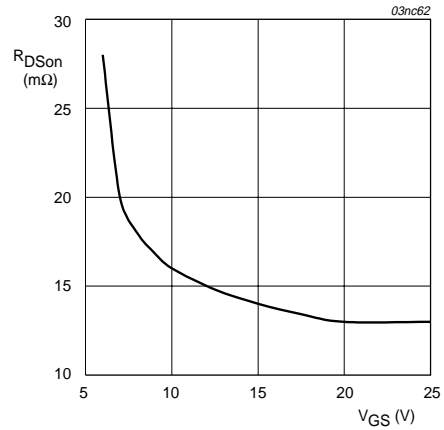
$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
$V_{SD}$	source-drain (diode forward) voltage	$I_S = 20\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; <b>Figure 15</b>	–	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20\text{ A}$ ; $dI_S/dt = -100\text{ A}/\mu\text{s}$	–	45	–	ns
$Q_r$	recovered charge	$V_{GS} = -10\text{ V}$ ; $V_{DS} = 30\text{ V}$	–	110	–	nC



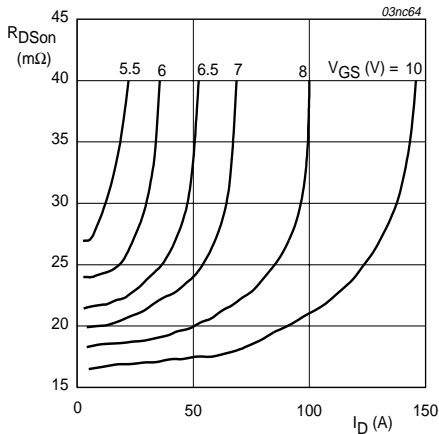
$T_j = 25\text{ }^\circ\text{C}$

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.**



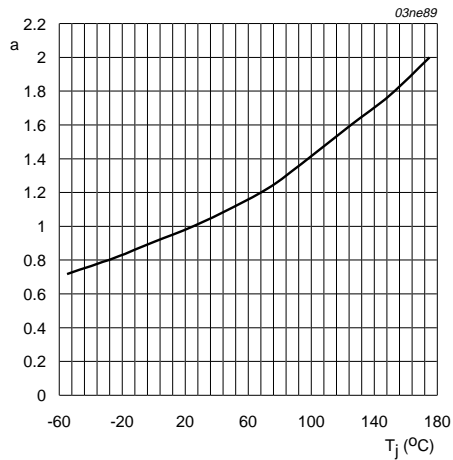
$T_j = 25\text{ }^\circ\text{C}$ ;  $I_D = 25\text{ A}$

**Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.**



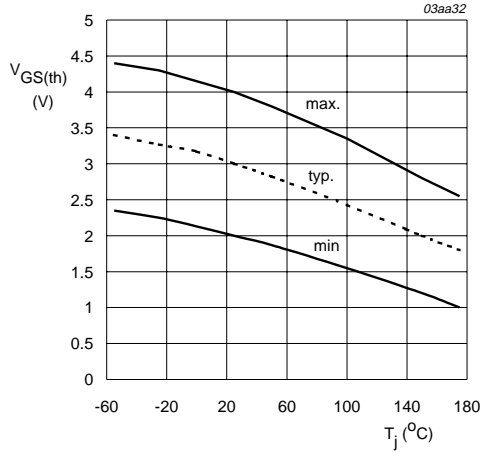
$T_j = 25\text{ }^\circ\text{C}$

**Fig 7. Drain-source on-state resistance as a function of drain current; typical values.**



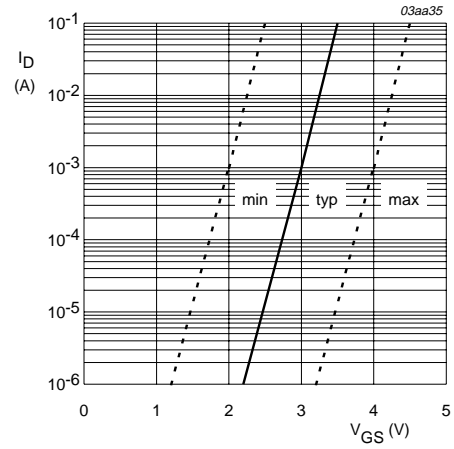
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

**Fig 8. Normalized drain source on-state resistance factor as a function of junction temperature.**



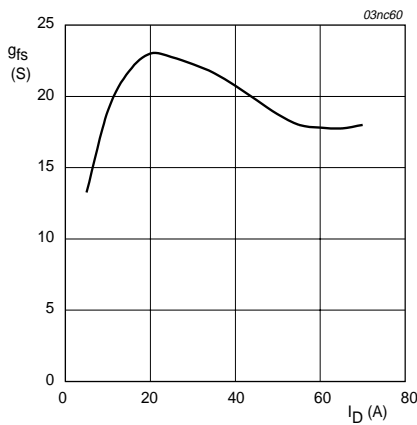
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

**Fig 9. Gate-source threshold voltage as a function of junction temperature.**



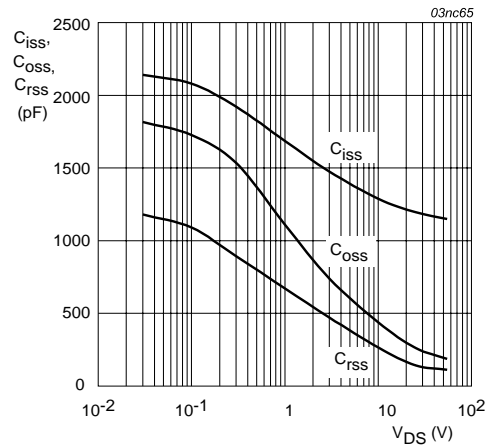
$T_j = 25 \text{ }^{\circ}C; V_{DS} = V_{GS}$

**Fig 10. Sub-threshold drain current as a function of gate-source voltage.**



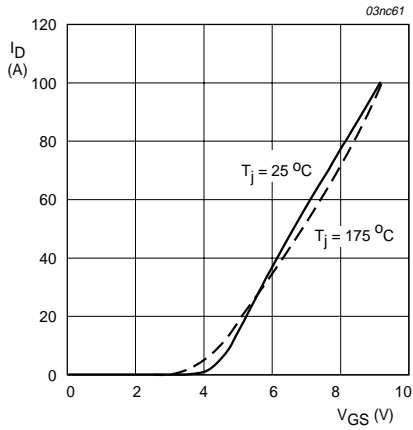
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 25 \text{ V}$

**Fig 11. Forward transconductance as a function of drain current; typical values.**



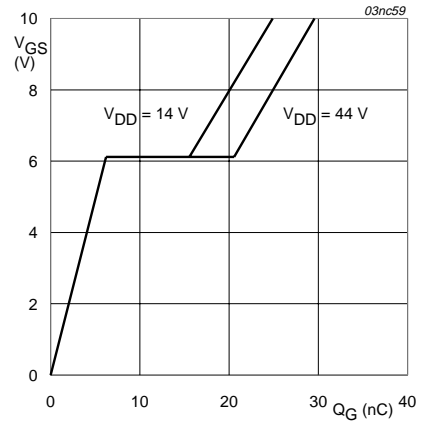
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

**Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.**



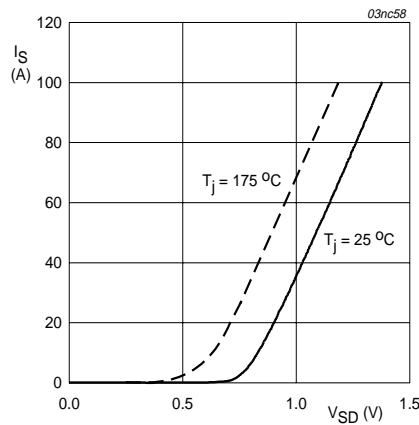
$V_{DS} = 25\text{ V}$

**Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.**



$T_j = 25\text{ }^\circ\text{C}; I_D = 25\text{ A}$

**Fig 14. Gate-source voltage as a function of turn-on gate charge; typical values.**



$V_{GS} = 0\text{ V}$

**Fig 15. Reverse diode current as a function of reverse diode voltage; typical values.**



**9. Package outline**

**Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads (one lead cropped)**

**SOT428**



**Fig 16. SOT428 (D-PAK).**

## 10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20010417	-	Product specification; initial version.

## 11. Data sheet status

Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup>	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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