

## TrenchMOS™ transistor Standard level FET

BUK7621-30

### GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope suitable for surface mounting using 'trench' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

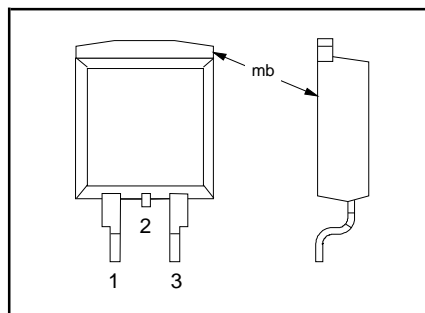
### QUICK REFERENCE DATA

| SYMBOL       | PARAMETER  | MAX. | UNIT |
|--------------|--|------|------|
| $V_{DS}$     | Drain-source voltage                             | 30   | V    |
| $I_D$        | Drain current (DC)                               | 50   | A    |
| $P_{tot}$    | Total power dissipation                          | 94   | W    |
| $T_j$        | Junction temperature                             | 175  | °C   |
| $R_{DS(ON)}$ | Drain-source on-state resistance $V_{GS} = 10$ V | 21   | mΩ   |

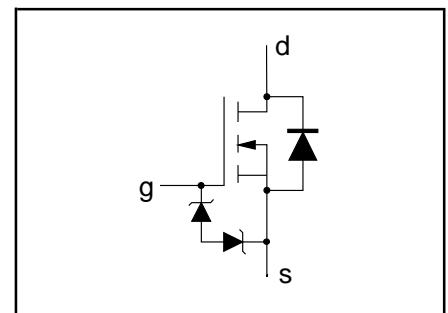
### PINNING - SOT404 (D<sup>2</sup>PAK)

| PIN | DESCRIPTION |
|-----|-------------|
| 1   | gate        |
| 2   | drain       |
| 3   | source      |
| mb  | drain       |

### PIN CONFIGURATION



### SYMBOL



### LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| SYMBOL         | PARAMETER                        | CONDITIONS        | MIN. | MAX. | UNIT |
|----------------|----------------------------------|-------------------|------|------|------|
| $V_{DS}$       | Drain-source voltage             | -                 | -    | 30   | V    |
| $V_{DGR}$      | Drain-gate voltage               | $R_{GS} = 20$ kΩ  | -    | 30   | V    |
| $\pm V_{GS}$   | Gate-source voltage              | -                 | -    | 20   | V    |
| $I_D$          | Drain current (DC)               | $T_{mb} = 25$ °C  | -    | 50   | A    |
| $I_D$          | Drain current (DC)               | $T_{mb} = 100$ °C | -    | 29   | A    |
| $I_{DM}$       | Drain current (pulse peak value) | $T_{mb} = 25$ °C  | -    | 200  | A    |
| $P_{tot}$      | Total power dissipation          | $T_{mb} = 25$ °C  | -    | 94   | W    |
| $T_{stg}, T_j$ | Storage & operating temperature  | -                 | - 55 | 175  | °C   |

### THERMAL RESISTANCES

| SYMBOL         | PARAMETER                                    | CONDITIONS                     | TYP. | MAX. | UNIT |
|----------------|--|--------------------------------|------|------|------|
| $R_{th\ j-mb}$ | Thermal resistance junction to mounting base | -                              | -    | 1.6  | K/W  |
| $R_{th\ j-a}$  | Thermal resistance junction to ambient       | pcb mounted, minimum footprint | 50   | -    | K/W  |

### ESD LIMITING VALUE

| SYMBOL | PARAMETER   | CONDITIONS                        | MIN. | MAX. | UNIT |
|--------|---|-----------------------------------|------|------|------|
| $V_C$  | Electrostatic discharge capacitor voltage, all pins | Human body model (100 pF, 1.5 kΩ) | -    | 2    | kV   |

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### STATIC CHARACTERISTICS

T<sub>j</sub> = 25°C unless otherwise specified

| SYMBOL                | PARAMETER                        | CONDITIONS  | MIN.            | TYP.          | MAX.            | UNIT        |
|-----------------------|----------------------------------|---|-----------------|---------------|-----------------|-------------|
| V <sub>(BR)DSS</sub>  | Drain-source breakdown voltage   | V <sub>GS</sub> = 0 V; I <sub>D</sub> = 0.25 mA;<br>T <sub>j</sub> = -55°C                                    | 30<br>27        | -<br>-        | -<br>-          | V<br>V      |
| V <sub>GS(TO)</sub>   | Gate threshold voltage           | V <sub>DS</sub> = V <sub>GS</sub> ; I <sub>D</sub> = 1 mA<br>T <sub>j</sub> = 175°C<br>T <sub>j</sub> = -55°C | 2.0<br>1.0<br>- | 3.0<br>-<br>- | 4.0<br>-<br>4.4 | V<br>V<br>V |
| I <sub>DSS</sub>      | Zero gate voltage drain current  | V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 0 V;<br>T <sub>j</sub> = 175°C                                      | -               | 0.05          | 10              | μA          |
| I <sub>GSS</sub>      | Gate source leakage current      | V <sub>GS</sub> = ±10 V; V <sub>DS</sub> = 0 V<br>T <sub>j</sub> = 175°C                                      | -               | 0.02          | 1<br>500        | μA<br>μA    |
| ±V <sub>(BR)GSS</sub> | Gate source breakdown voltage    | I <sub>G</sub> = ±1 mA;<br>T <sub>j</sub> = 175°C   | 16              | -             | -               | V           |
| R <sub>DS(ON)</sub>   | Drain-source on-state resistance | V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A<br>T <sub>j</sub> = 175°C                                       | -               | 19            | 21<br>39        | mΩ<br>mΩ    |

### DYNAMIC CHARACTERISTICS

T<sub>j</sub> = 25°C unless otherwise specified

| SYMBOL              | PARAMETER                  | CONDITIONS  | MIN. | TYP. | MAX. | UNIT |
|---------------------|----------------------------|---|------|------|------|------|
| g <sub>fs</sub>     | Forward transconductance   | V <sub>DS</sub> = 25 V; I <sub>D</sub> = 25 A                         | 6    | 19   | -    | S    |
| Q <sub>g(tot)</sub> | Total gate charge          | I <sub>D</sub> = 25 A; V <sub>DD</sub> = 30 V; V <sub>GS</sub> = 10 V | -    | 28   | -    | nC   |
| Q <sub>gs</sub>     | Gate-source charge         |   | -    | 7    | -    | nC   |
| Q <sub>gd</sub>     | Gate-drain (Miller) charge |   | -    | 11   | -    | nC   |
| C <sub>iss</sub>    | Input capacitance          | V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz              | -    | 974  | -    | pF   |
| C <sub>oss</sub>    | Output capacitance         |   | -    | 325  | -    | pF   |
| C <sub>rss</sub>    | Feedback capacitance       |   | -    | 152  | -    | pF   |
| t <sub>d on</sub>   | Turn-on delay time         | V <sub>DD</sub> = 30 V; I <sub>D</sub> = 25 A;                        | -    | 10   | -    | ns   |
| t <sub>r</sub>      | Turn-on rise time          | V <sub>GS</sub> = 10 V; R <sub>G</sub> = 10 Ω                         | -    | 45   | -    | ns   |
| t <sub>d off</sub>  | Turn-off delay time        | Resistive load  | -    | 30   | -    | ns   |
| t <sub>f</sub>      | Turn-off fall time         |   | -    | 32   | -    | ns   |
| L <sub>d</sub>      | Internal drain inductance  | Measured from tab to centre of die                                    | -    | 3.5  | -    | nH   |
| L <sub>d</sub>      | Internal drain inductance  | Measured from drain lead solder point to centre of die                | -    | 4.5  | -    | nH   |
| L <sub>s</sub>      | Internal source inductance | Measured from source lead solder point to source bond pad             | -    | 7.5  | -    | nH   |

### REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T<sub>j</sub> = 25°C unless otherwise specified

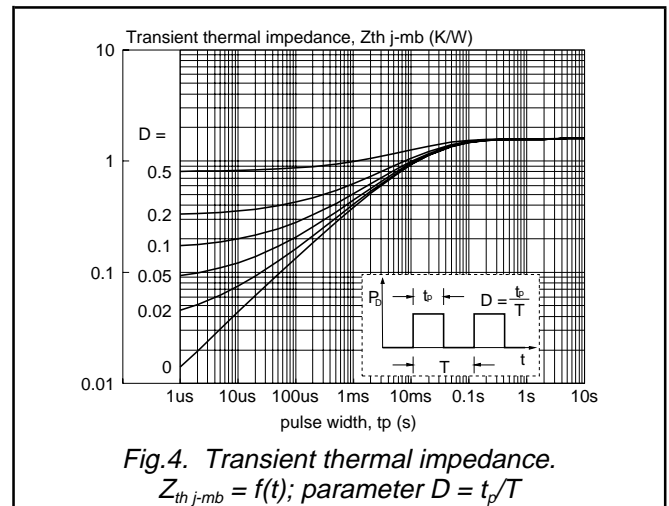
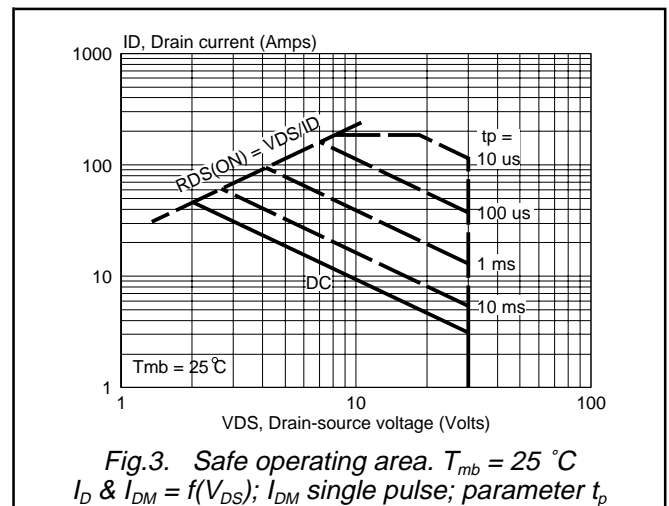
| SYMBOL           | PARAMETER                        | CONDITIONS   | MIN. | TYP.        | MAX.     | UNIT |
|------------------|----------------------------------|--|------|-------------|----------|------|
| I <sub>DR</sub>  | Continuous reverse drain current |  | -    | -           | 50       | A    |
| I <sub>DRM</sub> | Pulsed reverse drain current     |  | -    | -           | 200      | A    |
| V <sub>SD</sub>  | Diode forward voltage            | I <sub>F</sub> = 25 A; V <sub>GS</sub> = 0 V<br>I <sub>F</sub> = 50 A; V <sub>GS</sub> = 0 V | -    | 0.95<br>1.0 | 1.2<br>- | V    |
| t <sub>rr</sub>  | Reverse recovery time            | I <sub>F</sub> = 25 A; -di <sub>F</sub> /dt = 100 A/μs;                                      | -    | 100         | -        | ns   |
| Q <sub>rr</sub>  | Reverse recovery charge          | V <sub>GS</sub> = -10 V; V <sub>R</sub> = 25 V   | -    | 0.4         | -        | μC   |

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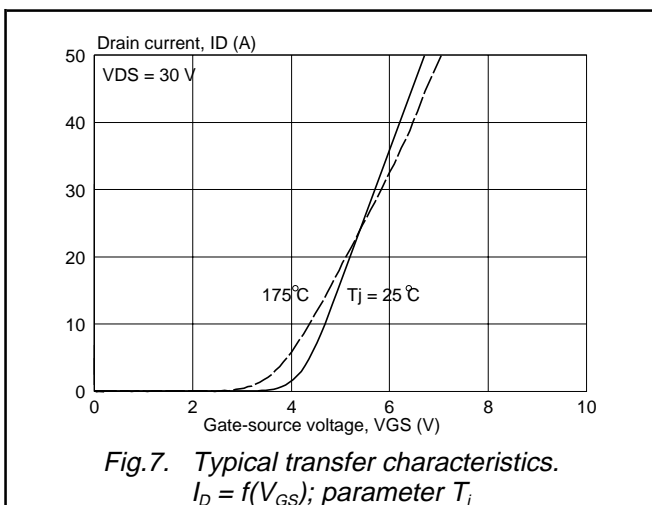
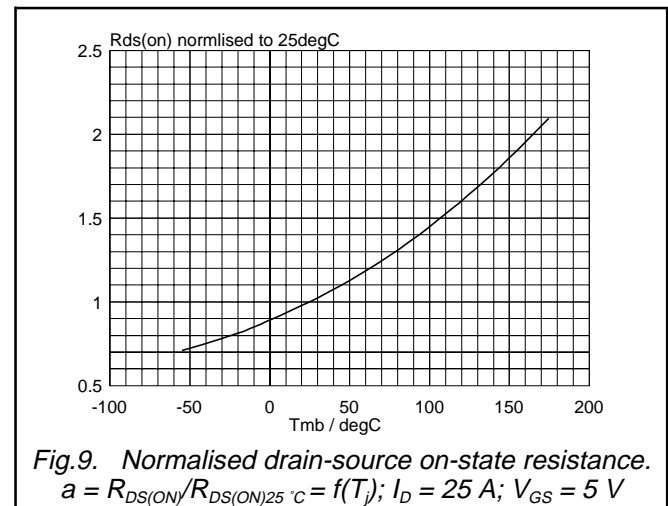
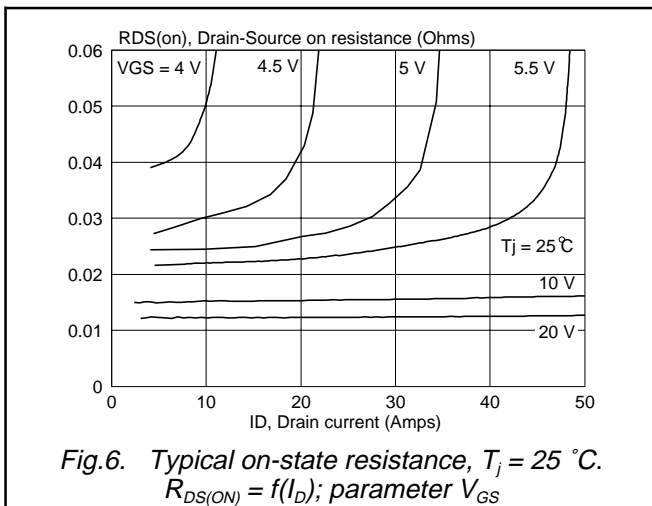
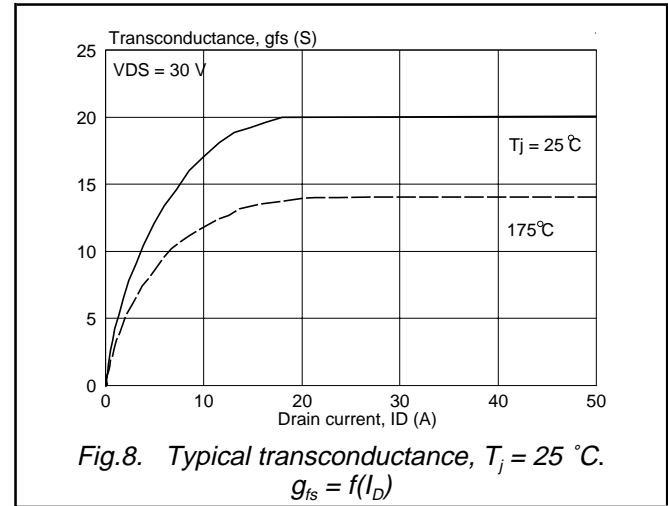
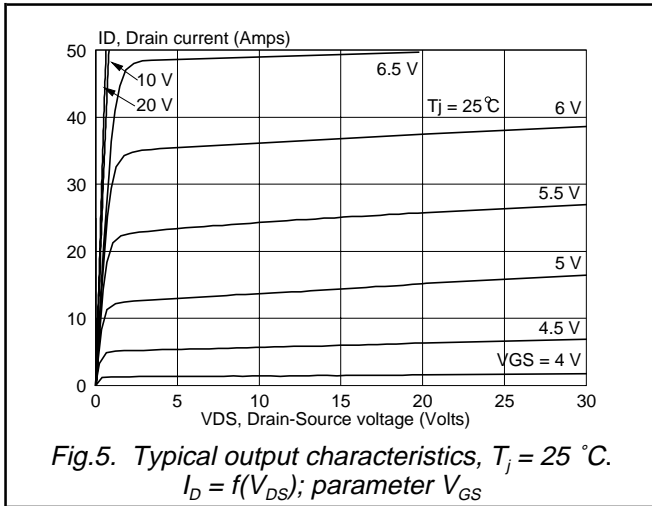
**AVALANCHE LIMITING VALUE**

| SYMBOL    | PARAMETER   | CONDITIONS  | MIN. | TYP. | MAX. | UNIT |
|-----------|---|---|------|------|------|------|
| $W_{DSS}$ | Drain-source non-repetitive unclamped inductive turn-off energy | $I_D = 25 \text{ A}; V_{DD} \leq 25 \text{ V}; V_{GS} = 10 \text{ V}; R_{GS} = 50 \text{ } \Omega; T_{mb} = 25 \text{ } ^\circ\text{C}$ | -    | -    | 70   | mJ   |



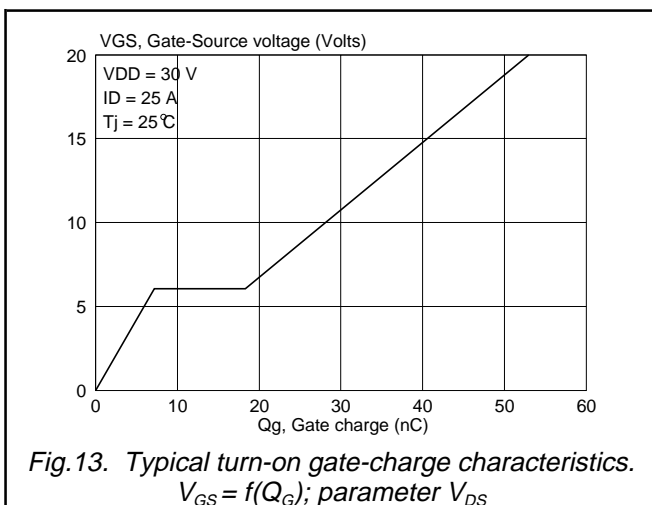
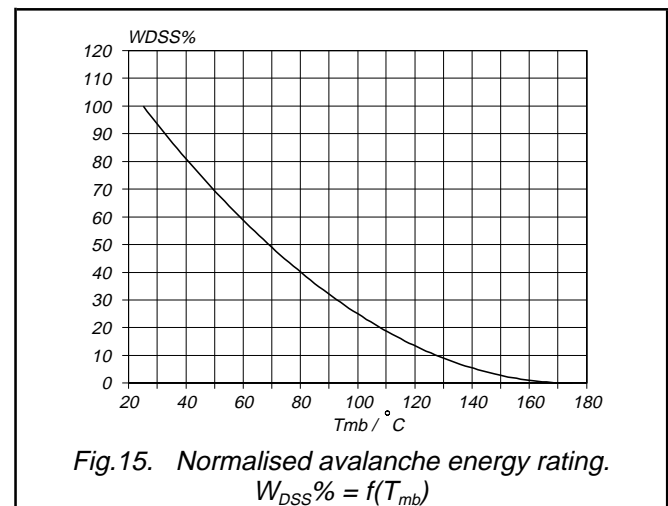
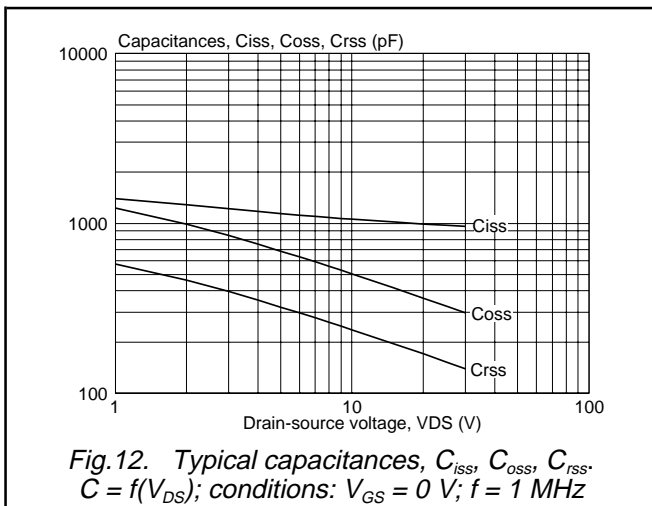
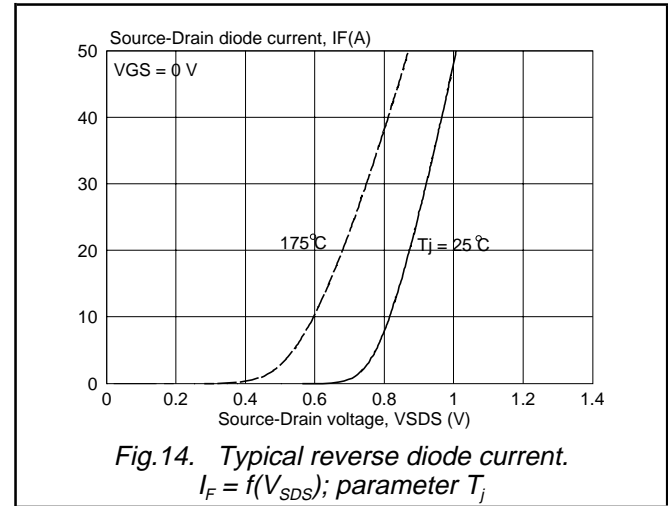
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MECHANICAL DATA

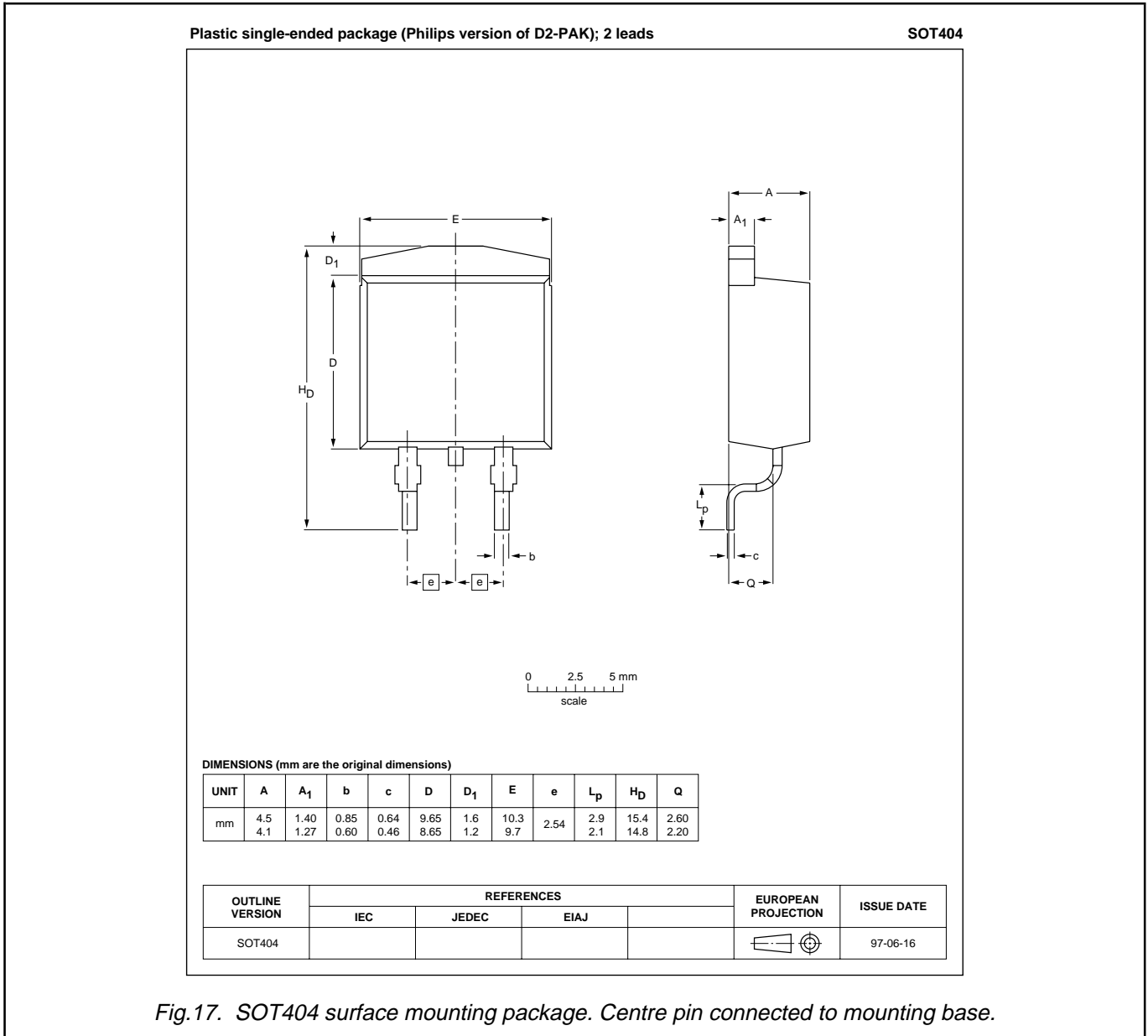


Fig.17. SOT404 surface mounting package. Centre pin connected to mounting base.

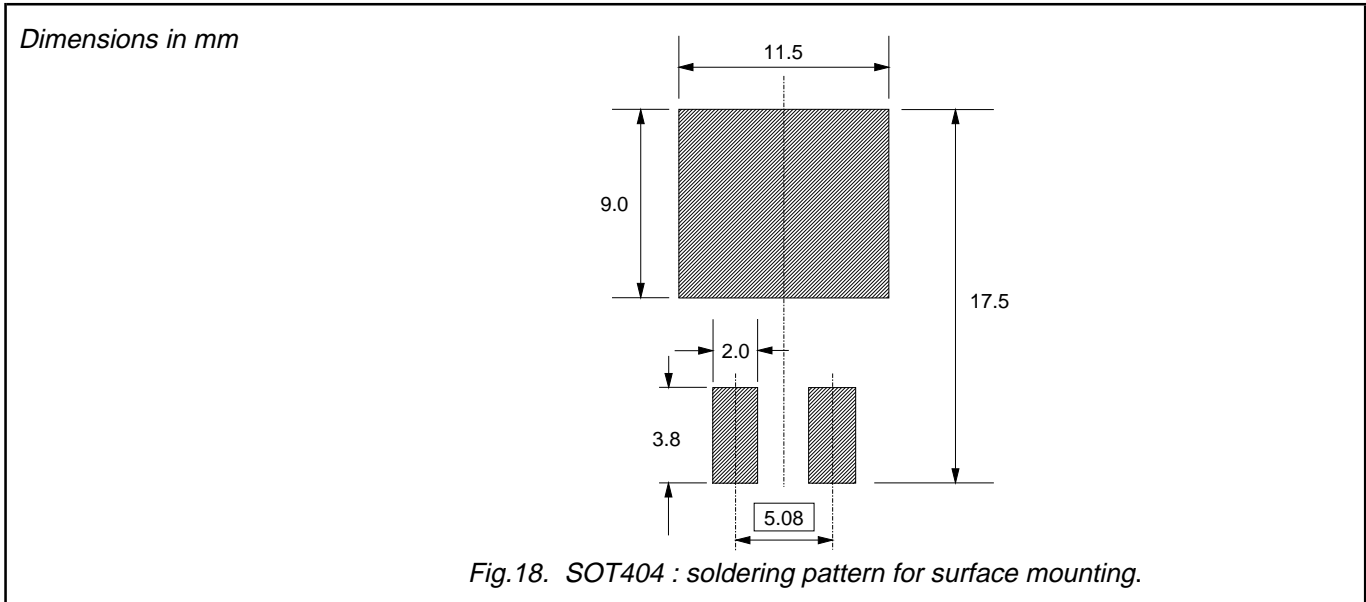
Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

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**MOUNTING INSTRUCTIONS**



**DEFINITIONS**

|  |   |
|--|---|
| <b>Data sheet status</b>   |   |
| Objective specification  | This data sheet contains target or goal specifications for product development.       |
| Preliminary specification  | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification  | This data sheet contains final product specifications.                                |
| <b>Limiting values</b>   |   |
| Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |   |
| <b>Application information</b>   |   |
| Where application information is given, it is advisory and does not form part of the specification.  |   |
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