

## CE7200A-LZ-90.112-LP

### APPROVALS

|                                 |                       |
|---------------------------------|-----------------------|
| <b>RALTRON</b>                  |                       |
| Eng. approval, date:            | Name (please print):  |
| Sales approval, date:           | Title (please print): |
| Created by, date: PartGenerator | Signature, date:      |
| Revision:                       |                       |

### MECHANICAL SPECIFICATION

OUTLINE TOLERANCE:  
+0.015" / 0.4mm  
(Unless otherwise specified)

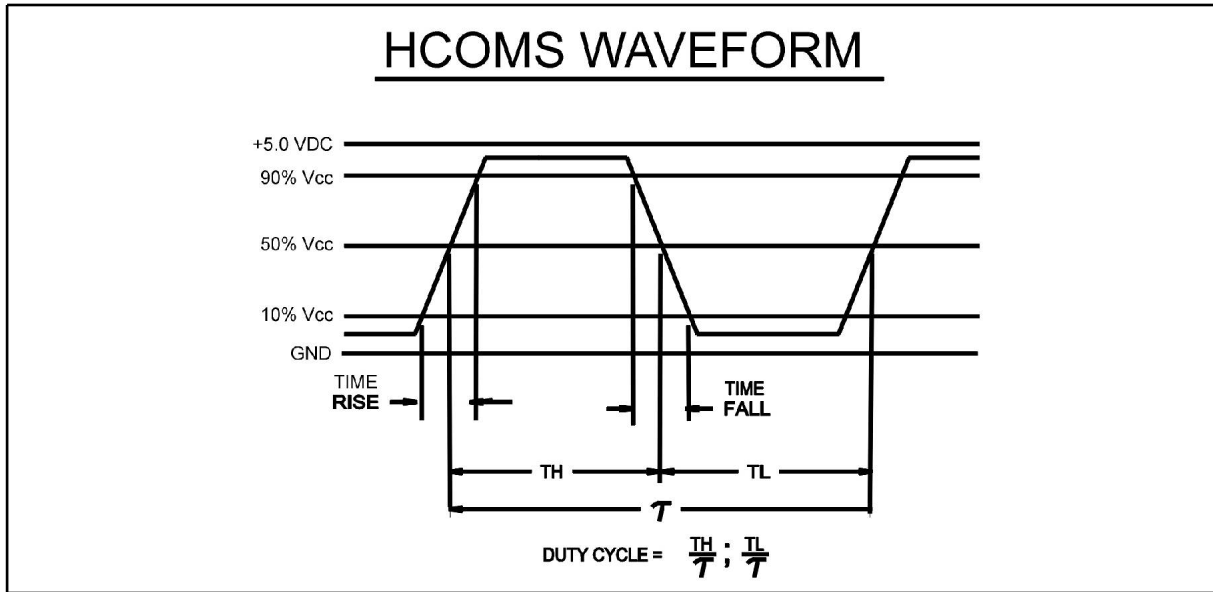
PIN FUNCTIONS:  
[1] ENABLE / DISABLE  
[7] CASE / GROUND  
[8] OUTPUT  
[14] SUPPLY VOLTAGE

MARKING:  
CE7200A-LZ  
90.112-LP  
RAL D/C

### ELECTRICAL SPECIFICATION

| PARAMETER                     | SYMBOL    | CONDITIONS  | VALUE       | UNIT |
|-------------------------------|-----------|---|-------------|------|
| Frequency, nom                | fo        | -   | 90.112      | MHz  |
| Supply Voltage, max.          | Vcc       | Vcc ±5%   | +5.0        | V    |
| Supply Current, max.          | Is        | Vcc=±5%, Ta=+25°C, 15 pF load   | 50.0        | mA   |
| HCMOS output levels           | VOH / VOL | Vcc=+5.0VDC, load=15 pF   | 4.5/0.5     | V    |
| Duty Cycle                    | DC        | load=15pF / @ 50%Vcc, Ta=+25°C  | 40...60     | %    |
| Rise- / fall time, max.       | tr / tf   | 20%~80% Vout, 80%~20% Vout  | 3.00        | ns   |
| Overall freq. stability, max. | Δf/fc     | Including temp., ±5% load & supply variations, calibration @+25°C and 10 year aging | 100.0       | ppm  |
| Enable option (pin 1)         | En        | High or open (min.)   | +2.4        | V    |
| Diabie option (pin 1)         | Dis       | Ground (output pin high impedance)  | +0.4        | V    |
| Operating temperature range   | Ta        | -   | 0...70      | °C   |
| Storage temperature range     | T(stg)    | -   | -55...125   | °C   |
| Absolute voltage Range        | Vcc (abs) | Non-destructive, DC   | -0.5...+7.0 | V    |

■ TIMING DIAGRAM



■ ELECTRICAL TEST DIAGRAM

