

## 4Mb (256K x 16) Pseudo Static RAM

### Features

- Wide voltage range: **2.70V–3.30V**
- Access Time: 70ns
- Ultra-low active power
  - Typical active current: **2.0mA @ f = 1 MHz**
  - Typical active current: **13mA @ f = f<sub>max</sub>**
- Ultra low standby power
- Easy memory expansion with  $\overline{CE}$ ,  $CE_2$ , and  $\overline{OE}$  features
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Offered in a 48 Ball BGA Package

### Functional Description<sup>[1]</sup>

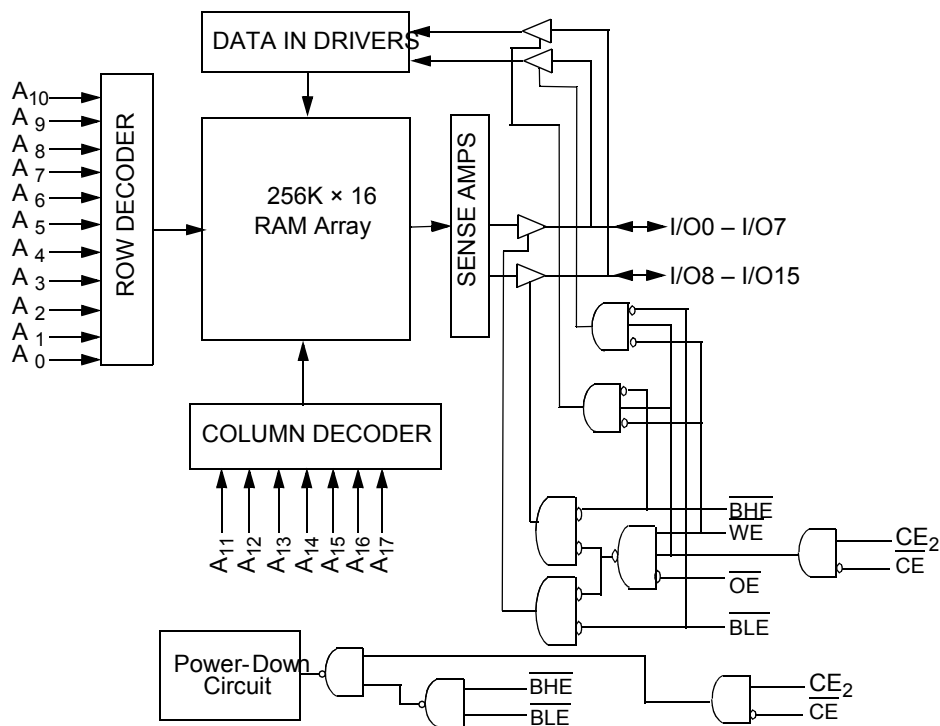
The CG6258AM is a high-performance CMOS Pseudo static RAM organized as 256K words by 16 bits that supports an asynchronous memory interface. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life<sup>®</sup> (MoBL) in portable applications such as cellular telephones. The device can be put into standby mode reducing power consumption by more than 99%. The device can also be put into standby mode

when deselected ( $\overline{CE}$  HIGH or  $CE_2$  LOW or both  $\overline{BHE}$  and  $\overline{BLE}$  are HIGH). The input/output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high-impedance state when: deselected ( $\overline{CE}$  HIGH or  $CE_2$  LOW), outputs are disabled ( $\overline{OE}$  HIGH), both Byte High Enable and Byte Low Enable are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW,  $CE_2$  HIGH and  $\overline{WE}$  LOW). **The addresses must not be toggled once the read is started on the device.**

Writing to the device is accomplished by taking  $\overline{CE}$  LOW and  $CE_2$  HIGH and Write Enable ( $\overline{WE}$ ) input LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from  $I/O$  pins ( $I/O_0$  through  $I/O_7$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{17}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from  $I/O$  pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{17}$ ).

Reading from the device is accomplished by taking  $\overline{CE}$  LOW and  $CE_2$  HIGH and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on  $I/O_8$  to  $I/O_{15}$ . See the truth table at the back of this datasheet for a complete description of read and write modes

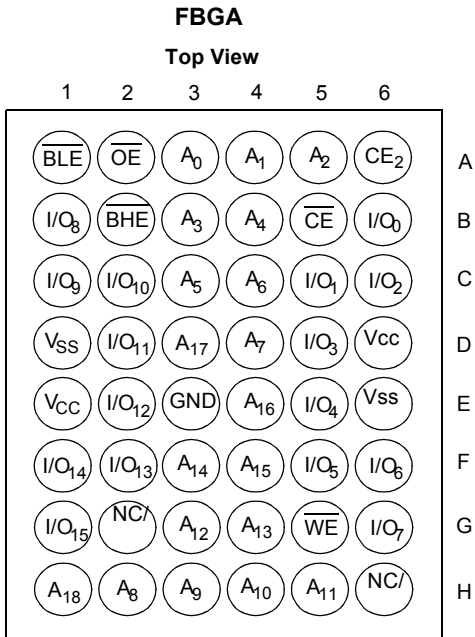
### Logic Block Diagram



**Note:**

1. For best-practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

**Pin Configuration**<sup>[2, 3, 4]</sup>



**Note:**

2. NC "no connect" - not connected internally to the die.
3. DNU pins are to be left floating or tied to V<sub>SS</sub>.
4. Ball G2 and H6 are the expansion pins for the 16Mb and 32Mb density resectively.



**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....-65°C to + 150°C  
 Ambient Temperature with Power Applied.....-55°C to + 85°C  
 Supply Voltage to Ground Potential..... -0.4V to 4.6V

DC Voltage Applied to Outputs in High Z State<sup>[5, 6, 7]</sup> .....-0.2V to 3.3V  
 DC Input Voltage<sup>[5, 6, 7]</sup> .....-0.2V to 3.3V  
 Output Current into Outputs (LOW)..... 20 mA  
 Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)  
 Latch-Up Current .....>200 mA

**Operating Range<sup>[9]</sup>**

Device	Range	Ambient Temperature	V <sub>CC</sub>
CG6258AM	Industrial	-25°C to +85°C	2.70V to 3.30V

**Product Portfolio**

Product	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
					Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
					f = 1MHz		f = f <sub>max</sub>			
Min.	Typ. <sup>[8]</sup>	Max.	Typ. <sup>[8]</sup>	Max.	Typ. <sup>[8]</sup>	Max.	Typ. <sup>[8]</sup>	Max.		
CG6258AM	2.70	3.0	3.30	70	2	4	13	17	55	80

**Notes:**

5. V<sub>IH(MAX)</sub> = V<sub>CC</sub> + 0.5V for pulse durations less than 20ns.
6. V<sub>IL(MIN)</sub> = -0.5V for pulse durations less than 20ns.
7. Overshoot and undershoot specifications are characterized and are not 100% tested.
8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub> (typ) and T<sub>A</sub> = 25C
9. V<sub>CC</sub> must be at minimal operational levels before inputs are turned ON.

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions		CG6258AM-70			Unit
				Min.	Typ. <sup>[8]</sup>	Max.	
V <sub>CC</sub>	Supply Voltage			2.7		3.3	V
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -1.0 mA	V <sub>CC</sub> = 2.70V	2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.0mA	V <sub>CC</sub> = 2.70V			0.4	V
V <sub>IH</sub>	Input HIGH Voltage	V <sub>CC</sub> = 2.7V to 3.3V		0.8*V <sub>CC</sub>		V <sub>CC</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW Voltage	V <sub>CC</sub> = 2.7V to 3.3V (F = 0)		-0.3		0.4	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled		-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	V <sub>CC</sub> = V <sub>CCmax</sub>		13	17	mA
		f = 1 MHz	I <sub>OUT</sub> = 0 mA CMOS levels		2.0	4	mA
I <sub>SB1</sub>	Automatic $\overline{CE}$ Power-Down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ , $V_{IN} \leq 0.2V$ f = f <sub>MAX</sub> (Address and Data Only), f = 0 (OE, WE, BHE and BLE), V <sub>CC</sub> = 3.30V		V <sub>CC</sub> = 3.3V		350	μA
I <sub>SB2</sub>	Automatic $\overline{CE}$ Power-Down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , f = 0, V <sub>CC</sub> = 3.30V		V <sub>CC</sub> = 3.3V	55	80	μA

**Capacitance**<sup>[10]</sup>

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub>	6	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

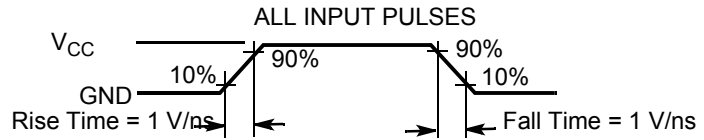
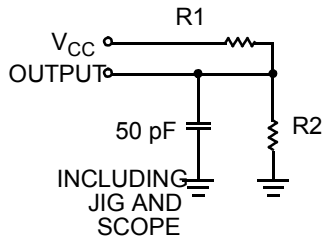
**Thermal Resistance**<sup>[10]</sup>

Description	Test Conditions	Symbol	BGA	Unit
Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	Θ <sub>JA</sub>	55	°C/W
Thermal Resistance (Junction to Case)		Θ <sub>JC</sub>	16	°C/W

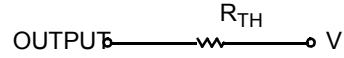
**Note:**

10. Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**



Equivalent to: THÉVENINEQUIVALENT



Parameters	3.0V V <sub>CC</sub>	Unit
R1	1179	Ω
R2	1941	Ω
R <sub>TH</sub>	733	Ω
V <sub>TH</sub>	1.87	V

**Switching Characteristics** Over the Operating Range<sup>[11]</sup>

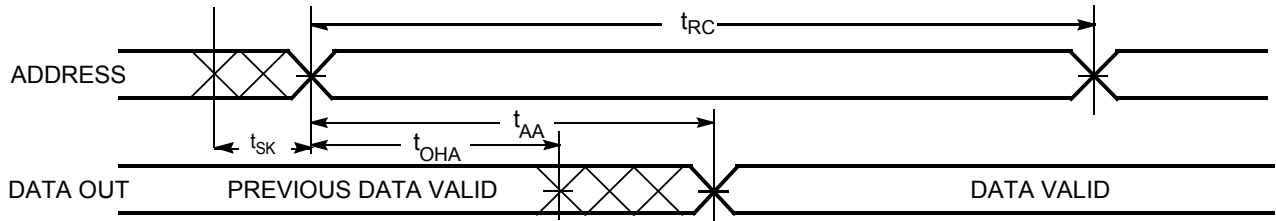
Parameter	Description	70 ns		Unit
		Min.	Max.	
<b>READ CYCLE</b>				
$t_{RC}$	Read Cycle Time	70		ns
$t_{AA}$	Address to Data Valid		70	ns
$t_{OHA}$	Data Hold from Address Change	10		ns
$t_{ACE}$	$\overline{CE}$ LOW and $CE_2$ HIGH to Data Valid		70	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		35	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[12, 14]</sup>	5		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[12, 14]</sup>		25	ns
$t_{LZCE}$	$\overline{CE}$ LOW and $CE_2$ HIGH to Low Z <sup>[12, 14]</sup>	5		ns
$t_{HZCE}$	$\overline{CE}$ HIGH and $CE_2$ LOW to High Z <sup>[12, 14]</sup>		25	ns
$t_{DBE}$	$\overline{BLE}$ / $\overline{BHE}$ LOW to Data Valid		70	ns
$t_{LZBE}$	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low Z <sup>[12, 14]</sup>	5		ns
$t_{HZBE}$	$\overline{BLE}$ / $\overline{BHE}$ HIGH to HIGH Z <sup>[12, 14]</sup>		25	ns
$t_{sk}$	<b>Address Skew</b>		<b>0</b>	<b>ns</b>
<b>WRITE CYCLE<sup>[13]</sup></b>				
$t_{WC}$	Write Cycle Time	70		ns
$t_{SCE}$	$\overline{CE}$ LOW and $CE_2$ HIGH to Write End	60		ns
$t_{AW}$	Address Set-Up to Write End	60		ns
$t_{HA}$	Address Hold from Write End	0		ns
$t_{SA}$	Address Set-Up to Write Start	0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	45		ns
$t_{BW}$	$\overline{BLE}$ / $\overline{BHE}$ LOW to Write End	60		ns
$t_{SD}$	Data Set-Up to Write End	45		ns
$t_{HD}$	Data Hold from Write End	0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High-Z <sup>[12, 14]</sup>		25	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low-Z <sup>[12, 14]</sup>	5		ns

**Notes:**

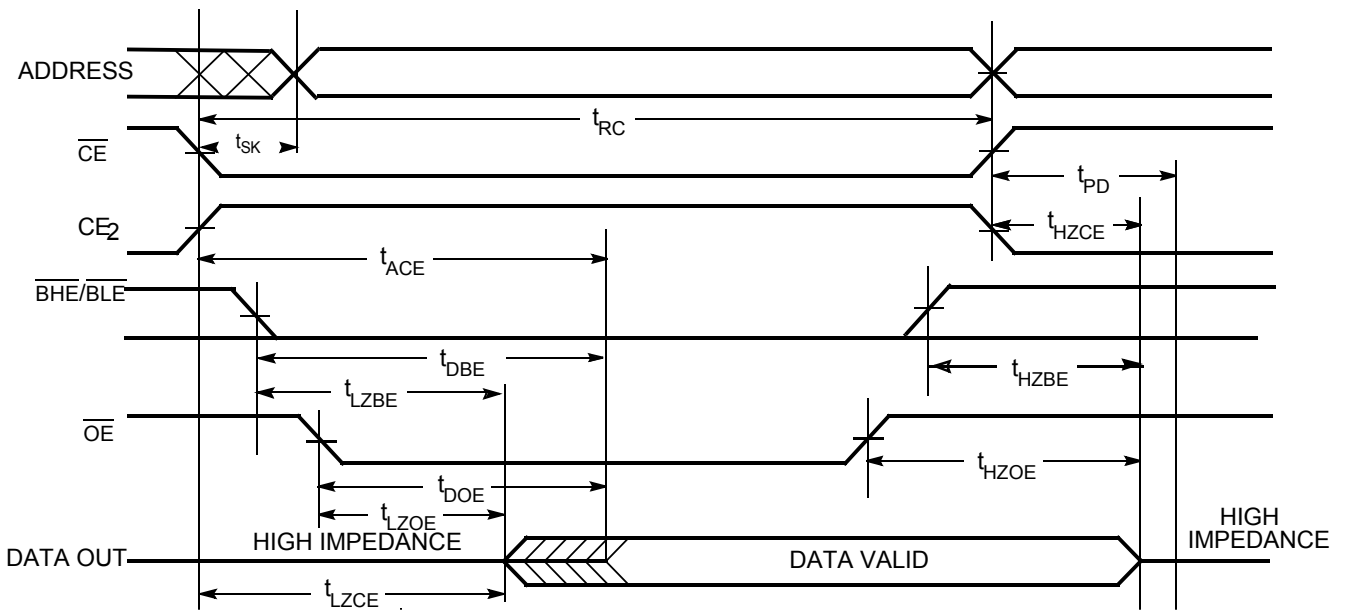
11. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1ns/V, timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the "AC Test Loads and Waveforms" section.
12.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.
13. The internal Write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $CE = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.
14. High-Z and Low-Z parameters are characterized and are not 100% tested.

**Switching Waveforms**

**Read Cycle 1 (Address Transition Controlled)<sup>[15, 16]</sup>**



**Read Cycle 2 ( $\overline{OE}$  Controlled)<sup>[15, 16]</sup>**

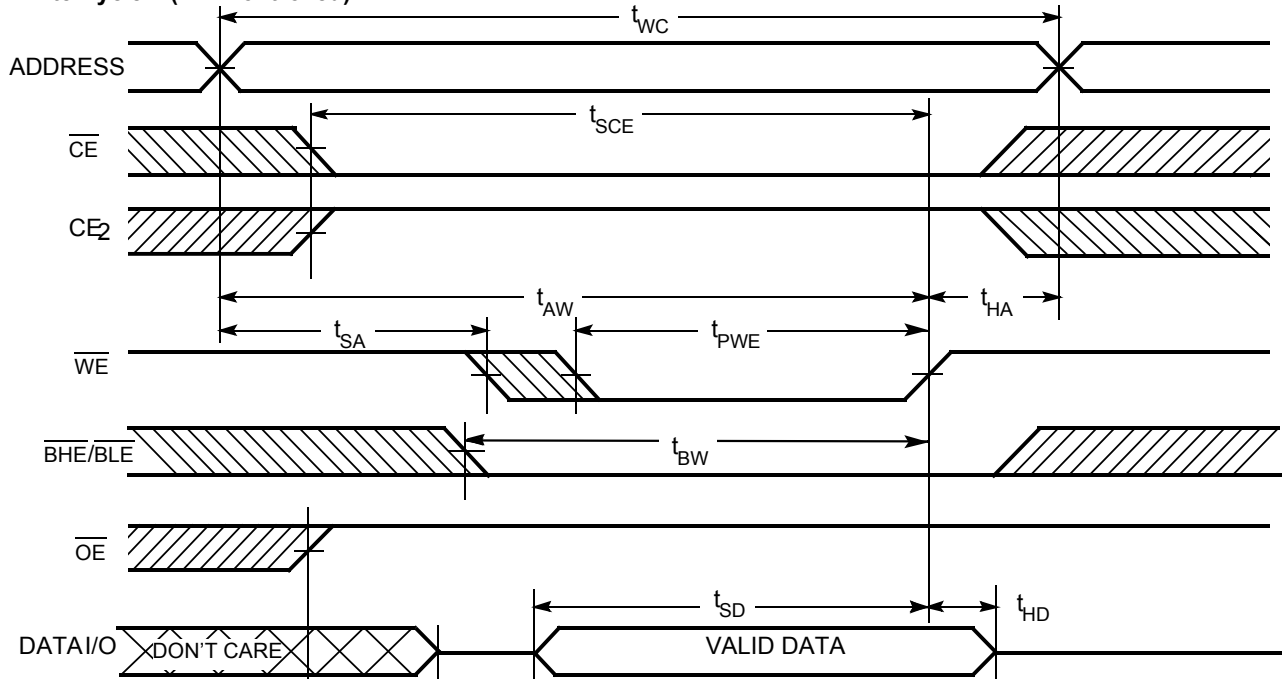


**Note:**

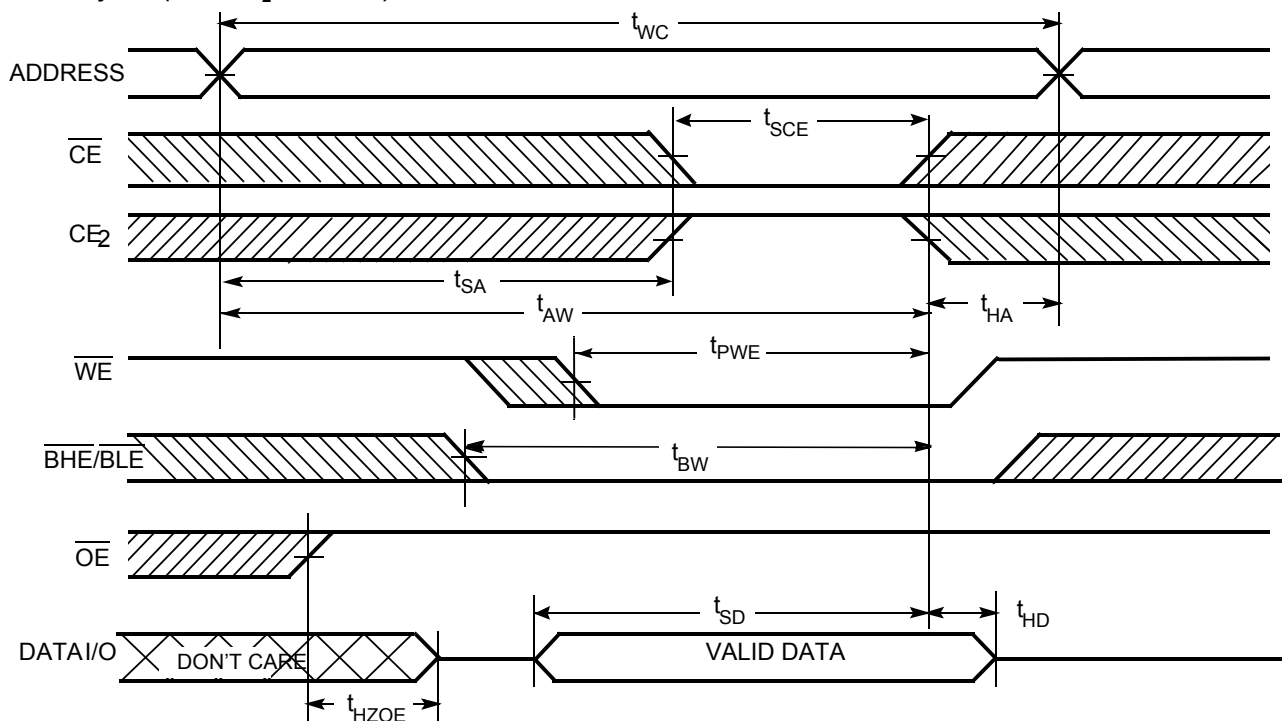
- 15.  $\overline{WE}$  is HIGH for read cycle.
- 16. Addresses should not be toggled after the start of a read cycle

**Switching Waveforms (continued)**

**Write Cycle 1 ( $\overline{WE}$  Controlled)** [13, 14, 17, 18, 19]



**Write Cycle 2 ( $\overline{CE}$  or  $CE_2$  Controlled)** [13, 14, 17, 18, 19]



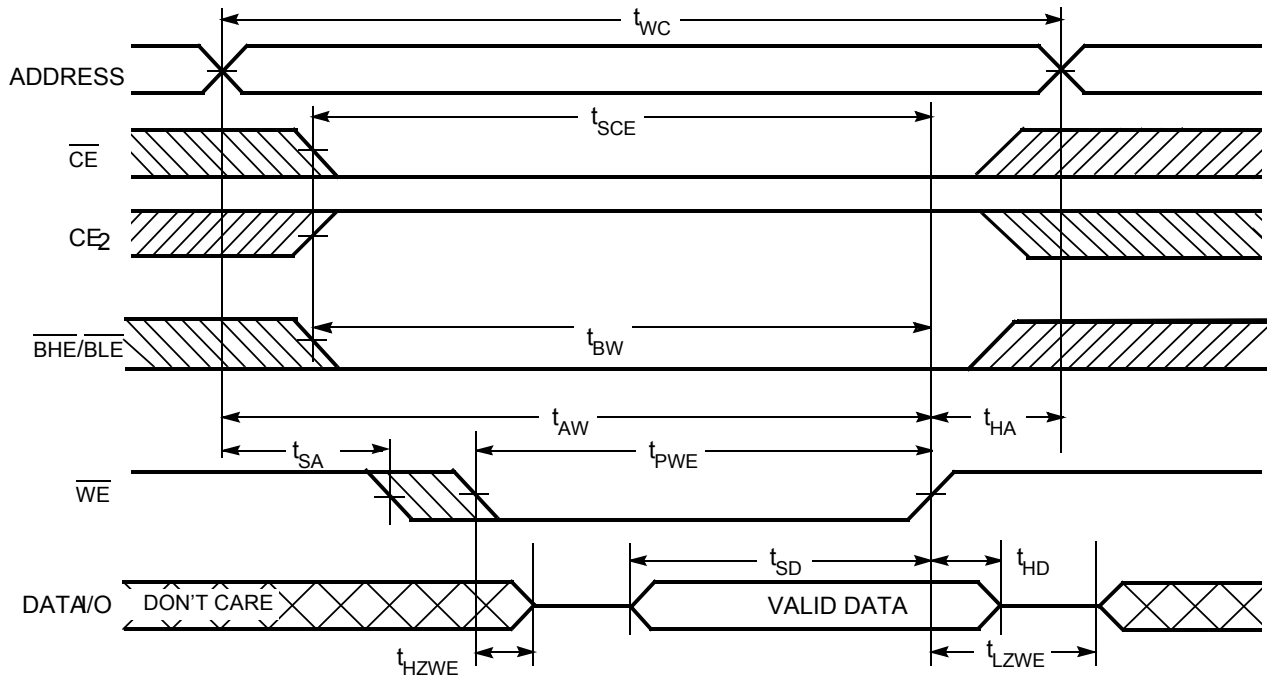
**Notes:**

- 17. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 18. If Chip Enable goes INACTIVE and  $CE_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high-impedance state.
- 19. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

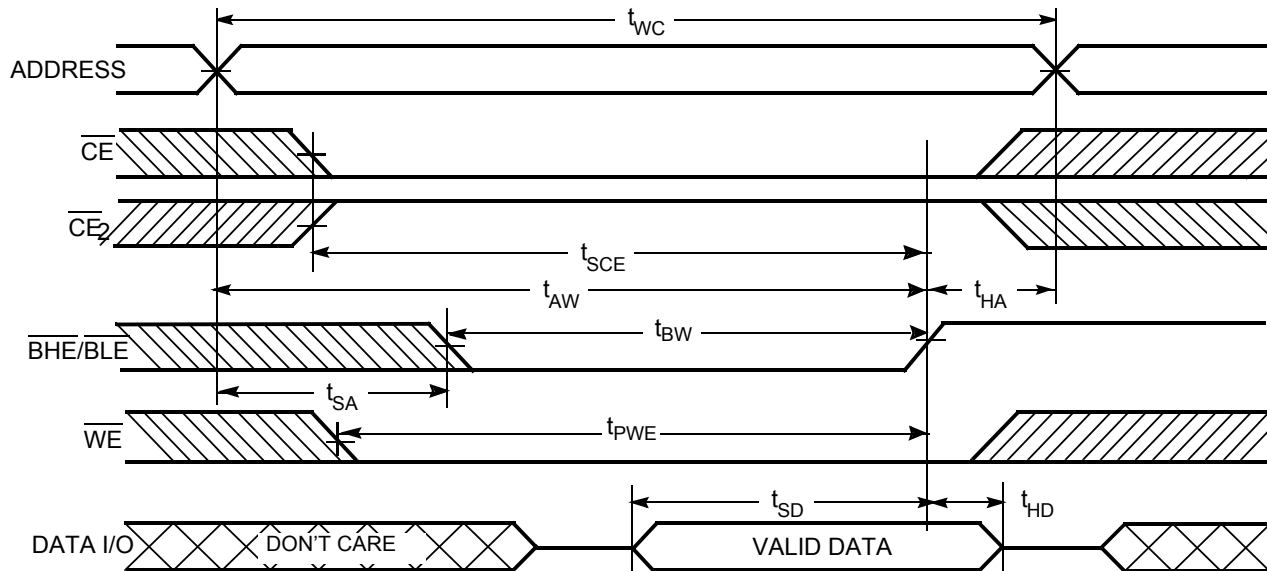


**Switching Waveforms (continued)**

**Write Cycle 3 (WE Controlled, OE LOW)<sup>[18, 19]</sup>**



**Write Cycle 4 (BHE/BLE Controlled, OE LOW)<sup>[18, 19]</sup>**



**Truth Table<sup>[20]</sup>**

CE	CE <sub>2</sub>	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-Down	Standby (I <sub>SB</sub> )
X	L	X	X	X	X	High Z	Deselect/Power-Down	Standby (I <sub>SB</sub> )
X	X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I <sub>SB</sub> )
L	H	H	L	L	L	Data Out (I/O0 – I/O15)	Read	Active (I <sub>CC</sub> )
L	H	H	L	H	L	Data Out (I/O0 – I/O7); High Z (I/O8 – I/O15)	Read	Active (I <sub>CC</sub> )
L	H	H	L	L	H	High Z (I/O0 – I/O7); Data Out (I/O8 – I/O15)	Read	Active (I <sub>CC</sub> )
L	H	H	H	L	H	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	H	H	H	H	L	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	H	H	H	L	L	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	H	L	X	L	L	Data In (I/O0 – I/O15)	Write	Active (I <sub>CC</sub> )
L	H	L	X	H	L	Data In (I/O0 – I/O7); High Z (I/O8 – I/O15)	Write	Active (I <sub>CC</sub> )
L	H	L	X	L	H	High Z (I/O0 – I/O7); Data In (I/O8 – I/O15)	Write	Active (I <sub>CC</sub> )

Note:

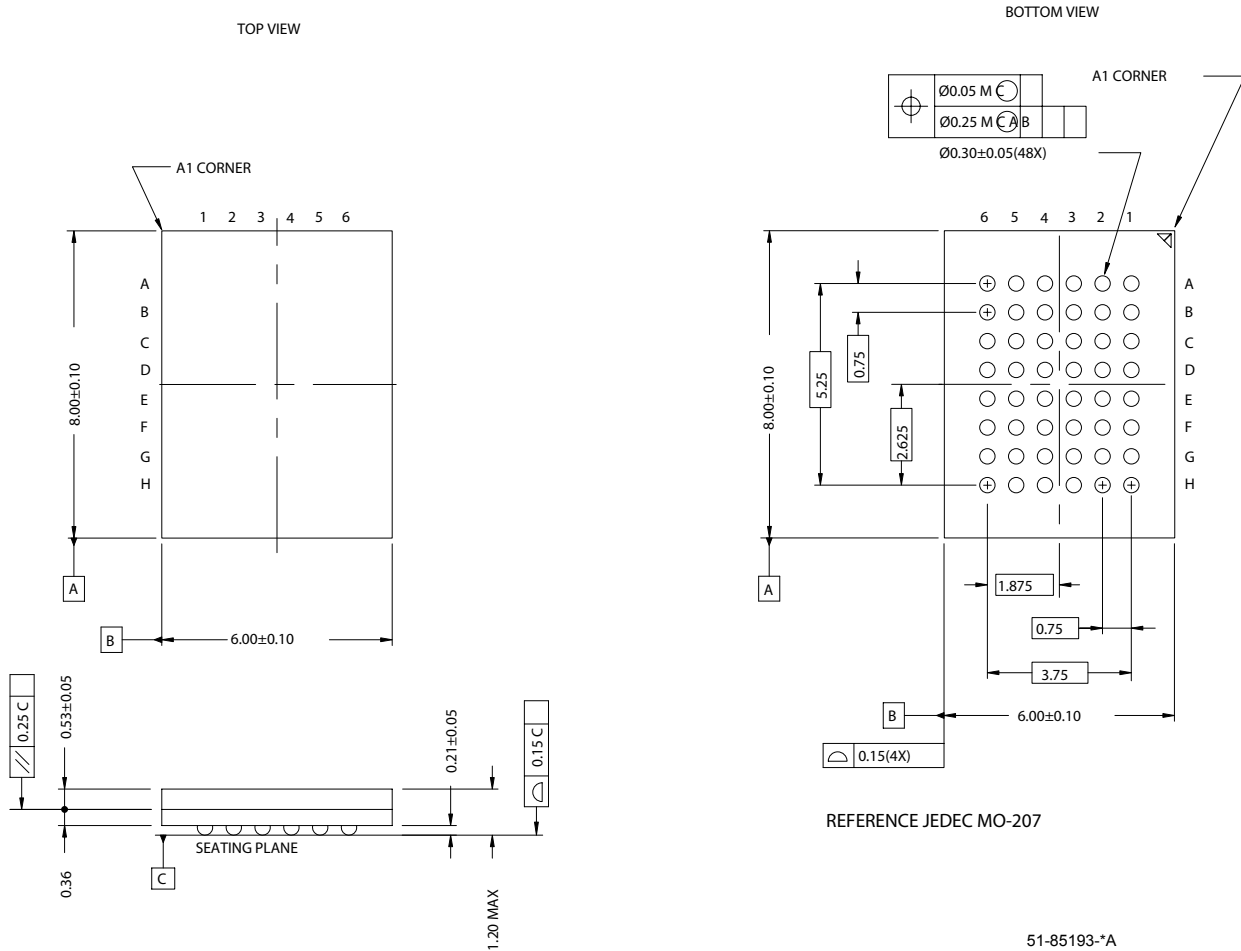
20. H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't Care

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CG6258AM	BA48K	48-ball Fine Pitch BGA (6 mm × 8mm × 1.2 mm)	Industrial

**Package**

**48-Ball (6 mm x 8mm x 1.2 mm) FBGA BA48K**



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## ADVANCE INFORMATION

CG6258AM

<b>Document Title: CG6258AM MoBL3<sup>®</sup> 4Mb (256K x 16) Pseudo Static RAM</b> <b>Document Number: 38-XXXXX</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**		10/16/03	MPR	New Datasheet