Design Example Report

Title	***22 W Triple Output Flyback Converter using DPA424R***
Specification	Input: 28 – 60 VDC Output: 3.3 V / 2 A, 9 V / 0.6 A, 24 V / 0.4 A
Application	Security Camera
Author	Power Integrations Applications Department
Document Number	DER-120
Date	October 26, 2005
Revision	1.0

Summary and Features

- Low parts Count
- High-Efficiency ~80% 48 VDC Input and Full Load
- Good cross-regulation

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Important Note:
This board is designed to be non-isolated. However the outputs are high voltage so please take the necessary safety precautions.

Design Reports contain a power supply design specification, schematic, bill of materials, and transformer documentation. Performance data and typical operation characteristics are included. Typically only a single prototype has been built.

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1 Introduction

This document is an engineering report describing a triple output Flyback converter employing the DPA424R. The input voltage range is 28 to 60 VDC providing a regulated +3.3 V at 2 A and a cross-regulated +9 V @ 0.6 A and +24 V @ 0.4 A.

This document contains the power supply specification, schematic, and bill of materials, transformer documentation, printed circuit layout, and performance data.

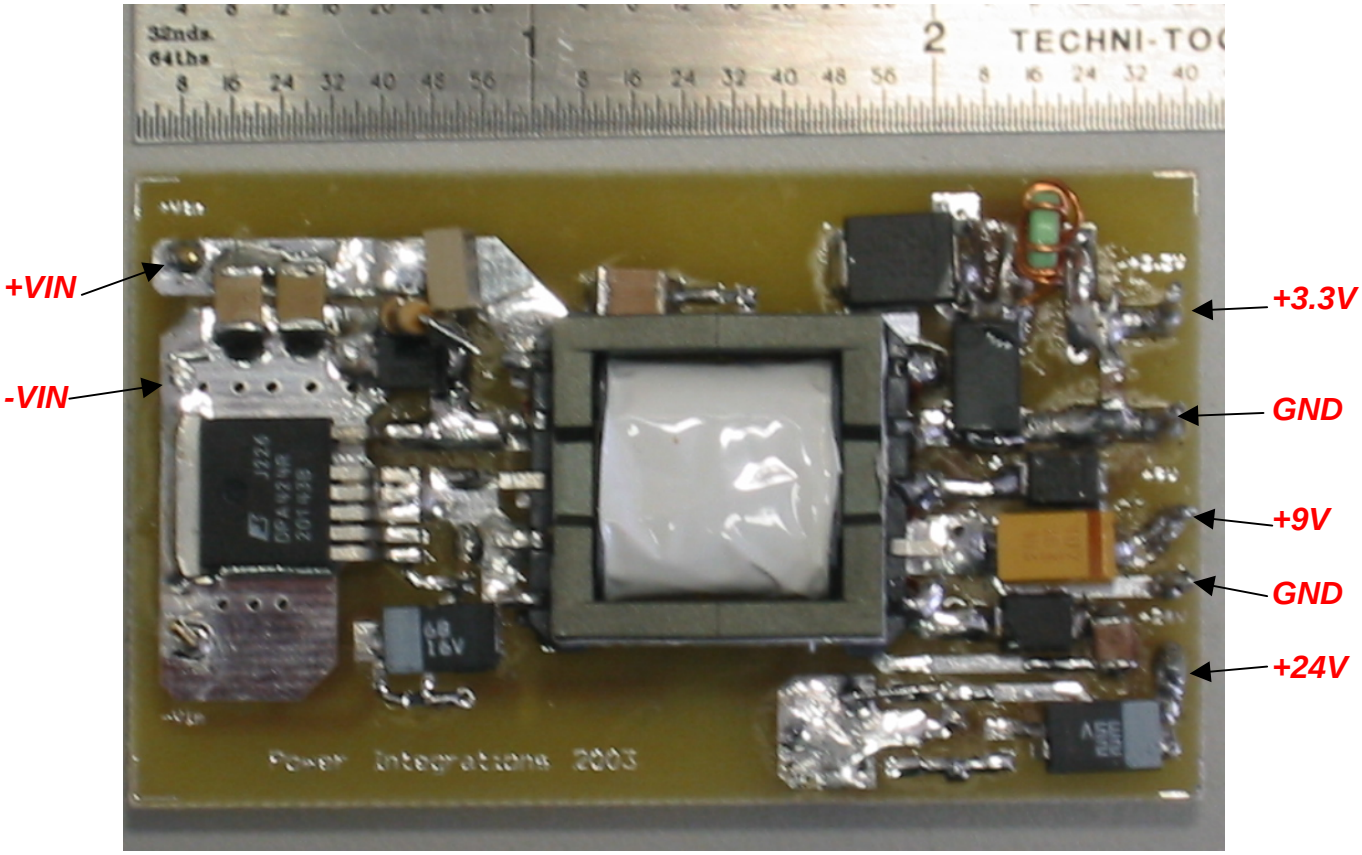

Figure 1 – Populated Circuit Board (Top-side).

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2 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	28	48	60	V_{DC}	
No-load Input Power ($60V_{DC}$)				1.2	W	
Output						
Output Voltage 1	V_{OUT1}	3.135	3.3	3.465	V	± 5%
Output Ripple Voltage 1	$V_{RIPPLE1}$			50	mV	20 MHz Bandwidth
Output Current 1	I_{OUT1}	0.75		2	A	
Output Voltage 2	V_{OUT2}	8.10	9.0	9.90	V	±10%
Output Ripple Voltage 2	$V_{RIPPLE2}$			200	mV	20 MHz Bandwidth
Output Current 2	I_{OUT2}	0.3		0.6	A	
Output Voltage 3	V_{OUT3}	21.6	24.0	26.4	V	±10%
Output Ripple Voltage 3	$V_{RIPPLE3}$			300	mV	20 MHz Bandwidth
Output Current 3	I_{OUT3}	0.1		0.4	A	
Total Output Power						
Continuous Output Power	P_{OUT}	7.6		21.6	W	
Peak Output Power	P_{OUT_PEAK}				W	
Efficiency	η		80		%	Measured at Max. P_{OUT}, 25 °C
Ambient Temperature	T_{AMB}	0		40	°C	Free convection, Sea level

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3 Schematic

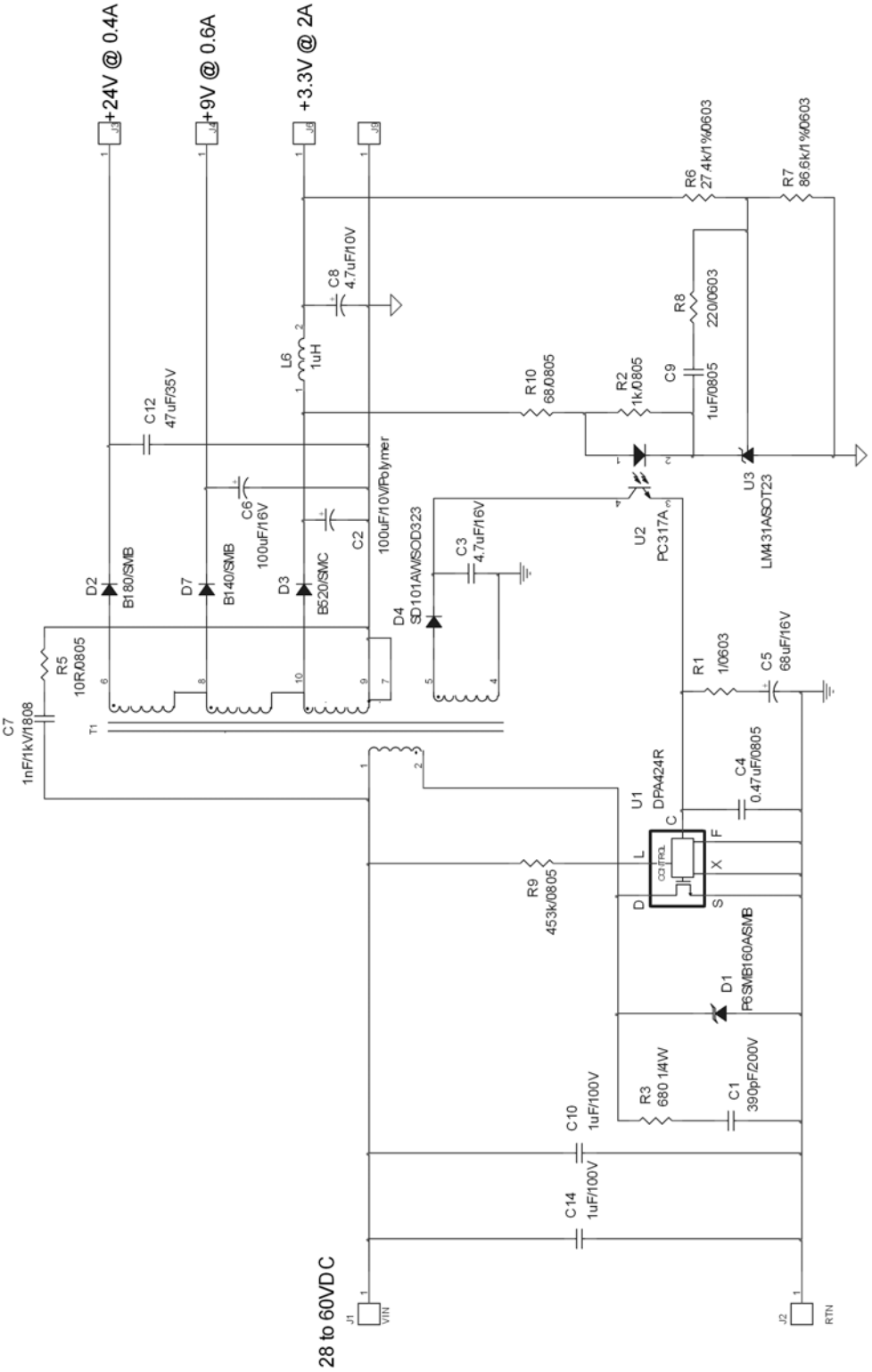

Figure 2 – Schematic.

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4 Circuit Description

4.1 Input EMI filtering

Figure 1 shows a single-ended Flyback converter using the DPA424R. The circuit is designed for an input range of 28 V to 60 V providing three isolated outputs at +3.3 V, +9 V and +24 V at 2 A, 0.6 A and 0.4 A respectively. C10 and C14 bypass the DC rail. The DC rail is applied to the primary winding of T1. The other side of the transformer primary is driven by the integrated MOSFET in U1. VR1 clamps the U1 drain leakage spikes. C1 and R3 dampen the drain-source voltage ringing.

R9 is used to set the low line turn-on threshold to approximately 23 V, and also sets the over-voltage shutdown level to approximately 61 V. C4 bypasses the U1 control pin, and provides the peak current necessary for driving the ***DPA-Switch*** internal MOSFET. C5 has three functions. It provides the energy required by U1 during startup, sets the auto-restart frequency during fault conditions, and also reduces the gain of U1 as a function of frequency. R1 adds a zero to stabilize the power supply control loop.

4.2 Output Rectification

The output of T1 is rectified and filtered by D3 (D7, D2) and C2 (C6, C12). L6 and C8 provide additional high frequency filtering.

An auxiliary Flyback winding on T1 powers U1 during normal operation. This winding delivers energy during the off time of U1, with an output voltage proportional to the supply output voltage. The turns-ratio of T1 sets the output voltage of the auxiliary winding to approximately 12 V. D4 and C8 rectify and filter the auxiliary winding output.

4.3 Output Feedback

R6 and R7 divide down the supply output voltage and apply it to the reference pin of error amplifier U3. C9 and R8 roll off the gain of U3. U3 drives the opto-coupler LED of U2 through resistor R10 to provide feedback information to the CONTROL pin of U1. The opto-coupler phototransistor output also provides power to U1 during normal operating conditions. R2 provides bias current to U3.

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5 PCB Layout

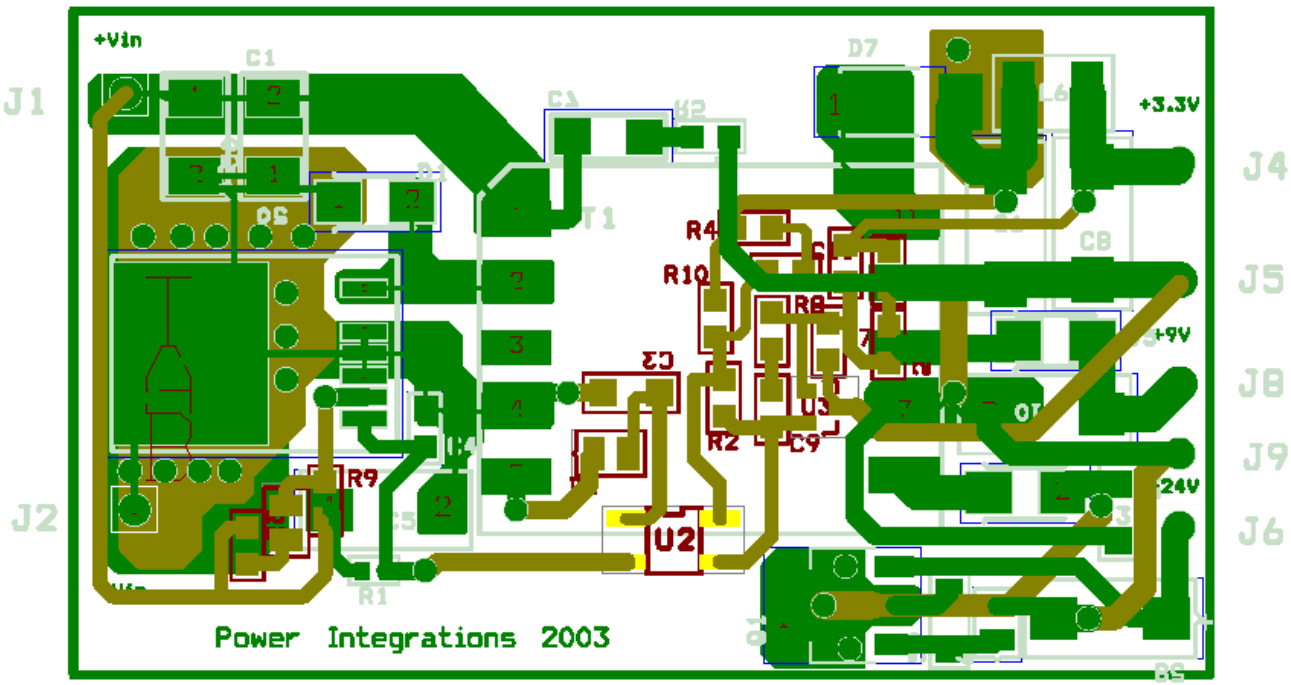

Figure 3 – Printed Circuit Layout.

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6 Bill Of Materials

6.1 Triple Output Flyback Converter

Item	Qty	Ref	Description	P/N	Manufacturer
1	1	C1	390pF/200V	C1210C391K2GAC	Kemet
2	1	C2	100uF/10V/Polymer	EEUFUD0J101RX	Panasonic
3	1	C3	4.7uF/16V	ECST1CY475R	Panasonic
4	1	C4	0.47uF/0805		
5	1	C5	68uF/16V	ECST1CD686R	Panasonic
6	1	C6	100uF/16V	T494D107(1)016AS	Kemet
7	1	C7	1nF/1kV/1812	18122R102KEBB0D	Yageo
8	1	C8	4.7uF/10V	ECST1AY475R	Panasonic
9	1	C9	1uF/0805		
10	1	C10	1uF/100V	C4532X7R2A105M	TDK
11	1	C12	4.7uF/10V	C3216X5R1A475K	TDK
12	1	C14	1uF/100V	C4532X7R2A105M	TDK
13	1	D1	160V TVS	P6SMB160A/SMB	On Semiconductor
14	1	D2	1A/80V Schottky	B180/SMB	Diodes, Inc
15	1	D3	5A/20V Schottky	B520/SMC	Diodes, Inc
16	1	D4	Small Signal Diode	SD101AW/SOD323	Diodes, Inc
17	1	D7	1A/40V Schottky	B140/SMB	Diodes, Inc
18	1	L6	1uH		
19	1	R1	1/0603		
20	1	R2	1k/0805		
21	1	R3	680 1/4W		
22	1	R5	10R/0805		
23	1	R6	27.4k/1%/0603		
24	1	R7	86.6k/1%/0603		
25	1	R8	220/0603		
26	1	R9	453k/0805		
27	1	R10	68/0805		
28	1	T1	Custom Flyback EFD20		
29	1	U1	PWM + MOSFET	DPA424R	Power Integrations
30	1	U2	Opto-coupler	PC317A	Sharp
31	1	U3	Prec. Shunt Regulator	LM431A/SOT23	National Semiconductor

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7 Transformer Specification

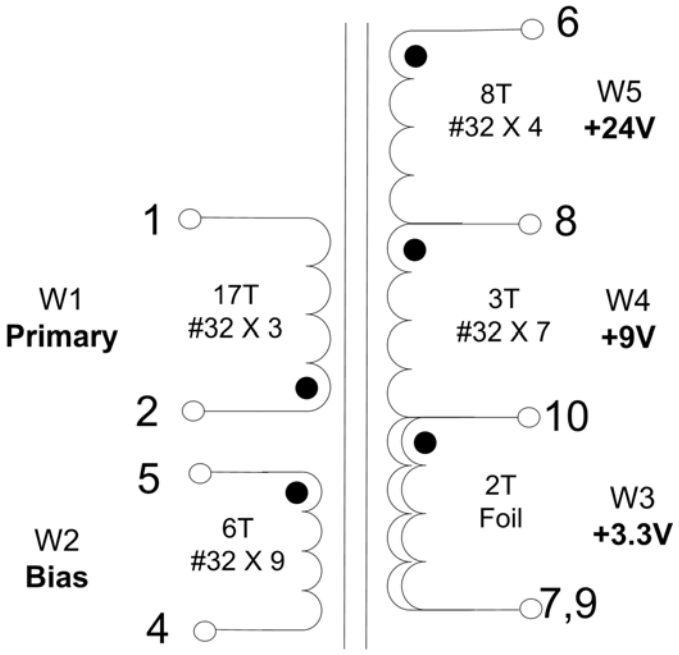

Figure 4 – Transformer Diagram

7.1 Electrical Specifications

Electrical Strength	1 second, from Pins 1-5 to Pins 6-10	1000 VDC
Creepage	Between Pins 1-5 and Pins 6-10	N/A
Primary Inductance	Pins 1,2, all other windings open, measured at 400KHz, 400mVRMS	40 μH, ±10 %
Resonant Frequency	Pins 1,2, all other windings open	5.0 MHz (Min.)
Primary Leakage Inductance	Pins 1,2, with Pins 6-10 shorted, measured at 400KHz, 400mVRMS	0.75 μH (Max.)

7.2 Materials

Item	Description
[1]	Core: EFD20/3F3 or equivalent gap for A_L of 133 nH/T^2
[2]	Bobbin: 10 pin surface mount
[3]	Magnet Wire: #32 AWG Double Coated
[4]	Foil
[5]	Tape, Polyester
[6]	Varnish

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7.3 Transformer Build Diagram

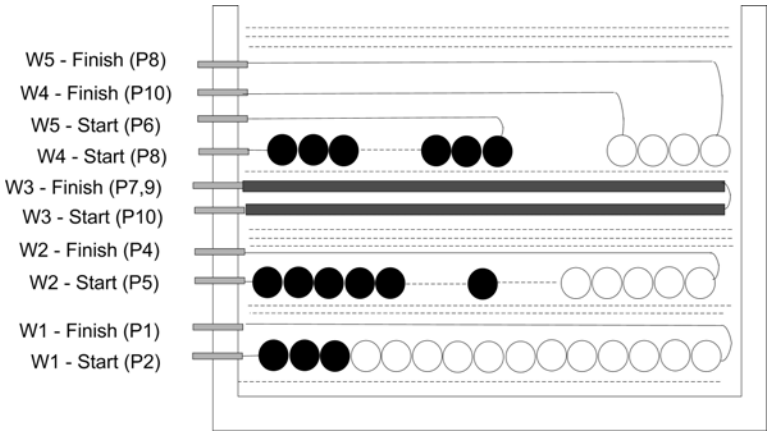

Figure 5 – Transformer Cross-Section

7.4 Transformer Construction

Primary	Start at Pin 2. Wind 17 trifilar turns of item [3] uniformly on a single layer. Finish on pin 1.
Basic Insulation	Use one layer of item [5] for basic insulation.
Bias Winding	Start at Pin 5. Wind 6 turns of 9 strands of item [3] uniformly on a single layer. Finish on Pin 4.
Insulation	Use 3 layers of item [5] for basic insulation.
+3.3 V Winding	Prepare cuffed foil assembly. Start at Pin 10. Wind 2 turns of item [4]. Finish on pin 7 and 9.
Basic Insulation	Use one layer of item [5] for basic insulation.
+9 V & +12 V Windings	Wind +9 V and +12 V windings simultaneously and uniformly on a single layer. Start +9 V winding on pin 8 with 7 strands on item [3] and start +12 V winding on pin 6 with a quadfilar item [3] make 3 turns and finish +9V windings to pin 10. Continue +12 v windings an additional 5 turns and finish on pin 8.
Outer Wrap	Wrap windings with 3 layers of tape [item [5].
Final Assembly	Assemble and secure core halves. Dip varnish cores (item [6]). Do not impregnate

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8 Transformer Spreadsheets

A	B	D	F	G	I
DPASwitch_Flyback_Rev_1e_090302; Copyright Power Integrations Inc. 2002	INPUT	INFO	OUTPUT	UNITS	DPASwitch_Flyback_090302 - Continuous/Discontinuous mode Spreadsheet. Copyright 2002 Power Integrations
ENTER APPLICATION VARIABLES					h DPA
VDCMIN	28			Volts	Minimum DC Input Voltage
VDCMAX	60			Volts	Maximum DC Input Voltage
VO	3.3			Volts	Output Voltage
PO	22			Watts	Output Power
n	0.86				Efficiency Estimate
Z			0.7		Loss Allocation Factor, (0.7 Recommended)
VB	15			Volts	Bias Voltage
UV AND OV PARAMETERS					
		min	max		
VUVOFF		22.8	25.1	Volts	Minimum undervoltage On-Off threshold
VUVON		24.4	26.2	Volts	Maximum undervoltage Off-On threshold (turn-on)
VOVON		55.9	-	Volts	Minimum overvoltage Off-On threshold
VOVOFF			70.5	Volts	Maximum overvoltage On-Off threshold (turn-off)
RL			456.6	k-Ohms	Line Sense Resistor
ENTER DPASWITCH VARIABLES					
DPASWITCH	**dpa424**			*16VDC*	*36VDC*
Chosen Device	*DPA424*		*Power Out*	*15.5W*	*35W*
ILIMITMAX	*2.32*	*2.68*		Amps	From DPASWITCH Data Sheet
Frequency	*f*				Enter 'F' for fS = 400KHz and 'L' for fS = 300KHz
fS	400000			Hertz	DPASWITCH Switching Frequency
VOR	**33**		**33**	Volts	Reflected Output Voltage
KI	1.00		1		Current Limit Reduction Factor
ILIMITEXT			2.320	Amps	Minimum External Current limit
RX			-	k-Ohms	Resistor from X pin to source to set external current limit
VDS	2.5			Volts	DPASWITCH on-state Drain to Source Voltage
VD	0.5			Volts	Output Winding Diode Forward Voltage Drop
VDB	0.7			Volts	Bias Winding Diode Forward Voltage Drop
KRP/KDP	**0.45**				Ripple to Peak Current Ratio (0.2 < KRP < 1.0 : 1.0< KDP<6.0)
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**efd20**				
Core Manuf					
Bobbin Manuf					
Core		*EFD20*		*P/N:*	*EFD20-3F3-Exxx-xx*
Bobbin		*EFD20_Bobbin*		*P/N:*	*0*
AE			0.31	cm^2	Core Effective Cross Sectional Area
LE			4.7	cm	Core Effective Path Length
AL			1200	nH/T^2	Ungapped Core Effective Inductance
BW			13.5	mm	Bobbin Physical Winding Width
M	0			mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	**1**				Number of Primary Layers
NS	**2**				Number of Secondary Turns
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.56		Maximum Duty Cycle
IAVG			0.91	Amps	Average Primary Current
IP		***Warning***	2.09	Amps	!!!!!!!!!! REDUCE Ip< KI*0.9*2.32 (increase VOR, decrease KDP,larger DPASWITCH)
IR			0.94	Amps	Primary Ripple Current
IRMS			1.23	Amps	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			40	uHenries	Primary Inductance
NP			17		Primary Winding Number of Turns
NB			8		Bias Winding Number of Turns
ALG			133	nH/T^2	Gapped Core Effective Inductance
BP			1733	Gauss	Peak Flux density during transients (Limit to 4000 Gauss)
BM		***Warning***	1561	Gauss	Peak Flux density<2000 Gauss, A smaller core may be used
BAC			351	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1448		Relative Permeability of Ungapped Core
LG			**0.26**	mm	Gap Length (Lg >> 0.051 mm)
BWE			13.5	mm	Effective Bobbin Width
TRANSFORMER SECONDARY DESIGN PARAMETERS					
ISP			18.15	Amps	Peak Secondary Current
ISRMS			9.42	Amps	Secondary RMS Current
IO			6.67	Amps	Power Supply Output Current
IRIPPLE			6.65	Amps	Output Capacitor RMS Ripple Current
VOLTAGE STRESS PARAMETERS					
VDRAIN			149	Volts	Maximum Drain Voltage (Includes Effect of Leakage Inductance)
PIVS			10	Volts	Output Rectifier Maximum Peak Inverse Voltage
PIVB			44	Volts	Bias Rectifier Maximum Peak Inverse Voltage
ADDITIONAL OUTPUTS					
V_OUT2	9.0000			Volts	Auxiliary Output Voltage
VD_OUT2	0.5000			Volts	Auxiliary Diode Forward Voltage Drop
N_OUT2			5.00		Auxiliary Number of Turns
PIV_OUT2			26	Volts	Auxiliary Rectifier Maximum Peak Inverse Voltage
V_OUT3	24			Volts	Auxiliary Output Voltage
VD_OUT3	0.75			Volts	Auxiliary Diode Forward Voltage Drop
N_OUT3			13.03		Auxiliary Number of Turns

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9 Performance Data

All measurements performed at room temperature.

9.1 Cross Regulation Matrix

Input Voltage **28**

		LOAD	*Regulation*		*LOAD*	*Regulation*		*LOAD*	*Regulation*
+3.3V	3.39	0	102.7%	3.34	0.75	101.2%	3.35	0.75	101.5%
+9V	9.35	0	103.9%	9.1	0.3	101.1%	9.06	0.3	100.7%
+24V	24.32	0	101.3%	24.22	0.1	100.9%	23.83	0.4	99.3%
Input Current	0.018		η	0.353		η	0.667		η
Input Power	0.504		0.000%	9.884		77.469%	18.676		79.045%
+3.3V	3.35	0.75	101.5%	3.35	0.75	101.5%	3.33	2	100.9%
+9V	8.94	0.6	99.3%	8.89	0.6	98.8%	9.7	0.3	107.8%
+24V	24.14	0.1	100.6%	23.74	0.4	98.9%	25.89	0.1	107.9%
Input Current	0.466		η	0.791		η	0.571		η
Input Power	13.048		78.866%	22.148		78.303%	15.988		76.051%
+3.3V	3.35	2	101.5%	3.33	2	100.9%	3.34	2	101.2%
+9V	9.66	0.3	107.3%	9.51	0.6	105.7%	9.48	0.6	105.3%
+24V	25.44	0.4	106.0%	25.81	0.1	107.5%	25.36	0.4	105.7%
Input Current	0.929		η	0.695		η	1.067		η
Input Power	26.012		76.019%	19.46		76.809%	29.876		75.351%

Input Voltage **48**

		LOAD	*Regulation*		*LOAD*	*Regulation*		*LOAD*	*Regulation*
+3.3V	3.43	0	103.9%	3.38	0.75	102.4%	3.37	0.75	102.1%
+9V	10.05	0	111.7%	9.11	0.3	101.2%	9.01	0.3	100.1%
+24V	26.16	0	109.0%	24.18	0.1	100.8%	23.52	0.4	98.0%
Input Current	0.019		η	0.215		η	0.391		η
Input Power	0.912		0.000%	10.32		74.477%	18.768		77.997%
+3.3V	3.37	0.75	102.1%	3.37	0.75	102.1%	3.35	2	101.5%
+9V	8.93	0.6	99.2%	8.82	0.6	98.0%	9.48	0.3	105.3%
+24V	24.01	0.1	100.0%	23.45	0.4	97.7%	25.27	0.1	105.3%
Input Current	0.277		η	0.452		η	0.333		η
Input Power	13.296		77.365%	21.696		79.275%	15.984		75.519%
+3.3V	3.36	2	101.8%	3.36	2	101.8%	3.36	2	101.8%
+9V	9.4	0.3	104.4%	9.32	0.6	103.6%	9.29	0.6	103.2%
+24V	24.7	0.4	102.9%	25.16	0.1	104.8%	24.67	0.4	102.8%
Input Current	0.514		η	0.397		η	0.581		η
Input Power	24.672		78.713%	19.056		77.813%	27.888		79.468%

Input Voltage **60**

		LOAD	*Regulation*		*LOAD*	*Regulation*		*LOAD*	*Regulation*
+3.3V	3.4	0	103.0%	3.36	0.75	101.8%	3.37	0.75	102.1%
+9V	10.13	0	112.6%	9.09	0.3	101.0%	9.02	0.3	100.2%
+24V	26.27	0	109.5%	24.17	0.1	100.7%	23.7	0.4	98.8%
Input Current	0.018		η	0.167		η	0.3		η
Input Power	1.08		0.000%	10.02		76.487%	18		81.742%
+3.3V	3.36	0.75	101.8%	3.36	0.75	101.8%	3.35	2	101.5%
+9V	8.93	0.6	99.2%	8.92	0.6	99.1%	9.49	0.3	105.4%
+24V	24.01	0.1	100.0%	23.64	0.4	98.5%	25.28	0.1	105.3%
Input Current	0.219		η	0.349		η	0.26		η
Input Power	13.14		78.227%	20.94		82.751%	15.6		77.404%
+3.3V	3.35	2	101.5%	3.35	2	101.5%	3.36	2	101.8%
+9V	9.46	0.3	105.1%	9.26	0.6	102.9%	9.23	0.6	102.6%
+24V	23.72	0.4	98.8%	24.99	0.1	104.1%	24.48	0.4	102.0%
Input Current	0.396		η	0.306		η	0.442		η
Input Power	23.76		80.076%	18.36		80.365%	26.52		83.145%

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9.2 Regulation

9.2.1 LINE

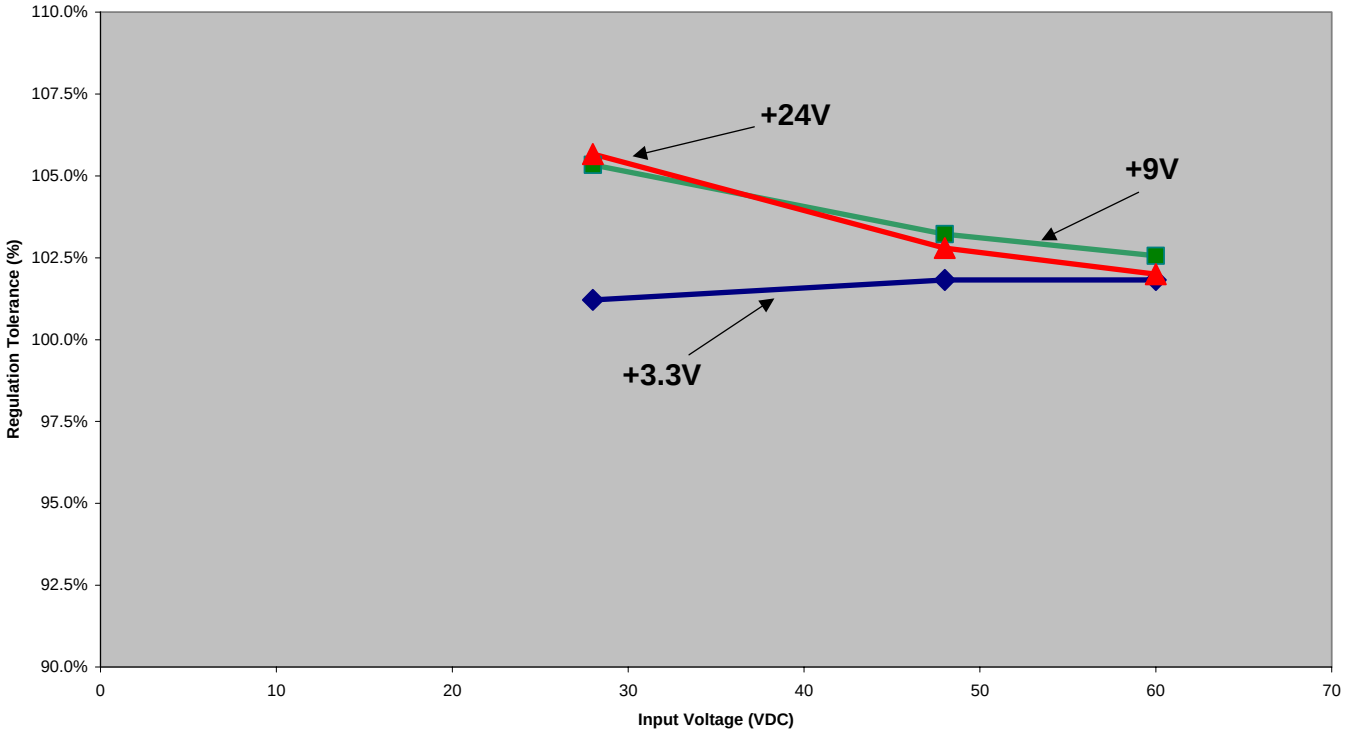

Figure 6 – Line Regulation, Full Load

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9.2.2 LOAD

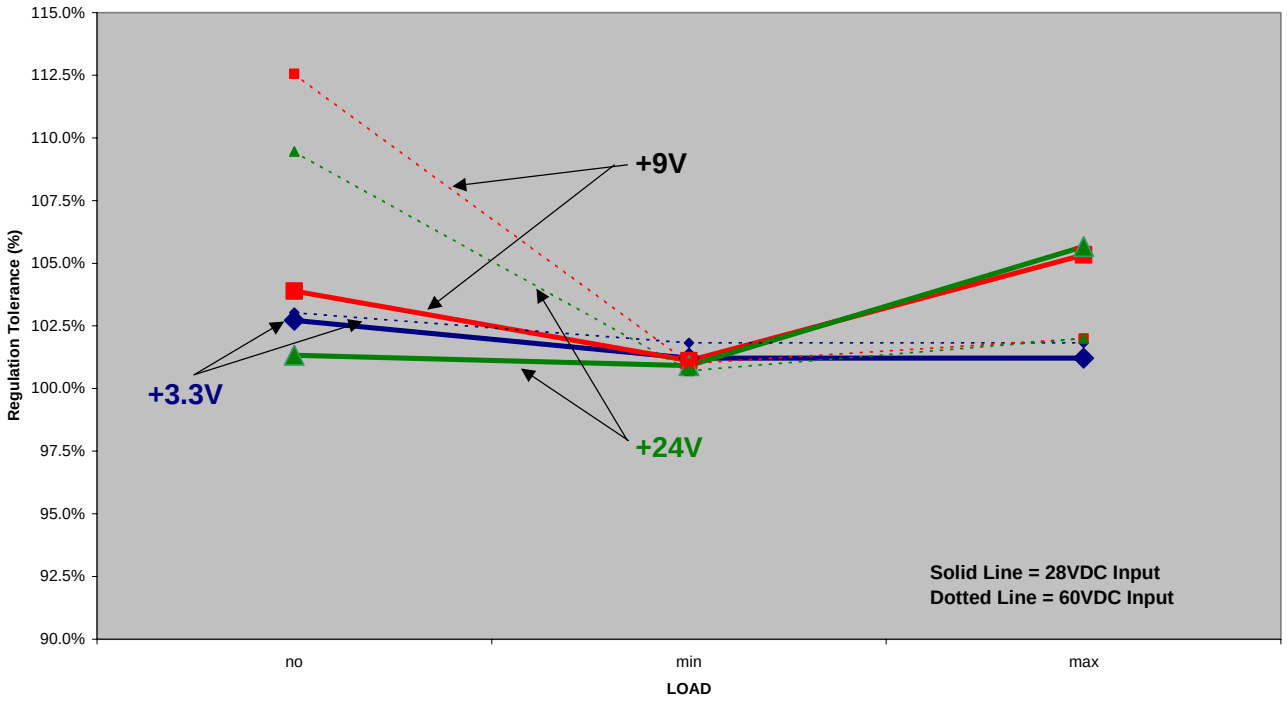

Figure 7 – Load Regulation, 28 V and 60 VDC Input

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10 Waveforms

10.1 Drain Voltage, Normal Operation

Figure 8 – 48 VDC, No Load.
Upper: I_{DRAIN}, 1 A/div
Lower: V_{DRAIN}, 50 V/div, 0.5 µs / div

Figure 9 – 48 VDC Input, Full Load.
Upper: I_{DRAIN}, 1 A/div
Lower: V_{DRAIN}, 50 V/div, 0.5 µs / div

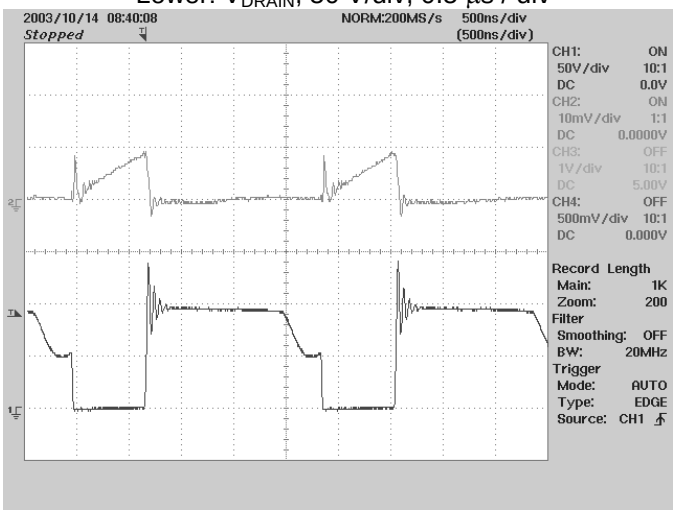

Figure 10 – 48 VDC, Minimum Load.
Upper: I_{DRAIN}, 1 A/div
Lower: V_{DRAIN}, 50 V/div, 0.5 µs / div

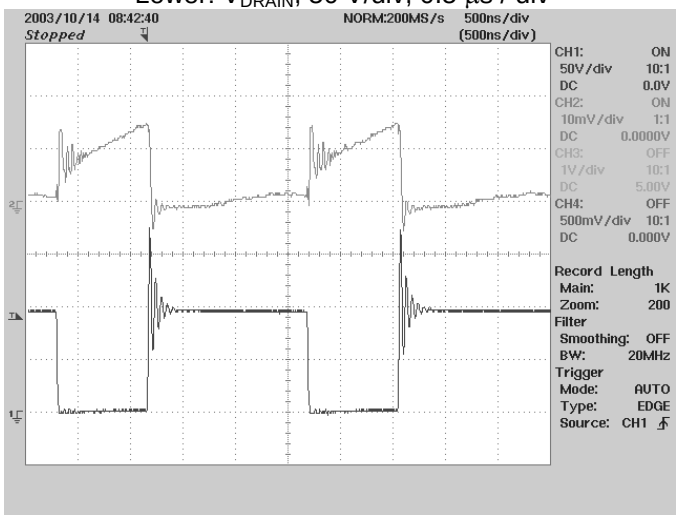

Figure 11 – 60 VDC Input, Full Load.
Upper: I_{DRAIN}, 1 A/div
Lower: V_{DRAIN}, 50 V/div, 0.5 µs / div

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10.2 Output Voltage Start-up Profile

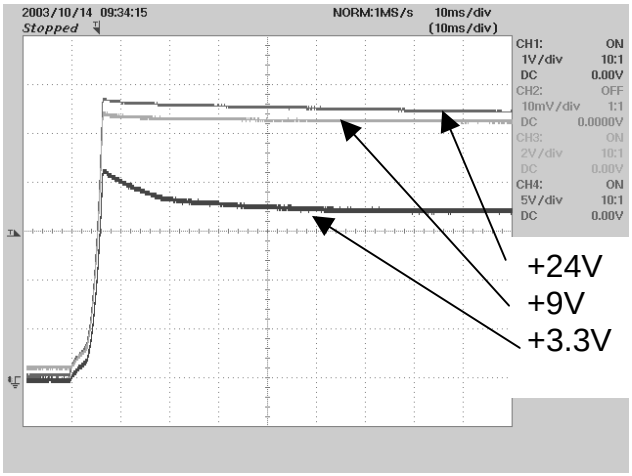

Figure 12 – Start-up Profile, 48 VDC No Load
T: 10msec/div

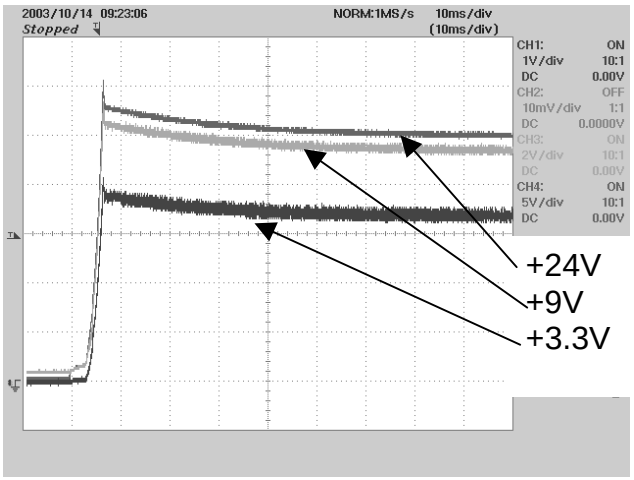

Figure 13 – Start-up Profile, 48 VDC Full Load
T: 10msec/div

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10.3 Load Transient Response (0.75 A to 2 A Load Step)

In the figures shown below, signal averaging was used to better enable viewing the load transient response. The oscilloscope was triggered using the load current step as a trigger source. Since the output switching and line frequency occur essentially at random with respect to the load transient, contributions to the output ripple from these sources will average out, leaving the contribution only from the load step response.
+9 V and +24 V Loads were set to maximum.

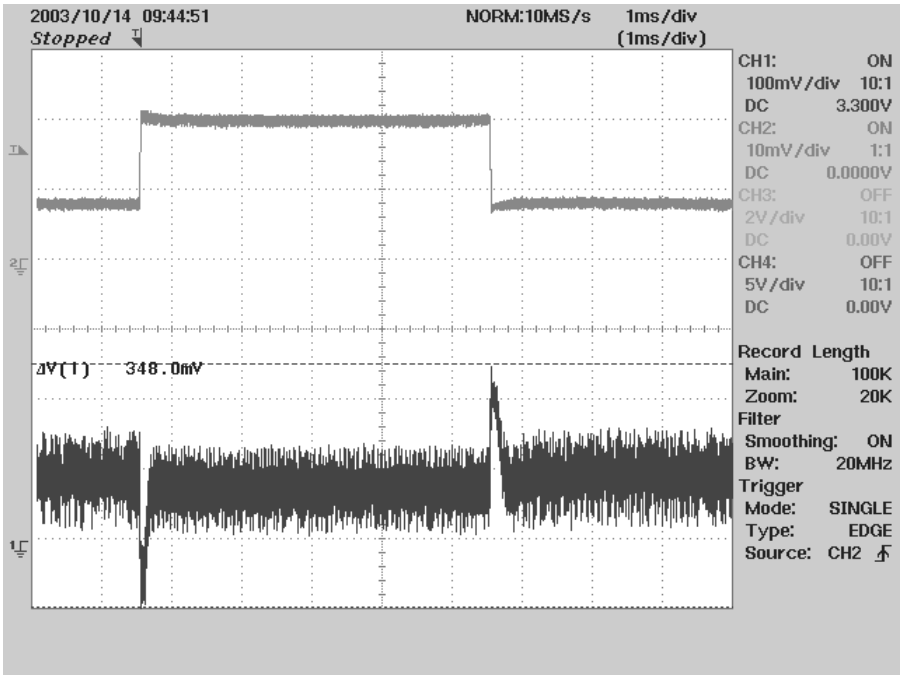

Figure 14 – Transient Response
Top: Load Current; 1 A/div.
Bottom: +3.3 V Output
100 mV, 1ms/div.

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10.4 Output Ripple Measurements

10.4.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in Figure 15 and Figure 16.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1.0 μF/50 V aluminum electrolytic. ***The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).***

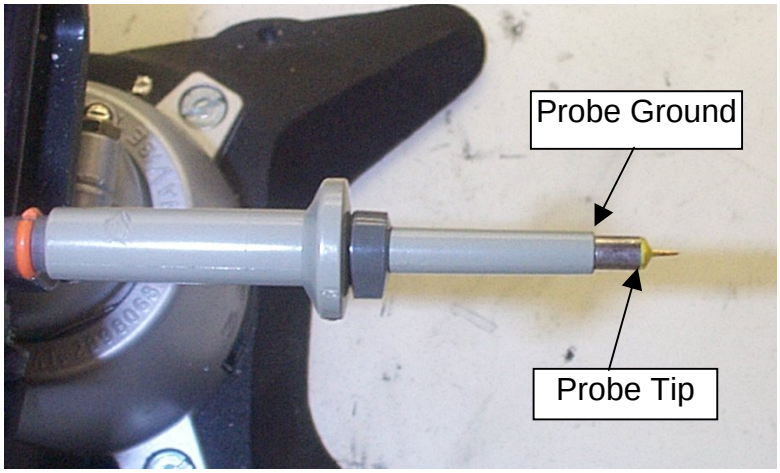

Figure 15 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

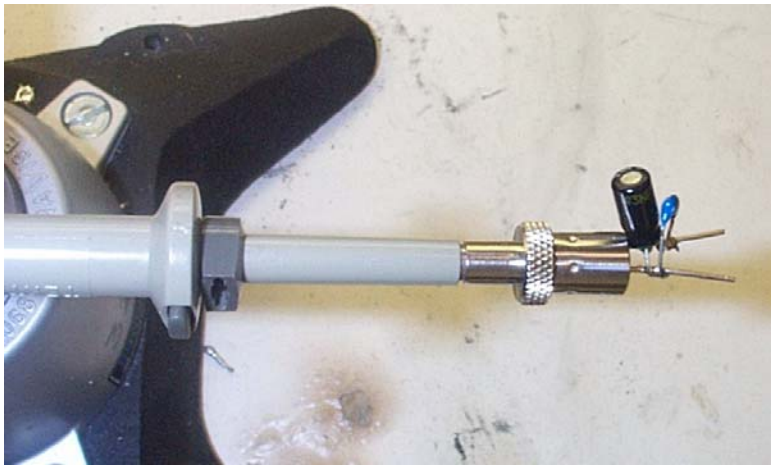

Figure 16 – Oscilloscope Probe with Probe Master 5125BA BNC Adapter. (Modified with wires for probe ground for ripple measurement, and two parallel decoupling capacitors added)

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10.4.2 Measurement Results at 48 VDC

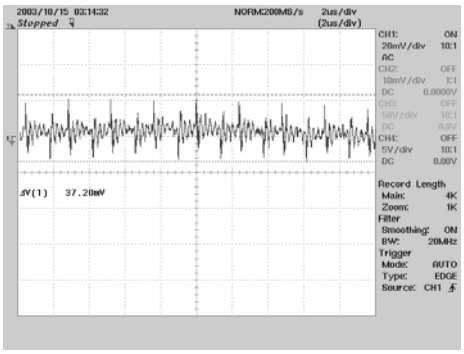

Figure 17 – +3.3 V Ripple, Full Load, 20mV/div; T: 2usec/div

38mV p-p

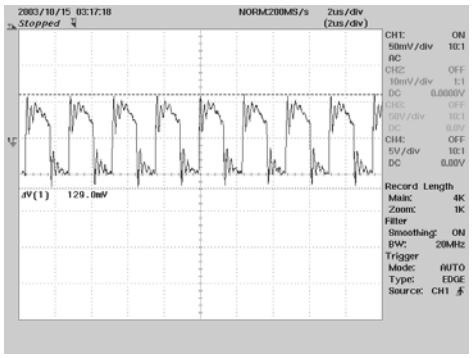

Figure 18 – +9 V Ripple, Full Load, 50mV/div; T: 2usec/div

130mV p-p

Figure 19 – +24 V Ripple, Full Load, 50mV/div; T: 2usec/div

160mV p-p

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11 Control Loop Measurements

11.1 Maximum Load

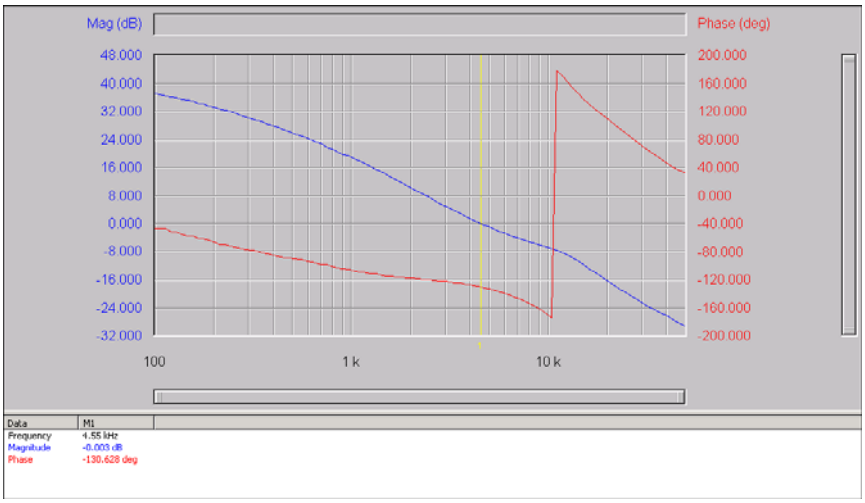

Figure 20 – Gain-Phase Plot, 28VDC Input Maximum Steady State Load
Vertical Scale: Gain = 8 dB/div, Phase = 40 °/div.
Crossover Frequency = 4.55 kHz Phase Margin = 49.4°

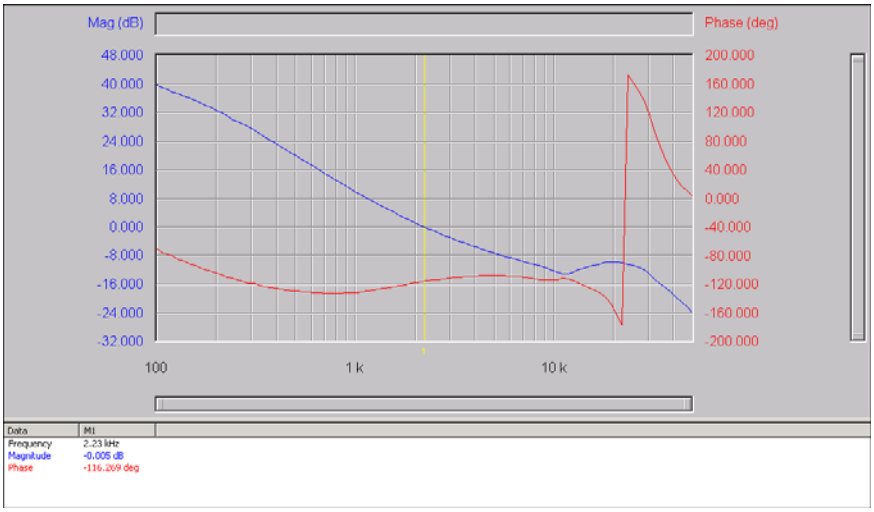

Figure 21 – Gain-Phase Plot, 48VDC Input Maximum Steady State Load
Vertical Scale: Gain = 8 dB/div, Phase = 40 °/div.
Crossover Frequency = 2.23 kHz Phase Margin = 63.7°

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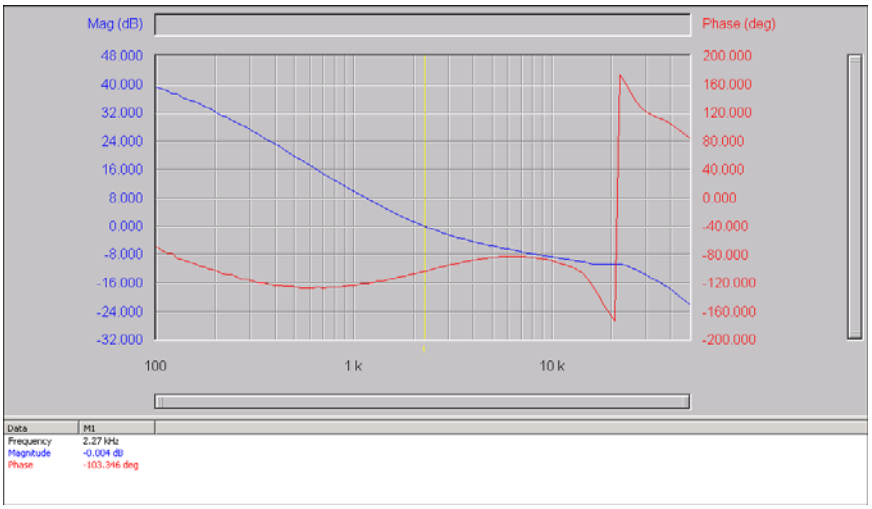

Figure 22 – Gain-Phase Plot, 60 VDC Input Maximum Steady State Load
Vertical Scale: Gain = 8 dB/div, Phase = 40 °/div.
Crossover Frequency = 2.27 kHz Phase Margin = 76.7°

11.2 Minimum Load

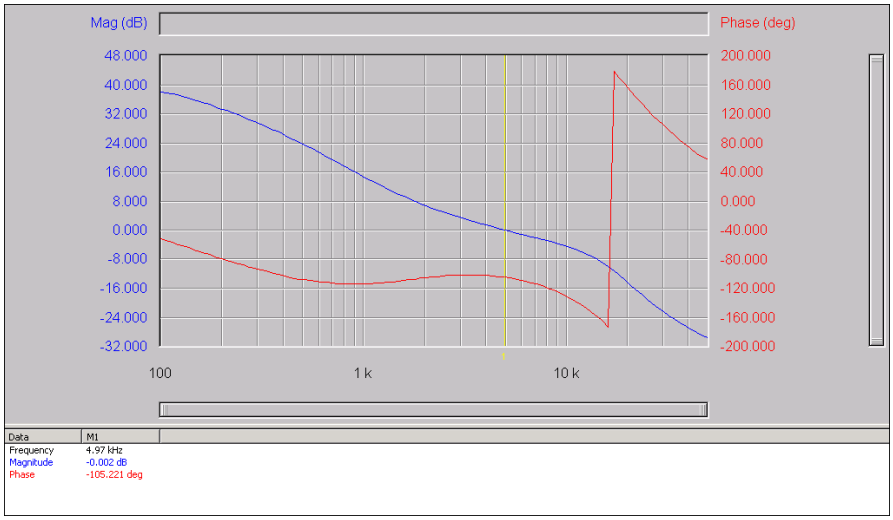

Figure 23 – Gain-Phase Plot, 28 VDC Input Minimum Load
Vertical Scale: Gain = 8 dB/div, Phase = 40 °/div.
Crossover Frequency = 4.97 kHz Phase Margin = 74.8°

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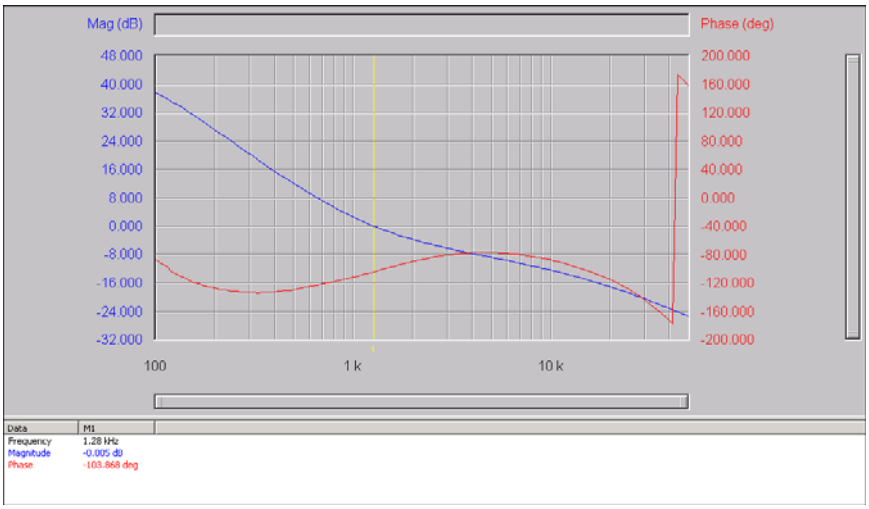

Figure 24 – Gain-Phase Plot, 48 VDC Input Minimum Load
Vertical Scale: Gain = 8 dB/div, Phase = 40 °/div.
Crossover Frequency = 1.28 kHz Phase Margin = 76.1°

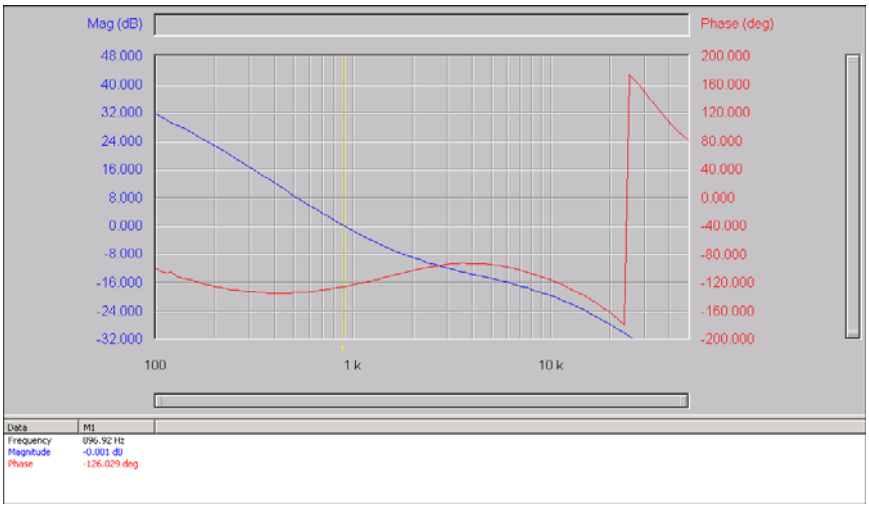

Figure 25 – Gain-Phase Plot, 60 VDC Input Minimum Load
Vertical Scale: Gain = 8 dB/div, Phase = 40 °/div.
Crossover Frequency = 896Hz Phase Margin = 53.98°

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12 Revision History

Date	Author	Revision	Description & changes	Reviewed
10-26-05	RSP	1.0	Initial release	VC, JC, KM

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