Design Example Report

Title	***4.5W (6Wpk) Multiple Output DVB-T Power Supply using TNY264P***
Specification	Input: 195 – 265 VAC Output: 2.5V/0.55A (0.7A pk), 3.3V/0.3A (0.4A pk), 12V/100mA(0.15 A pk), 33V/1.5mA (2mA pk)
Application	DVB–T Set Top Box
Author	Power Integrations Applications Department
Document Number	DER-46
Date	April 20, 2005
Revision	1.0

Summary and Features

This document is a prototype engineering report describing a 6 W multiple output power supply utilizing a TNY264P for a DVB-T Set-Top supply.

- Low cost / component count
- No Y-cap / no X-cap / no common-mode choke
- Low EMI even with output grounded
- Good output cross-regulation with no post-regulators

Power Integrations
5245 Hellyer Avenue, San Jose, CA 95138 USA.
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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

Design Reports contain a power supply design specification, schematic, bill of materials, and transformer documentation. Performance data and typical operation characteristics are included. Typically only a single prototype has been built.

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1 Introduction

This document is a prototype engineering report describing a 6 W multiple output power supply utilizing a TNY264P for a DVB-T Set-Top supply.

This design is low cost and meets EMI with no common-mode choke, no X-cap, and no Y-cap. Cross-regulation is tight even though it has multiple outputs with no post-regulators.

The DBV-T Set-Top has several advantages using Power Integrations' TinySwitch-II – TNY264P.

- No external AC/DC Adapter
- No internal DC/DC post converter
- No common mode Ferrite Core on the DC cord

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

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2 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	195		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
Output						
Output Voltage 1	V_{OUT1}	2.35	2.5	2.65	V	
Output Ripple Voltage 1	$V_{RIPPLE1}$			50	mV	20 MHz Bandwidth
Output Current 1	I_{OUT1}		0.55	0.7	A	
Output Voltage 2	V_{OUT2}	3.15	3.3	3.45	V	=
Output Ripple Voltage 2	$V_{RIPPLE2}$			50	mV	20 MHz Bandwidth
Output Current 2	I_{OUT2}		0.30	0.40	A	
Output Voltage 3	V_{OUT3}	4.75	5	5.25	V	
Output Ripple Voltage 3	$V_{RIPPLE3}$			50	mV	20 MHz Bandwidth
Output Current 3	I_{OUT3}		0.10	0.15	A	
Output Voltage 4	V_{OUT4}	11.5	12	12.5	V	
Output Ripple Voltage 4	$V_{RIPPLE4}$			80	mV	20 MHz Bandwidth
Output Current 4	I_{OUT4}		0.13	0.15	A	
Output Voltage 5	V_{OUT5}	30	33	33	V	
Output Ripple Voltage 5	$V_{RIPPLE5}$			400	mV	20 MHz Bandwidth
Output Current 5	I_{OUT5}		1.5	2.0	mA	
Total Output Power						
Continuous Output Power	P_{OUT}		4.5		W	
Peak Output Power	P_{OUT_PEAK}			6	W	
Efficiency	η		62		%	Measured at full load, 25 °C
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Ambient Temperature	T_{AMB}	0		40	°C	Free convection, sea level

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3 Schematic

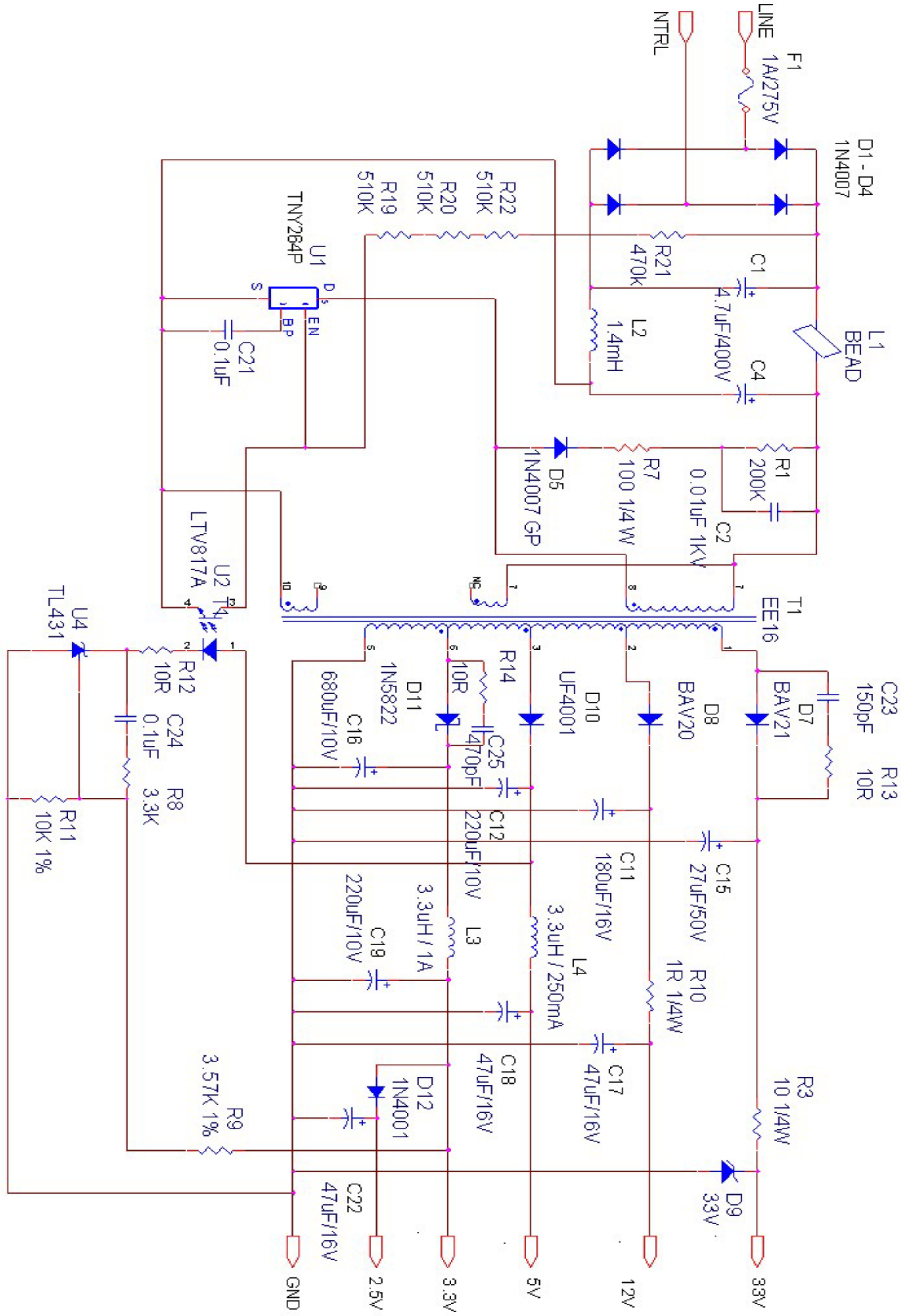

Figure 1 – Schematic

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4 Circuit Description

The schematic in Figure 1 shows an off-line flyback converter using the TNY264P. The circuit is designed to operate from 195 VAC to 265 VAC input and provides isolated multiple outputs (i.e. 2.5V; 3.3V; 5V; 12V; 33V).

4.1 TinySwitch Primary

AC input power is rectified by a full bridge, consisting of D1 through D4. The rectified DC is then filtered by the bulk storage capacitors C1 and C4. Inductors L1, L2, C1 and C4 form a pi (π) filter, which attenuates conducted differential-mode EMI noise.

The rectified DC rail is applied to one end of the transformer primary, the other end being connected to the drain pin of the integrated MOSFET of U1.

To keep the peak DRAIN voltage acceptably below the BV_{DSS} (700V) of U1, diode D5, C2, R1, and R7 form a primary clamp. This network clamps the voltage spike seen on the DRAIN due to primary and secondary reflected leakage inductance.

Capacitor C21 is the decoupling cap for the TOPSwitch.

R19, R20, R21 and R22 enables the under voltage (UV) line sensing that inhibits U1 to start switching below 70VAC during start-up.

4.2 Output Rectification

The secondary of T1 has four windings AC stacked together. Each rectified and filtered to provide 3.3V, 5V, 12V and 33V DC outputs. While the 2.5V output was derived from 3.3V through a voltage dropping diode D12.

A zener (D9) - resistor (R3) pre load was employed to clamp the 33V from going over voltage only when it is lightly loaded while the rest of the outputs are heavily loaded.

4.3 Output Feedback and control

The main feedback loop is closed on 3.3V output. DC feedback to the output voltage regulator error amplifier (U4) comes from a divider network R9 and R11. The center point is tied to the reference input of U4. Capacitor C24 and resistor R8 roll off the high frequency gain of U4 while R12 sets the overall gain.

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5 PCB Layout

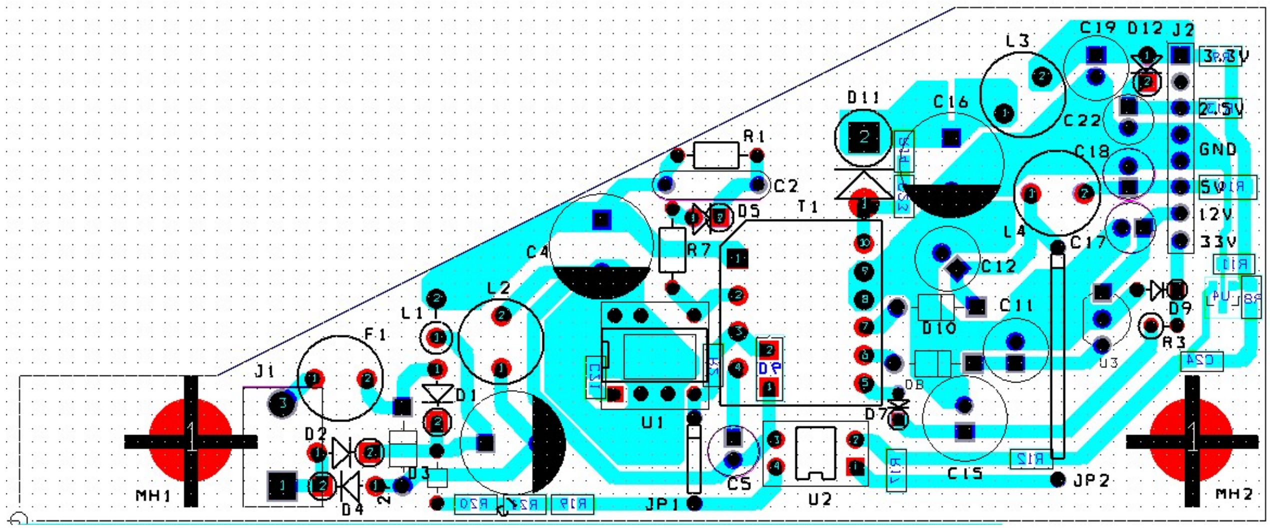

Figure 2 – Printed Circuit Layout

Note: The assembled unit has some component locations not fitted.

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6 Bill Of Materials

Item	Quantity	Reference	Part
1	2	C1	4.7uF/400V_Electrolytic capacitor
		C4	4.7uF/400V_Electrolytic capacitor
2	1	C2	0.01uF 1KV_Ceramic capacitor
3	1	C11	180uF/16V_LOW ESR electrolytic capacitor
4	2	C19	220uF/10V_LOW ESR electrolytic capacitor
		C12	220uF/10V_LOW ESR electrolytic capacitor
5	1	C15	27uF/50V_LOW ESR electrolytic capacitor
6	1	C16	680uF/10V_LOW ESR electrolytic capacitor
7	3	C17	47uF/16V_General purpose electrolytic capacitor
		C18	47uF/16V_General purpose electrolytic capacitor
		C22	47uF/16V_General purpose electrolytic capacitor
8	2	C21	0.1uF; 0805
		C24	0.1uF; 0805
9	1	C23	150pF/ 200V; Ceramic
10	1	C25	470pF/ 100V; Ceramic
11	4	D2	1N4007
		D3	1N4007
		D4	1N4007
		D1	1N4007
12	1	D5	1N4007 GP
13	1	D7	BAV21
14	1	D8	BAV20
15	1	D9	33V Zener 2%
16	1	D10	UF4001
17	1	D11	1N5822
18	1	D12	1N4001
19	1	F1	1A/275V Safety Fuse
20	1	L1	BEAD
21	1	L2	1.4mH
22	1	L3	3.3uH / 1A
23	1	L4	3.3uH / 250mA
24	1	R1	200K 1/4W
25	1	R3	10R 1/4W
26	1	R7	100R 1/4 W
27	1	R8	3.3K; 0805
28	1	R9	3.57K 1%; 0805
29	1	R10	1R 1/4W
30	1	R11	10K 1%; 0805
31	3	R12	10R; 0805
		R13	10R; 005
		R14	10R; 0805
32	3	R19	510K; 0805
		R20	510K; 0805
		R22	510K; 0805
33	1	R21	470K 1/8W
34	1	T1	Custom EE16
35	1	U1	TNY264P
36	1	U2	LTV817A
37	1	U4	TL431_SOT23

Note: All resistors and capacitors are SMD-0805 unless otherwise specified.

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7 Transformer Specification

7.1 Electrical Diagram

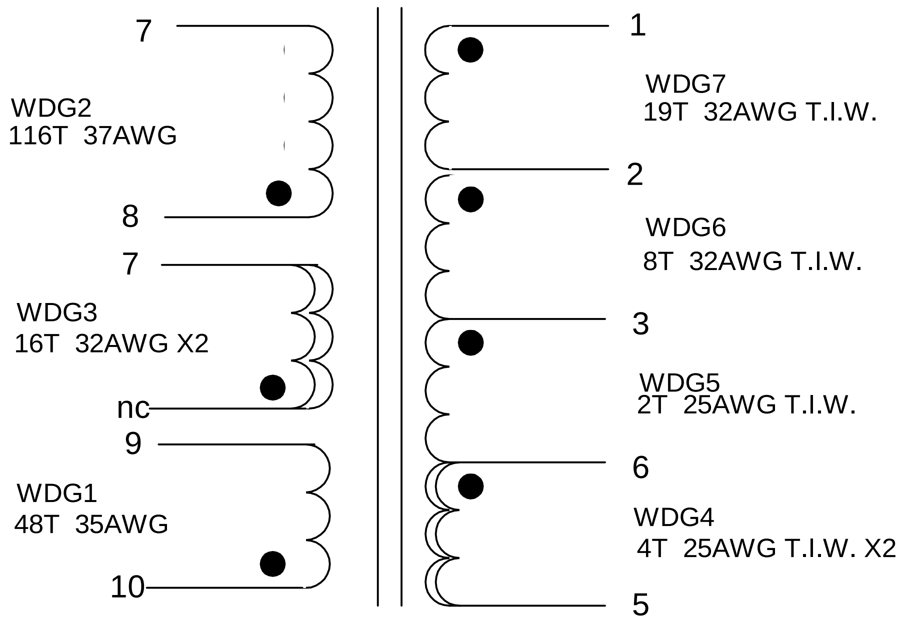

Figure 3 –Transformer Electrical Diagram

7.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1-6 to pins 7-10	3000 VAC
Primary Inductance	Pins 7-8, all other windings open. Measured at 132 kHz, 1 VRMS	2.4 mH +/- 7%
Resonant Frequency	Pin 7-8, all other windings open	300 kHz (Min.)
Primary Leakage Inductance	Pins 7-8, with pins 1-6 shorted. Measured at 132 kHz, 1 VRMS	70 µH (Max.)

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7.3 Materials

Item	Description
[1]	Core: EE16, Gapped for AL of 178 nH/T^2
[2]	Bobbin: EE16 Vertical 10 pins
[3]	Magnet Wire: # 35 AWG
[4]	Magnet Wire: #37 AWG
[5]	Magnet Wire: #32 AWG
[6]	Triple Insulated Wire (T.I.W.) #25AWG
[7]	Triple Insulated Wire (T.I.W.) #32AWG
[8]	Tape: 3M 1298 Polyester Film, 8.2mm wide

7.4 Transformer Build Diagram

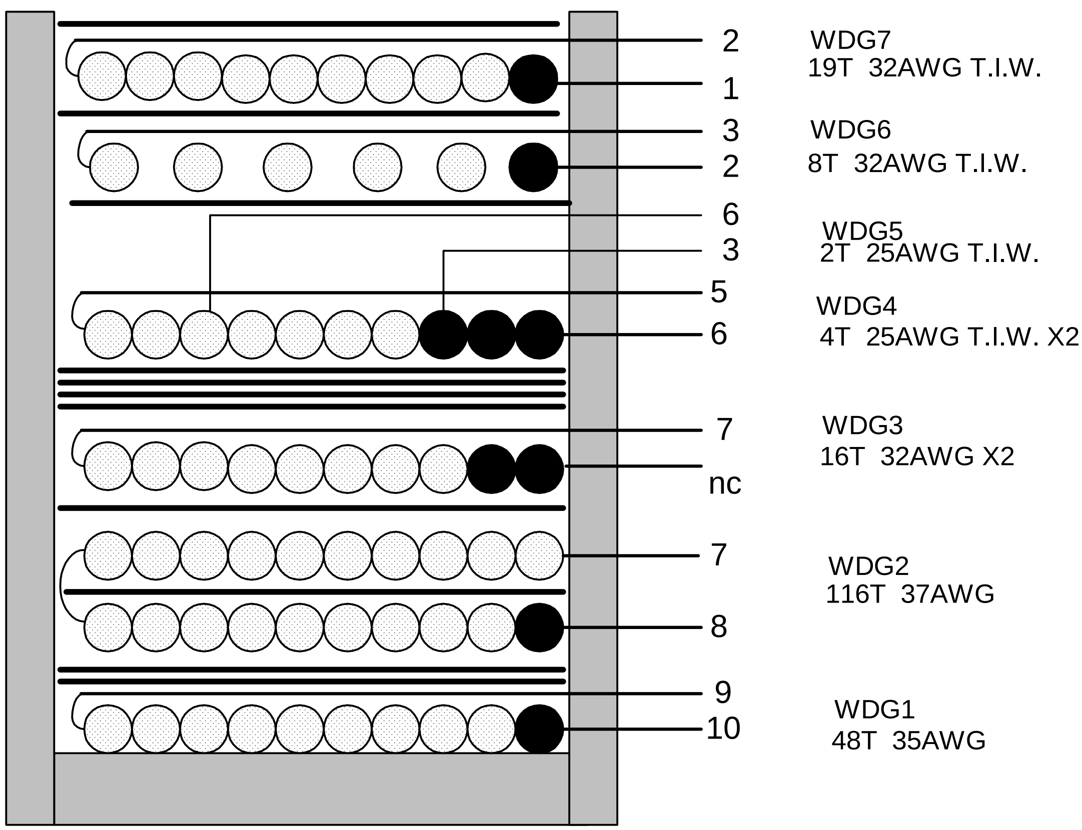

Figure 4 – Transformer Build Diagram

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7.5 Winding Instructions

Bobbin Set Up Orientation	Set up the bobbin with its pins oriented to the right hand side.
WDG1: SHLD1 Winding	Start at pin 10. Wind 48 turns of magnetic wire #35AWG from right to left. No winding should overlap. Finish at pin 9.
Basic Insulation	Apply 2 layers of tape (8.2mm)
WDG2: Primary Winding (2 layers)	Start at pin 8. Wind 58 turns of magnetic wire #37AWG from right to left. Place 1T of tape (8.2mm). Continue winding 58 turns from left to right for the second layer. No winding should overlap. Finish on pin 7.
Basic Insulation	Apply 1 layer of tape (8.2mm)
WDG3: SHLD2 Winding	Start on pin 10 temporarily. Wind 16 bifilar turns of magnetic wire #32AWG from right to left. No winding should overlap. Finish on pin 7. Cut trim start lead from pin 10.
Basic Insulation	Apply 4 layers of tape (8.2mm)
WDG4: 3.3 V Winding.	Start at pin 6. Wind 4 bifilar turns of T.I.W#25AWG. The wires should be tightly and uniformly wound spread across the bobbin width. Finish on pin 5.
WDG5: 5V Winding	Start on pin 3. Wind 2 turns of T.I.W#25AWG. Wind the wire between 3.3V windings. Finish on pin 6.
Basic Insulation	Apply 1 layer of tape (8.2mm)
WDG6: 12V Winding	Start at pin 2. Wind 8 turns of T.I.W#32AWG. Wind uniformly spread across the bobbin. Finish at pin 3.
Basic Insulation	Apply 1 layer of tape (8.2mm)
WDG7: 33V Winding	Start at pin 1. Wind 19 turns of T.I.W#32AWG. Finish on pin 2.
Basic Insulation	Apply 1 layer of tape (8.2mm)
Core Assembly	Assemble and secure core halves. Item [1]

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8 Transformer Spreadsheet

Design Passed (No Optimization)							
Power Supply Input							
VACMIN	Volts	195					Min Input AC Voltage
VACMAX	Volts	265					Max Input AC Voltage
FL	Hertz	50					AC Main Frequency
TC	mSecond	1.75					Bridge Rectifier Conduction Time Estimate
Z		0.69					Loss Allocation Factor
N	%	70.0					Efficiency Estimate
Power Supply Outputs							
VOx	Volts		5.00	3.30	12.00	33.00	Output Voltage
IOx	Amps		0.100	1.000	0.130	0.015	Output Current
Device Variables							
Device		TNY264P/G					Device Name
PO	Watts	5.85					Total Output Power
VDRAIN	Volts	630					Maximum Drain Voltage Estimate (Includes Effect of Leakage Inductance)
VDS	Volts	6.7					Device On-State Drain to Source Voltage
FSNOM	Hertz	132000					TinySwitch-II Switching Frequency
FSMIN	Hertz	120000					TinySwitch-II Minimum Switching Frequency (inc. Jitter)
FSMAX	Hertz	144000					TinySwitch-II Maximum Switching Frequency (inc. Jitter)
KRPKDP		1.02					Ripple to Peak Current Ratio
ILIMITMIN	Amps	0.23					Device Current Limit Minimum
ILIMITMAX	Amps	0.27					Device Current Limit Maximum
IRMS	Amps	0.08					Primary RMS Current
DMAX		0.31					Maximum Duty Cycle
Power Supply Components Selection							
CIN	uFarads	9.4					Input Filter Capacitor
VMIN	Volts	248					Minimum DC Input Voltage
VMAX	Volts	375					Maximum DC Input Voltage
VCLO	Volts	170					Clamp Zener Voltage
PZ	Watts	0.6					Estimated Primary Zener Clamp Loss
Power Supply Output Parameters							
VDx	Volts		0.5	0.5	0.7	1.0	Output Winding Diode Forward Voltage Drop
PIVSx	Volts		23	16	54	147	Output Rectifier Maximum Peak Inverse Voltage
ISPx	Amps		0.37	3.66	0.48	0.05	Peak Secondary Current
ISRMSx	Amps		0.17	1.74	0.23	0.03	Secondary RMS Current
IRIPPLEx	Amps		0.14	1.42	0.18	0.02	Output Capacitor RMS Ripple Current
Transformer Construction Parameters							
Core/Bobbin		EE16					Core and Bobbin Type
Core Manuf.		Generic					Core Manufacturing
Bobbin Manuf		Generic					Bobbin Manufacturing
LPmin	uHenries	2390					Minimum Primary Inductance
NP		118					Primary Winding Number of Turns
AWG	AWG	36					Primary Wire Gauge (Rounded to next smaller standard AWG value)
CMA	Cmils/A	320					Primary Winding Current Capacity
VOR	Volts	112.00					Reflected Output Voltage
BW	mm	8.50					Bobbin Physical Winding Width
M	mm	0.0					Safety Margin Width
L		2.5					Number of Primary Layers
AE	cm^2	0.19					Core Effective Cross Section Area
ALG	nH/T^2	172					Gapped Core Effective Inductance
BM	Gauss	3077					Maximum Operating Flux Density
BAC	Gauss	1312					AC Flux Density for Core Curves
LG	mm	0.12					Gap Length
LL	uHenries	47.8					Estimated Transformer Primary Leakage Inductance
LSEC	nHenries	20					Estimated Secondary Trace Inductance
Secondary Parameters							
NSx			5.79	4.00	13.37	35.79	Secondary Number of Turns
Rounded Down NSx			5		13	35	Rounded to Integer Secondary Number of Turns
Rounded Dc	Volts		4.26		11.68	32.33	Auxiliary Output Voltage for Rounded to Integer NSx
Rounded Up NSx			6		14	36	Rounded to Next Integer Secondary Number of Turns
Rounded Up	Volts		5.21		12.63	33.29	Auxiliary Output Voltage for Rounded to Next Integer NSx
AWGSx Rar	AWG		31 - 35	21 - 25	30 - 34	40 - 44	Secondary Wire Gauge Range Comment: Primary wire gauge is less than recommended minimum (26 AWG) and may overheat Tip: Consider a parallel winding technique (bifilar, trifilar), increase size of transformer (larger BW) or reduce margin (M). Comment: Wire

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9 Performance Data

All measurements performed at room temperature, 60 Hz input frequency.

9.1 Efficiency

Loading: 0.55A@2.5V; 0.30A@3.3V; 0.10A@5V; 0.13A@12V; 2mA@33V

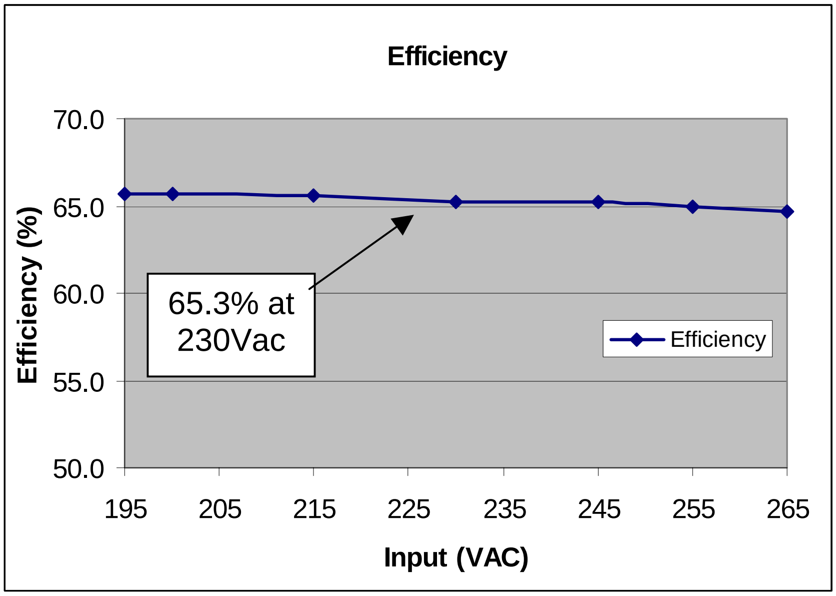

Figure 5- Efficiency vs. Input Voltage, Room Temperature, 60 Hz. The efficiency at 230Vac is 65.3%

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9.2 Worst Case Cross Regulation

The test was done at room temperature at minimum and maximum input voltage.

Voltage input @195Vac

Load (A)					Output (V)				
3.3V	2.5V	5V	12V	33V	3.3V	2.5V	5V	12V	33V
0.3	0.55	0.1	0.13	2mA	3.34	2.52	4.98	12.17	32.29
0	0.55	0.1	0.13	2	3.35	2.53	4.91	11.95	31.98
0	0.22	0.1	0.13	2	3.37	2.58	4.77	11.53	31.27
0.2	0.20	0.15	0.15	2	3.36	2.57	4.77	11.73	31.77
0.3	0.55	0.03	0.1	2	3.33	2.51	5.19	12.43	32.5
0.3	0.55	0.01	0.08	2	3.33	2.5	5.18	12.42	32.6
0.4	0.70	0.01	0.08	2	3.33	2.50	5.18	12.42	32.6
0.4	0.70	0.15	0.15	2	3.34	2.52	4.91	12.16	32.4

Voltage input @265Vac

Load (A)					Output (V)				
3.3V	2.5V	5V	12V	33V	3.3V	2.5V	5V	12V	33V
0.3	0.55	0.1	0.13	2mA	3.34	2.52	5.0	12.19	32.44
0	0.55	0.1	0.13	2	3.35	2.53	4.92	11.93	32.09
0	0.22	0.1	0.13	2	3.37	2.58	4.78	11.53	31.39
0.2	0.20	0.15	0.15	2	3.36	2.57	4.78	11.74	31.86
0.3	0.55	0.03	0.1	2	3.33	2.51	5.20	12.38	32.6
0.3	0.55	0.01	0.08	2	3.33	2.51	5.21	12.47	32.6
0.4	0.70	0.01	0.08	2	3.33	2.50	5.20	12.46	32.8
0.4	0.70	0.15	0.15	2	3.34	2.52	4.93	12.20	32.5

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10 Thermal Performance

Measurement was taken at 195Vac; $T_{AMBIENT}$ =25^{o}C with no airflow.

Reference	Description	All outputs at Nominal Load	All outputs at Peak Load
U1	TNY264P	***56ºC***	***70ºC***
T1	EE13 Transformer	***47ºC***	***51ºC***
D11	3.3V Rectifier	***57ºC***	***64ºC***

11 Waveforms

11.1 Drain Voltage and Current, Normal Operation

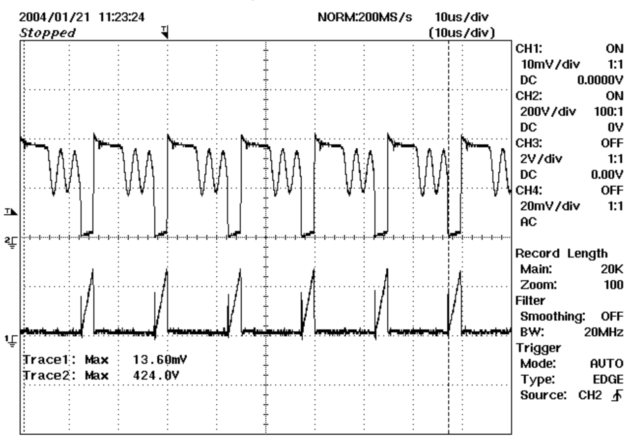

Figure 6 - 195 VAC, Full Load.
Upper: V_{DRAIN}, 200 V, 10 µs / div
Lower: I_{DRAIN}, 0.2 A / div

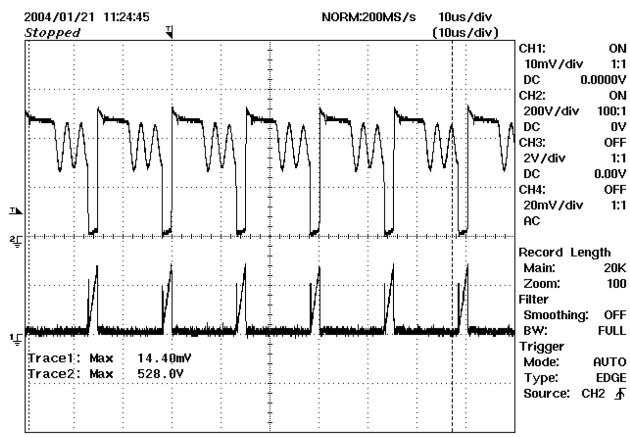

Figure 7 - 265 VAC, Full Load
Upper: V_{DRAIN}, 200 V, 10 µs / div
Lower: I_{DRAIN}, 0.2 A / div

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11.2 Output Ripple Measurements

11.2.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in Figure 8 and Figure 9.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1.0 μF/50 V aluminum electrolytic. ***The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).***

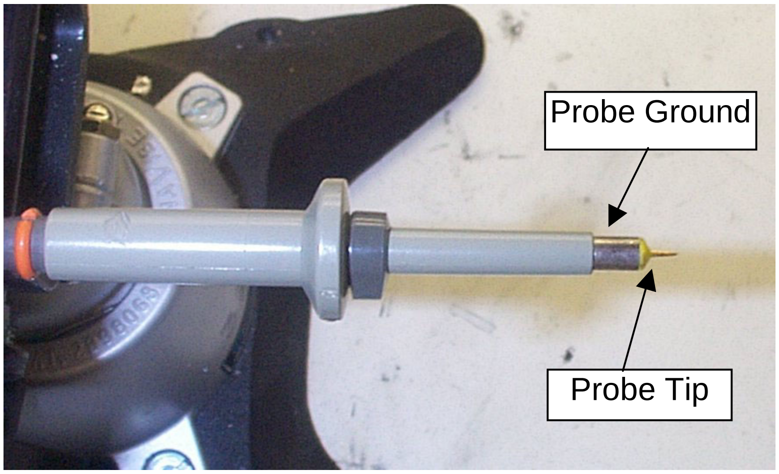

Figure 8 - Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

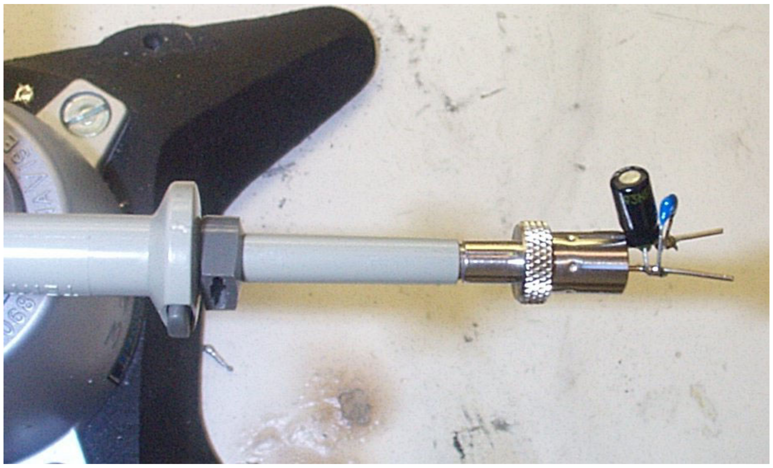

Figure 9 - Oscilloscope Probe with Probe Master 5125BA BNC Adapter. (Modified with wires for probe ground for ripple measurement, and two parallel decoupling capacitors added)

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11.2.2 Measurement Results

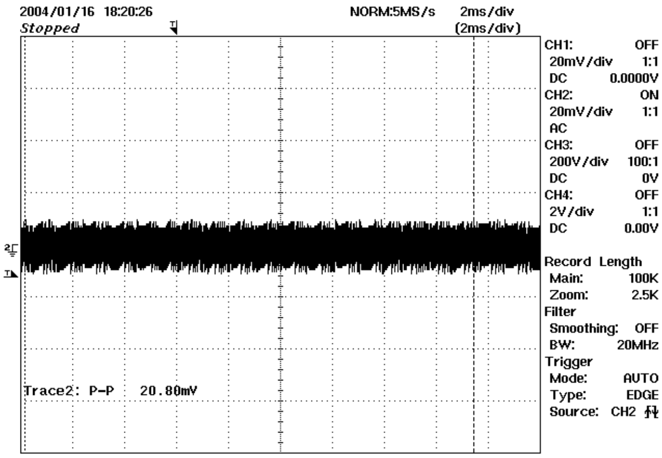

Figure 10 – 3.3V Ripple, 195 VAC, Full Load.
2 ms, 20 mV / div

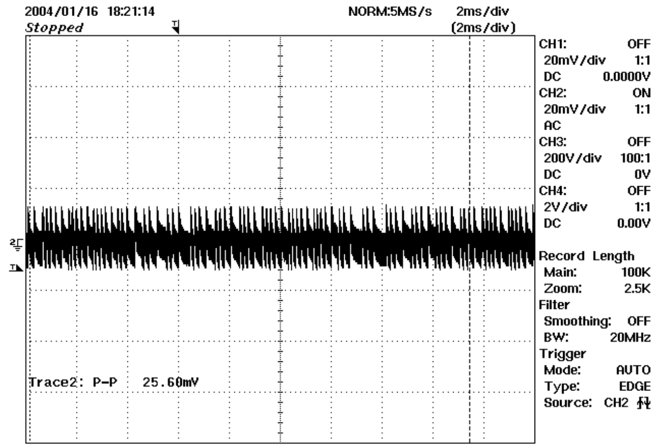

Figure 11 –3.3V Ripple, 265 VAC, Full Load.
2 ms, 20 mV / div

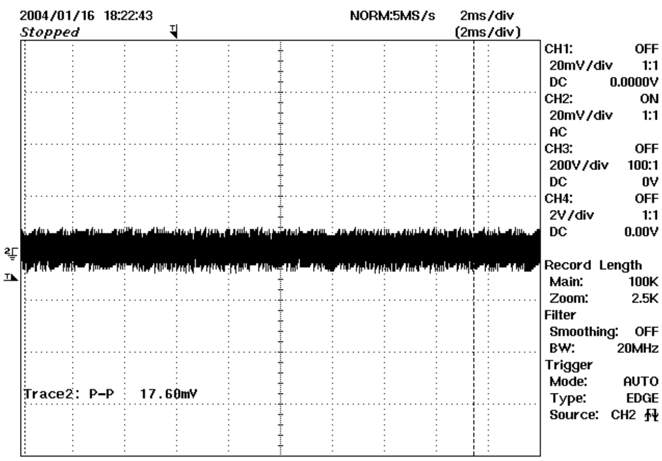

Figure 12 – 2.5VRipple, 195 VAC, Full Load.
2 ms, 20 mV /div

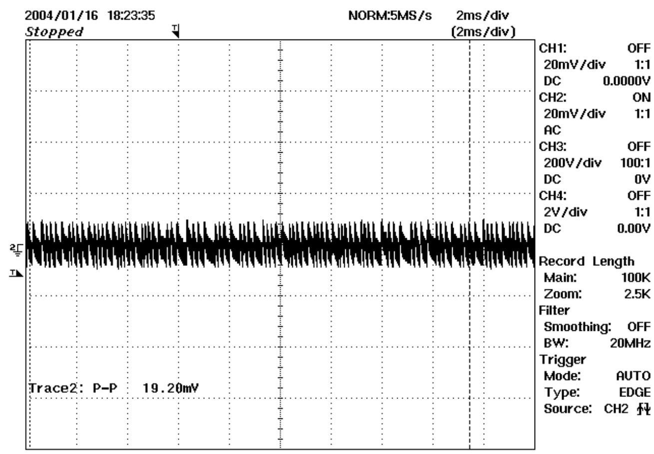

Figure 13 – 2.5VRipple, 265 VAC, Full Load.
2 ms, 20 mV /div

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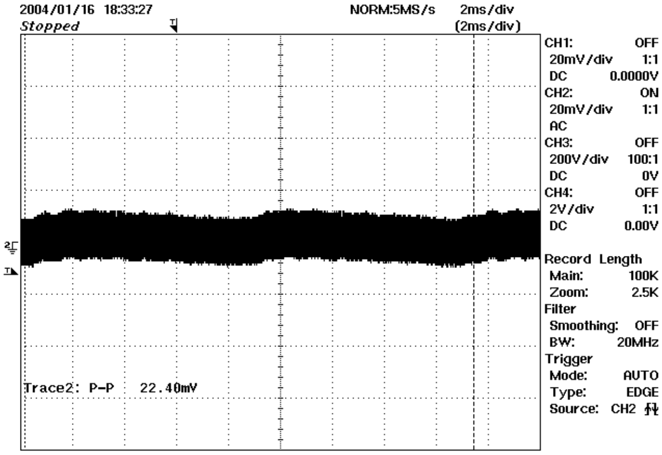

Figure 14 – 5V Ripple, 195 VAC, Full Load.
2 ms, 20 mV / div

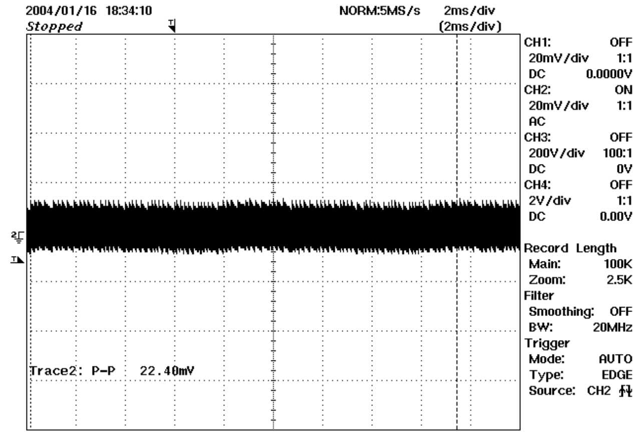

Figure 15 –5V Ripple, 265 VAC, Full Load.
2 ms, 20 mV / div

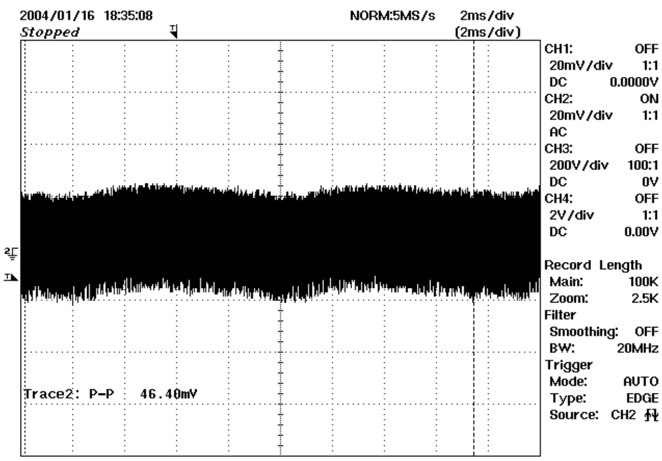

Figure 16 – 12VRipple, 195 VAC, Full Load.
2 ms, 20 mV /div

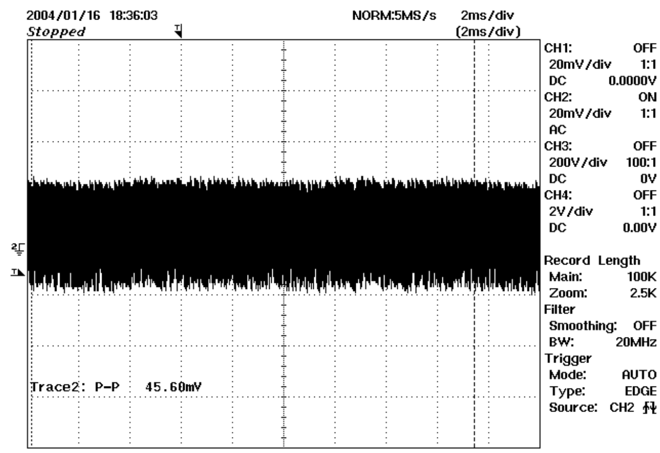

Figure 17 – 12VRipple, 265 VAC, Full Load.
2 ms, 20 mV /div

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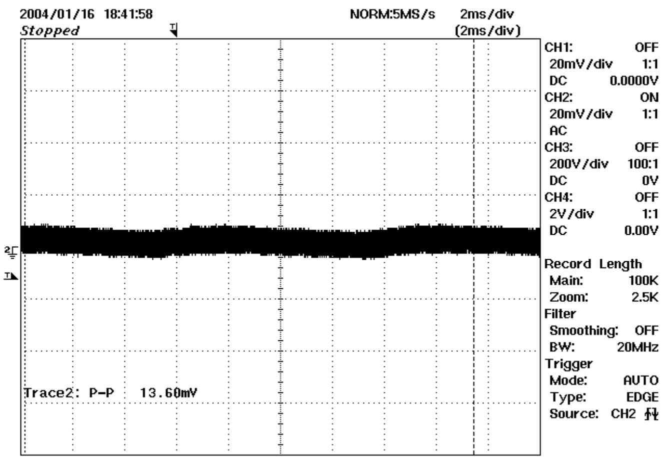

Figure 18 – 33V Ripple, 195 VAC, Full Load.
2 ms, 20 mV / div

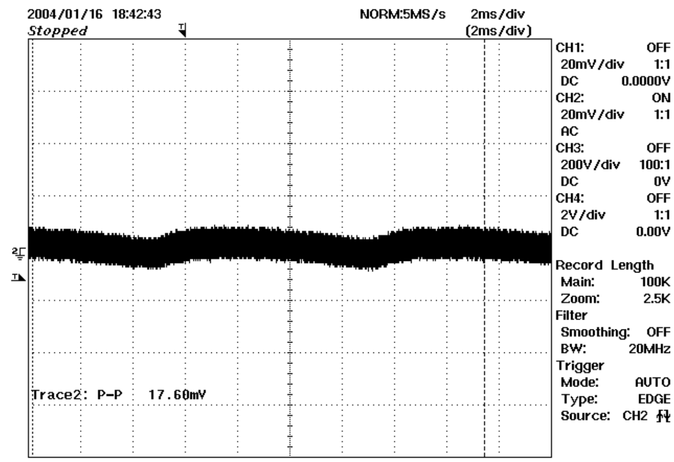

Figure 19 –33V Ripple, 265 VAC, Full Load.
2 ms, 20 mV / div

11.3 Transient Response: 3.3V – 50% - 100% Load Step

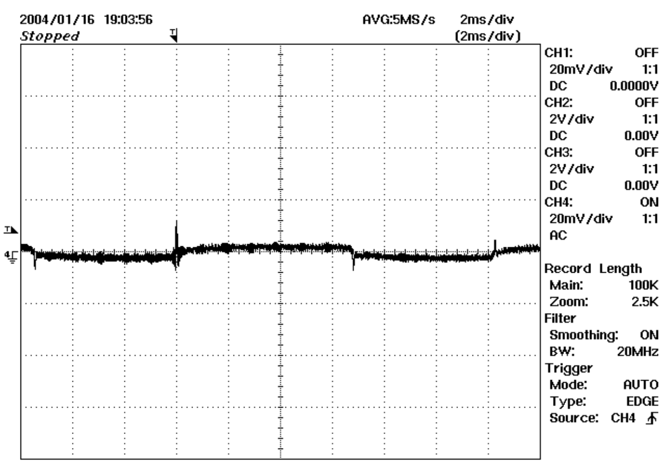

Figure 20 – 3.3V, 195 VAC, 200mA-400mA.
2 ms, 20 mV / div

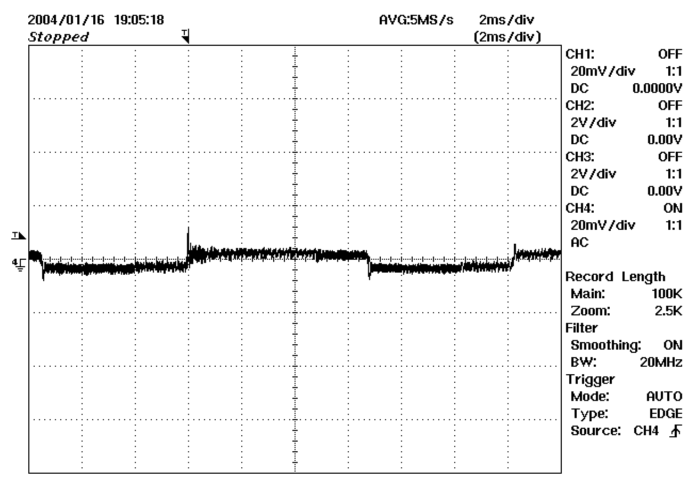

Figure 21 –3.3V, 265 VAC, 200mA-400mA.
2 ms, 20 mV / div

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12 Conducted EMI

EMI was tested at room temperature, 230 VAC input, with following resistor load on each output: 11 ohms @ 3.3 V; 4.5 ohms @ 2.5V; 49.6 ohms @ 5V; 94 ohms @ 12V; 21 Kohms @ 33V.

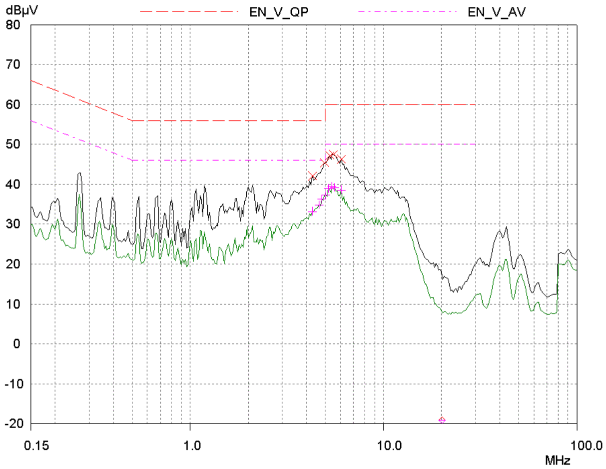

Figure 22 – NEUTRAL, Secondary Ground Connected to Earth.

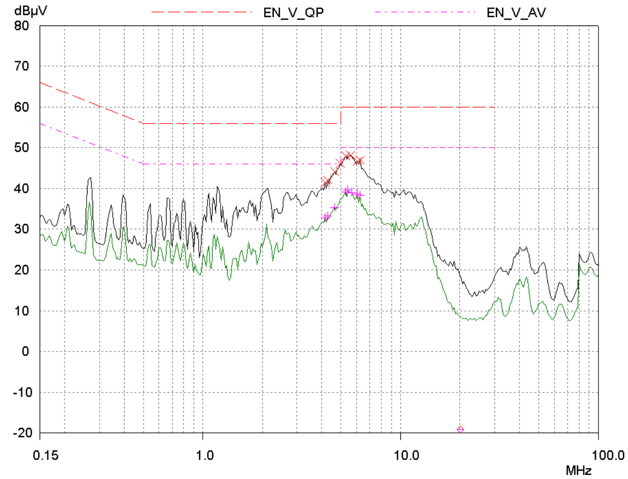

Figure 23 – LINE, Secondary Ground Connected to Earth.

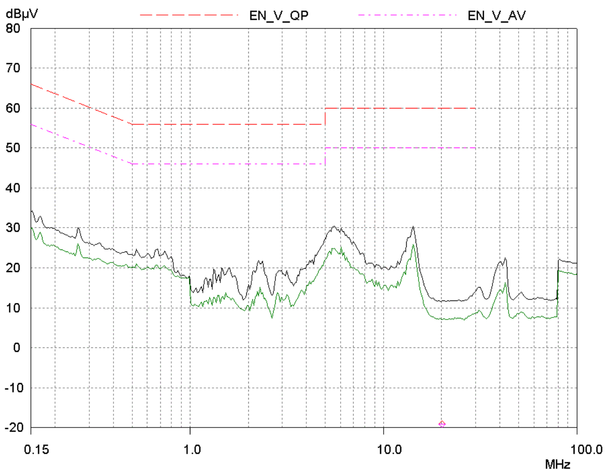

Figure 24 – NEUTRAL, Secondary Ground NOT Connected to Earth.

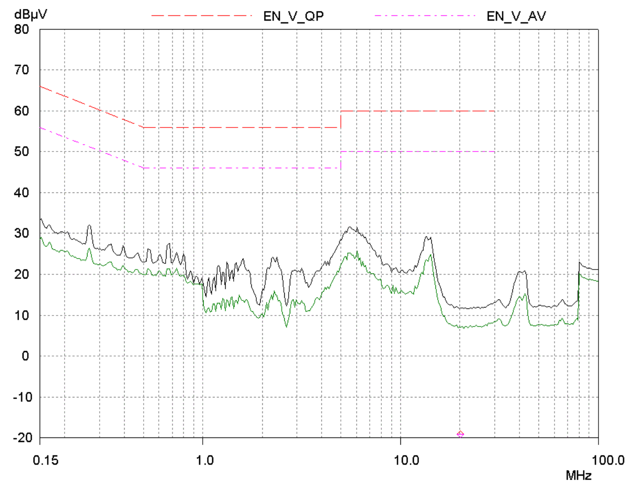

Figure 25 - LINE, Secondary Ground NOT Connected to Earth.

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Tel: +1 408 414 9200 Fax: +1 408 414 9201
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13 Revision History

Date	Author	Revision	Description & changes	Reviewed
April 20, 2005	ME	1.0	Initial release	VC / AM

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

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WORLD HEADQUARTERS
Power Integrations
5245 Hellyer Avenue,
San Jose, CA 95138, USA
Main: +1-408-414-9200
Customer Service:
Phone: +1-408-414-9665
Fax: +1-408-414-9765
e-mail:
usasales@powerint.com

CHINA (SHENZHEN)
Power Integrations
International Holdings, Inc.
Rm# 1705, Bao Hua Bldg.
1016 Hua Qiang Bei Lu,
Shenzhen, Guangdong,
518031, China
Phone: +86-755-8367-5143
Fax: +86-755-8377-9610
e-mail: chinasales@powerint.com

ITALY
Power Integrations s.r.l.
Via Vittorio Veneto 12,
Bresso, Milano,
20091, Italy
Phone: +39-028-928-6001
Fax: +39-028-928-6009
e-mail:
eurosales@powerint.com

SINGAPORE (ASIA PACIFIC HEADQUARTERS)
Power Integrations, Singapore
51 Newton Road,
#15-08/10 Goldhill Plaza,
Singapore, 308900
Phone: +65-6358-2160
Fax: +65-6358-2015
e-mail:
singaporesales@powerint.com

AMERICAS
Power Integrations, Inc.
4335 South Lee Street,
Suite G,
Buford, GA 30518, USA
Phone: +1-678-714-6033
Fax: +1-678-714-6012
e-mail:
usasales@powerint.com

GERMANY
Power Integrations, GmbH
Rueckerstrasse 3,
D-80336, Munich, Germany
Phone: +49-895-527-3910
Fax: +49-895-527-3920
e-mail: eurosales@powerint.com

JAPAN
Power Integrations, K.K.
Keihin-Tatemono 1st Bldg.
12-20 Shin-Yokohama,
2-Chome,
Kohoku-ku, Yokohama-shi,
Kanagawa 222-0033, Japan
Phone: +81-45-471-1021
Fax: +81-45-471-3717
e-mail:
japansales@powerint.com

TAIWAN
Power Integrations
International Holdings, Inc.
17F-3, No. 510,
Chung Hsiao E. Rd., Sec. 5,
Taipei, Taiwan 110, R.O.C.
Phone: +886-2-2727-1221
Fax: +886-2-2727-1223
e-mail:
taiwansales@powerint.com

CHINA (SHANGHAI)
Power Integrations
International Holdings, Inc.
Rm 807, Pacheer,
Commercial Centre,
555 Nanjing West Road,
Shanghai, 200041, China
Phone: +86-21-6215-5548
Fax: +86-21-6215-2468
e-mail:
chinasales@powerint.com

INDIA (TECHNICAL SUPPORT)
Innovatech
261/A, Ground Floor
7th Main, 17th Cross,
Sadashivanagar
Bangalore, India, 560080
Phone: +91-80-5113-8020
Fax: +91-80-5113-8023
e-mail: indiasales@powerint.com

KOREA
Power Integrations
International Holdings, Inc.
8th Floor, DongSung Bldg.
17-8 Yoido-dong,
Youngdeungpo-gu,
Seoul, 150-874, Korea
Phone: +82-2-782-2840
Fax: +82-2-782-4427
e-mail:
koreasales@powerint.com

UK (EUROPE & AFRICA HEADQUARTERS)
1st Floor, St. James's House
East Street
Farnham, Surrey GU9 7TJ
United Kingdom
Phone: +44-1252-730-140
Fax: +44-1252-727-689
e-mail: eurosales@powerint.com

APPLICATIONS HOTLINE
World Wide +1-408-414-9660

APPLICATIONS FAX
World Wide +1-408-414-9760