



## Design Example Report

<b>Title</b>	<b><i>4.8 W Buck-Boost Converter Using LNK306P</i></b>
<b>Specification</b>	Input: 85 - 135 VAC Output: -24 V / 0.2 A
<b>Application</b>	Home Appliance
<b>Author</b>	Power Integrations Applications Department
<b>Document Number</b>	DER-59
<b>Date</b>	June 6, 2006
<b>Revision</b>	1.1

### Summary and Features

- Non-Isolated Topology - no direct path from input to output
- Low cost off the shelf inductor – no custom transformer required
- 15 components including EMI filter
- Loop Fault Protection
- Short Circuit Protection
- Hysteretic Thermal Shutdown
- Output Referenced to Neutral
- Precise Output Voltage control
- Frequency Jitter
- Excellent Conducted EMI (>10 dB margin across spectrum)
- Extremely low standby power consumption (<150 mW)

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### Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

Design Reports contain a power supply design specification, schematic, bill of materials, and transformer documentation. Performance data and typical operation characteristics are included. Typically only a single prototype has been built.



## 1 Introduction

This document is an engineering report describing a non-isolated buck-boost (inverting) power supply utilizing a LNK306P. This power supply is intended as a power supply for an appliance application.

The document contains the power supply specification, schematic, bill-of-materials, printed circuit layout, and performance data.

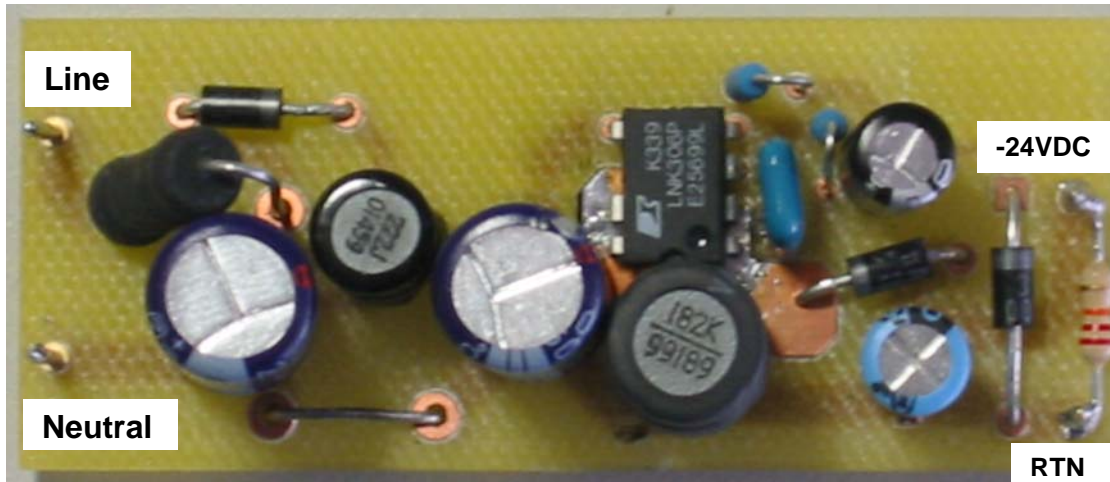


Figure 1 – Populated Circuit Board Photograph.

## 2 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
<b>Input</b>						
Voltage	$V_{IN}$	85		135	VAC	2 Wire – no P.E.
Frequency	$f_{LINE}$	47	50/60	64	Hz	
No-load Input Power (230 VAC)				0.15	W	
<b>Output</b>						
Output Voltage 1	$V_{OUT1}$	-26.4	-24	-21.6	V	± 10% 20 MHz Bandwidth
Output Ripple Voltage 1	$V_{RIPPLE1}$			400	mV	
Output Current 1	$I_{OUT1}$			0.2	A	
<b>Total Output Power</b>						
Continuous Output Power	$P_{OUT}$			4.8	W	
<b>Efficiency</b>	$\eta$				%	Measured at $P_{OUT}$ (4.8 W), 25 °C
<b>Environmental</b>						
Conducted EMI		Meets CISPR22B / EN55022B				1.2/50 $\mu$ s surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 $\Omega$ Common Mode: 12 $\Omega$
Safety		Designed to meet IEC950, UL1950 Class II				
Surge			TBD		kV	
Surge			TBD		kV	100 kHz ring wave, 500 A short circuit current, differential and common mode
Ambient Temperature	$T_{AMB}$	0		70	°C	Free convection, sea level



### 3 Schematic

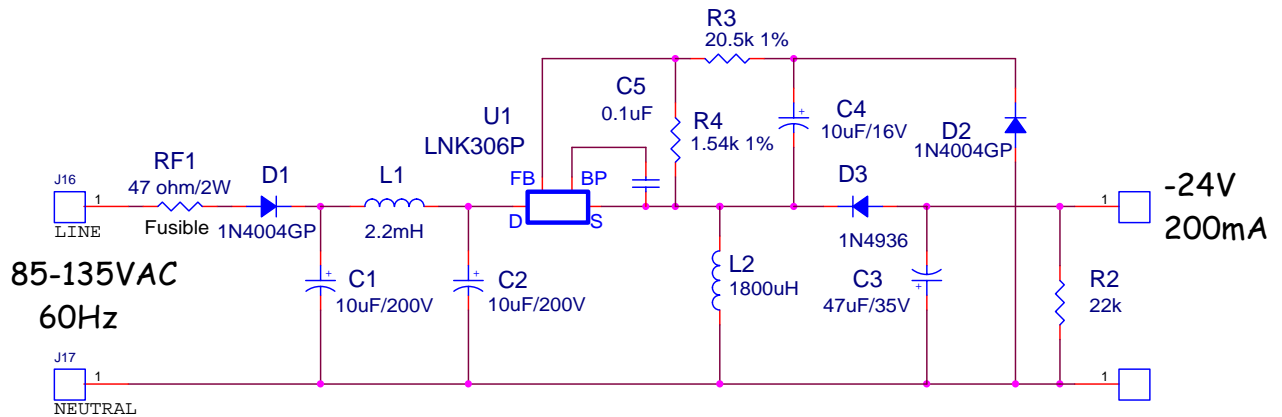


Figure 2 – Schematic.



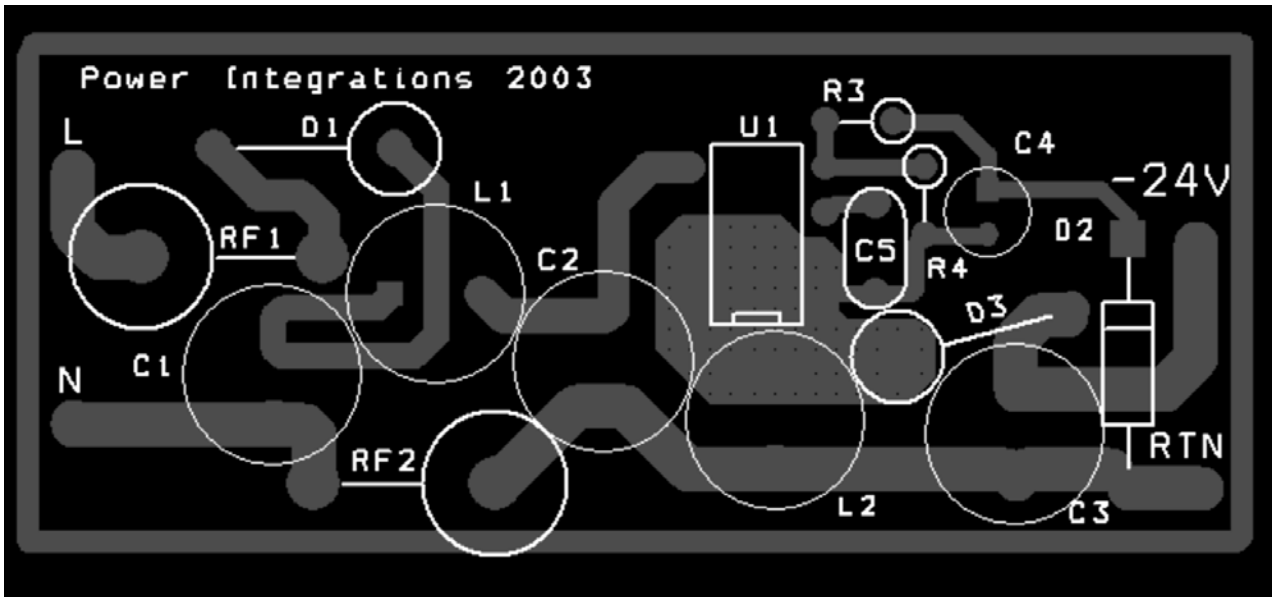
## 4 Circuit Description

The circuit shown in Figure 2 is a non-isolated buck-boost (inverting) topology. The input voltage range is 85 to 135 VAC 50/60Hz and provides a regulated  $-24\text{ V}$  at 200 mA. The buck-boost topology is essentially the non-isolated version of the Flyback Converter, in that the transformer is replaced with a single low cost inductor (L2).

RF1 is a fusible link resistor. The input AC is half-wave rectified and filtered by D1 and C1. C1, L1 and C2 form a pi-filter network to reduce common-mode emissions imposed to the input line, this in conjunction with the built-in frequency jitter of the LinkSwitch-TN (U1) ensure sufficient conducted EMI margins. U1, D2 and L2 form the buck-boost switching cell, which converts the rectified bulk positive DC voltage on C2 into a negative voltage on C3 (w/r/t Neutral/GND). D2 samples the output voltage onto C4 as a positive voltage with respect to the source of U1. The EN pin of U1 is internally set to 1.63 V (w/r/t pins 1,2, 7 and 8) this in conjunction with resistors R3 and R4 form a simple voltage divider to precisely set the output voltage to the desired level. C5 is a bypass capacitor that serves as high frequency decoupling and energy storage. This capacitor provides power to the IC as well as controls the auto-restart mechanism in the LinkSwitch-TN. Resistor R2 serves to reduce peak charging effects on C3 which tend to increase the output voltage, its static power dissipation is limited to less than 30 mW. Without this additional resistor the standby power consumption would be less than 100 mW.



### 5 PCB Layout



(RF2 not used)

Figure 3 – Printed Circuit Layout.



## 6 Bill Of Materials

Item	Qty	Ref Des	Value	Manufacturer	P/N
1	2	C1, C2	10uF/250V	Panasonic	ECA-2EM100
2	1	C3	47uF/35V		
3	1	C4	100uF/16V		
4	1	C5	1uF/50V		
5	2	D1, D2	Standard Rec. 1A/400V	Diodes, Inc.	1N4004GP
6	1	D3	Fast Recovery 1A/400V	Diodes, Inc.	1N4936
7	1	L1	2.2mH	Toko	262LY-222K
8	1	L2	1800uH	Toko	824MY-182K
9	1	R2	22k 5% 1/4W		
10	1	R3	20.5k 1% 1/8W		
11	1	R4	1.54k 1% 1/8W		
12	1	RF1	47 ohm/2W	RCD Components	
13	1	U1	PWM +MOSFET	Power Integrations	LNK306P





## 7 Performance Data

All measurements performed at room temperature, 60 Hz input frequency.

### 7.1 Efficiency

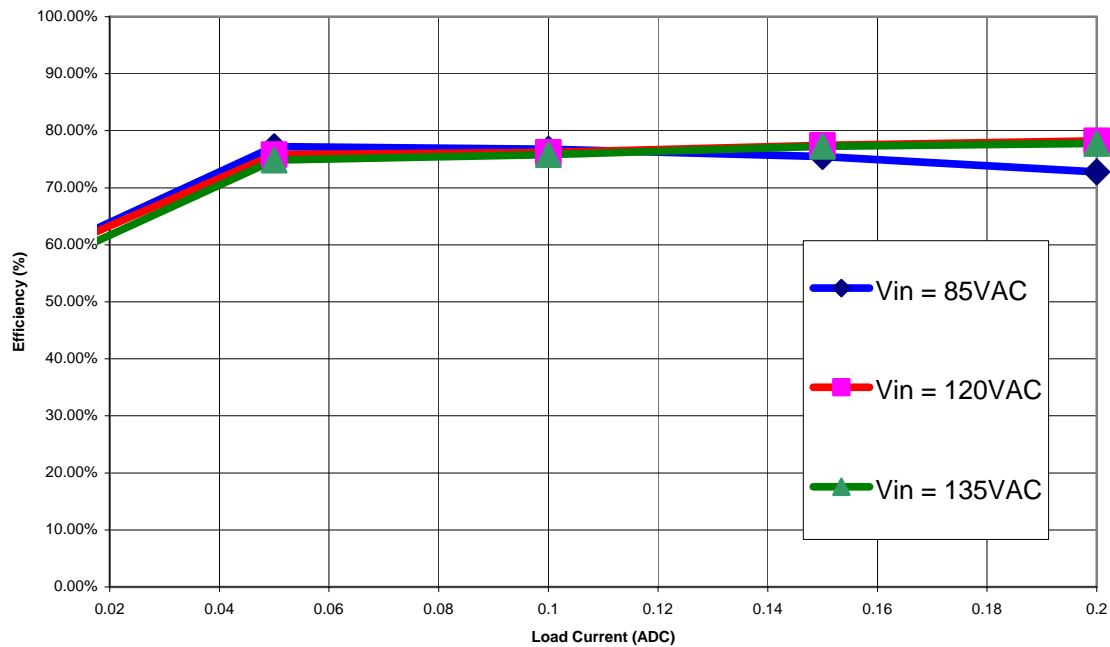


Figure 4 – Efficiency vs. Input Voltage.

### 7.2 Standby Power Consumption

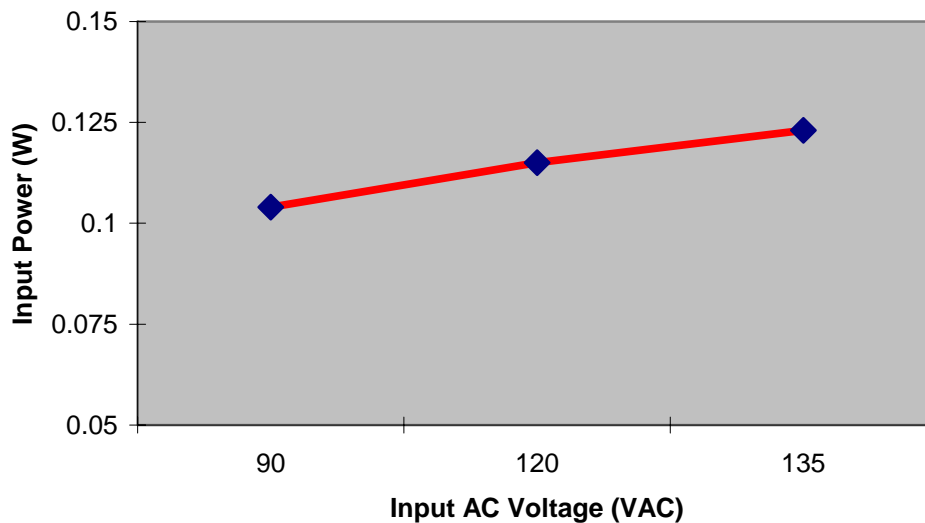


Figure 5 – Standby Power Consumption vs. Input Voltage.



### 7.3 Line/Load Regulation

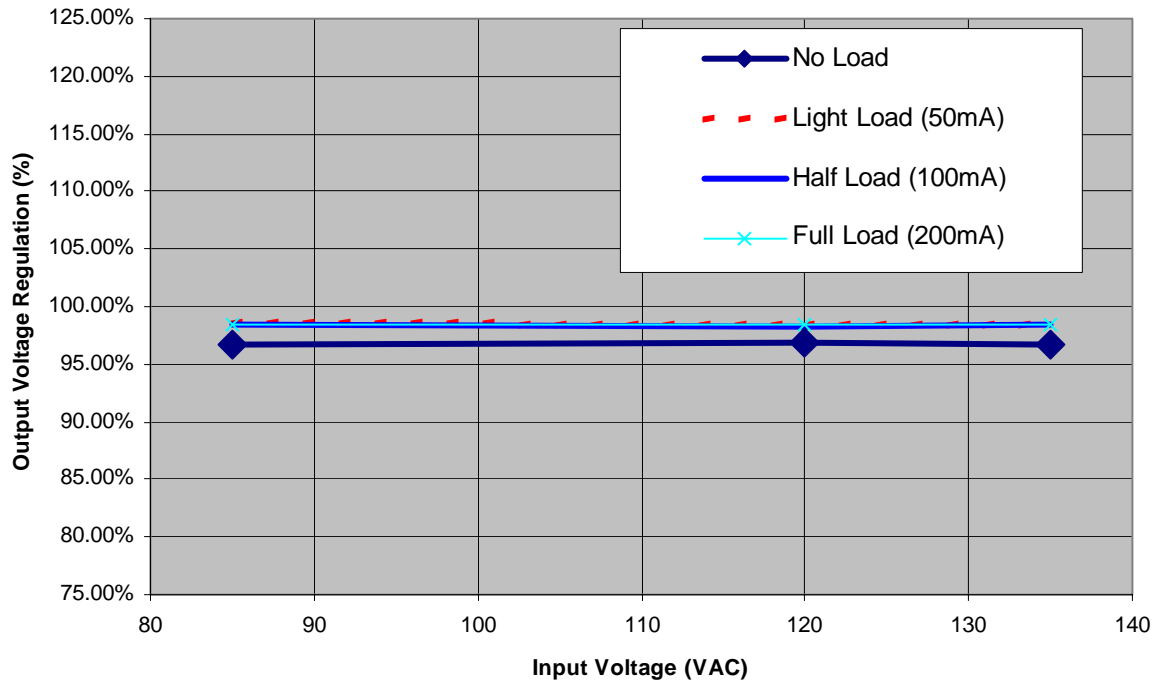
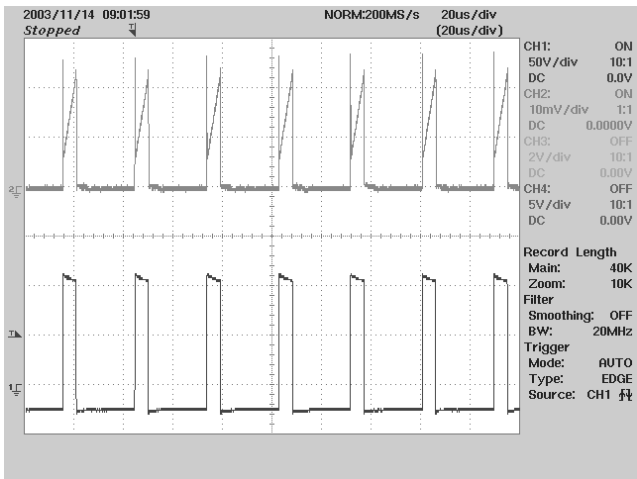


Figure 6 – Line/Load Regulation, Room Temperature.

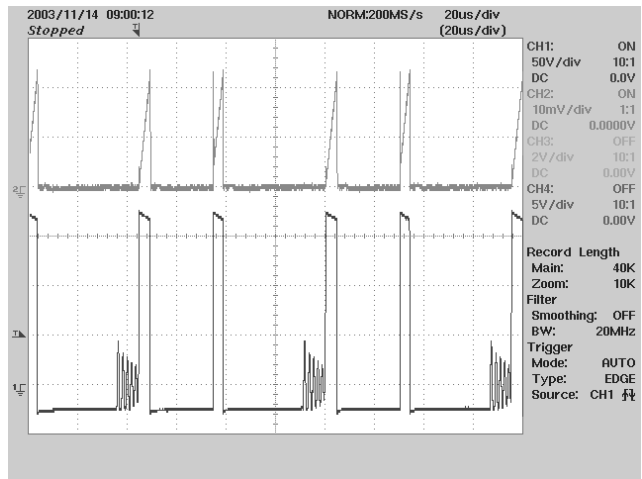


## 8 Waveforms

### 8.1 Switch Node Voltage and LinkSwitch-TN Drain Current, Normal Operation

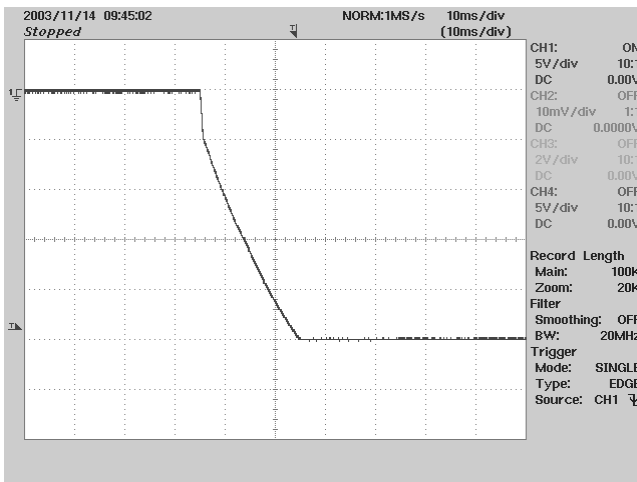


**Figure 7** – 85VAC, Full Load.  
Upper:  $I_{DRAIN}$ , 0.2 A / div  
Lower:  $V_{Switch-Node}$ , 50 V, 2  $\mu$ s / div

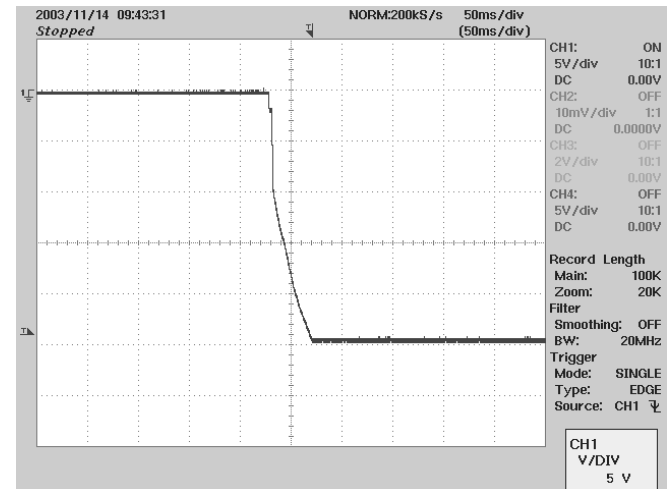


**Figure 8** – 135VAC, Full Load  
Upper:  $I_{DRAIN}$ , 0.2 A / div  
Lower:  $V_{Switch-Node}$ , 50 V / div

### 8.2 Output Voltage Start-up Profile



**Figure 9** – Start-up Profile, 120VAC (No Load)  
5 V, 10 ms / div.

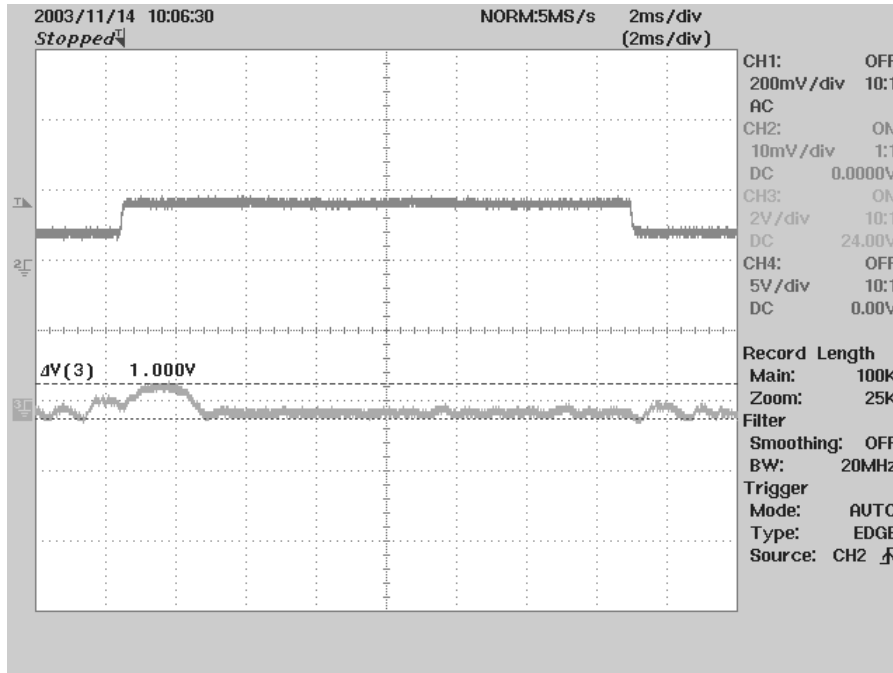


**Figure 10** – Start-up Profile, 120 VAC (Full Load)  
5 V, 50 ms / div.



### 8.3 Load Transient Response (50% to 100% Load Step)

In the figures shown below, signal averaging was used to better enable viewing the load transient response. The oscilloscope was triggered using the load current step as a trigger source. Since the output switching and line frequency occur essentially at random with respect to the load transient, contributions to the output ripple from these sources will average out, leaving the contribution only from the load step response.



**Figure 11** – Transient Response, 120 VAC, 50-100-50% Load Step.

Top: Load Current, 0.2 A/div.

Bottom: Output Voltage

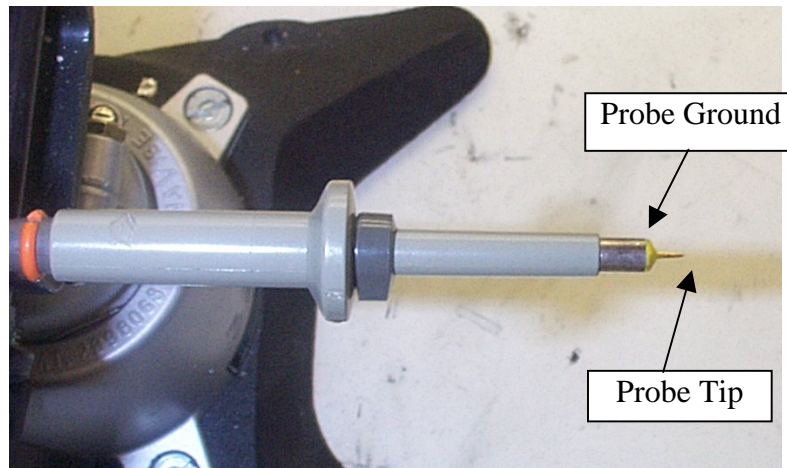
2V (24V Offset), 2ms / div.

## 8.4 Output Ripple Measurements

### 8.4.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in Figure 12 and Figure 13.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1  $\mu\text{F}/50\text{ V}$  ceramic type and one (1) 1.0  $\mu\text{F}/50\text{ V}$  aluminum electrolytic. ***The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).***



**Figure 12** – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)



**Figure 13** – Oscilloscope Probe with Probe Master 5125BA BNC Adapter. (Modified with wires for probe ground for ripple measurement, and two parallel decoupling capacitors added)

8.4.2 Measurement Results

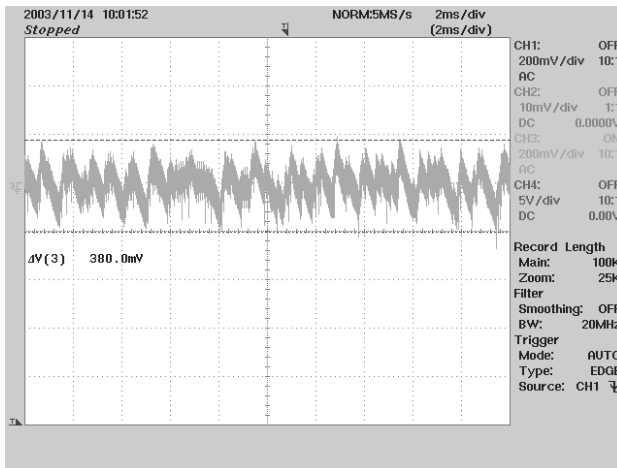


Figure 14 – Ripple, 85VAC, Full Load.  
2 ms, 200 mV / div

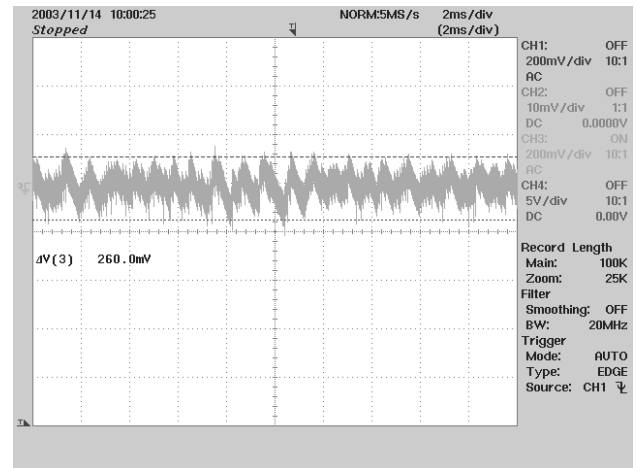


Figure 15 – Ripple, 135VAC, Full Load.  
2 ms, 200 mV / div



### 9 Conducted EMI

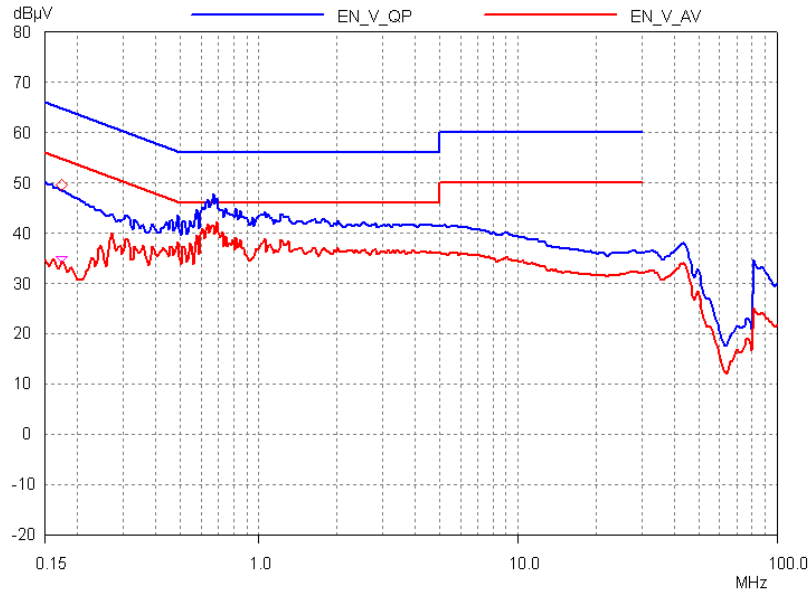


Figure 16 – Conducted EMI EN5022 B Limits - 120 VAC/60Hz Maximum Steady State Load (LINE)

Note: If more EMI margin is desired, an additional 1N4007 can be added in series with the NEUTRAL input

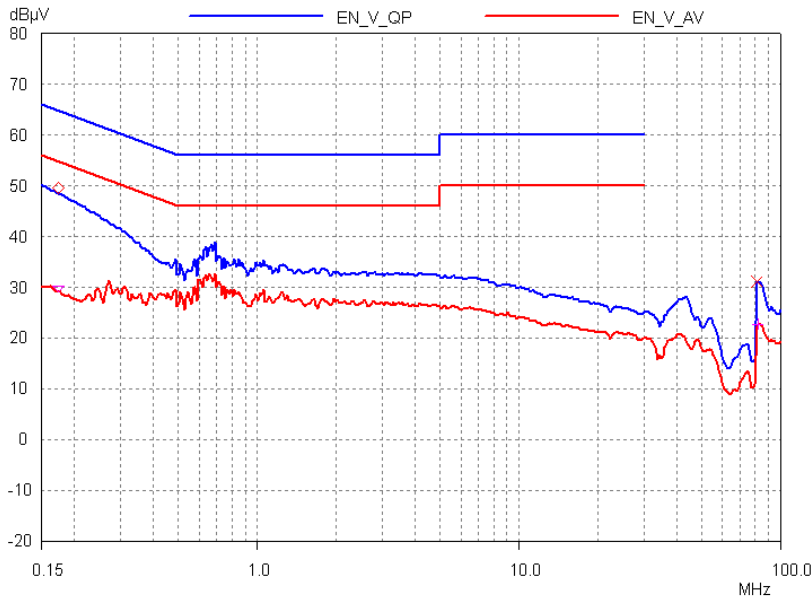


Figure 17 – Conducted EMI EN5022 B Limits - 120 VAC/60Hz Maximum Steady State Load (Neutral)



## 10 Revision History

<b>Date</b>	<b>Author</b>	<b>Revision</b>	<b>Description &amp; changes</b>	<b>Reviewed</b>
May 4, 2005	RSP	1.0	Initial Release	VC / AM
June 6, 2006	PV/SF	1.1	Updated tolerance in Section 2 from 5% to 10%. Adjusted output voltages accordingly.	KM





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