DFP Vishay Dale



Thick Film Resistor Networks Flat Pack, 11, 12 Schematics

FEATURES

- 11 and 12 Schematics
- 0.065" [1.65mm] height for high density packaging
- Low temperature coefficient (- 55°C to + 125°C) ± 100ppm/°C
- Hot solder dipped leads
- · Highly stable thick film
- Wide resistance range

 All devices are capable of passing the MIL-STD-202, Method 210, Condition C "Resistance to Soldering Heat" test

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STANDARD ELECTRICAL SPECIFICATIONS

	POWER RATING			LIMITING ELEMENT			DESISTANCE	TEMPERATURE
GLOBAL MODEL	P _{25°C} ELEMENT W	P _{25°C} PACKAGE W	CIRCUIT SCHEMATIC	VOLTAGE MAX. V≌	COEFFICIENT ppm/°C	TOLERANCE %	RANGE Ω	COEFFICIENT TRACKING ppm/°C
DED	0.25	0.65	11	75	± 100	2	10 - 1M	50
	0.15	0.65	12	75	± 100	2	10 - 1M	50
¹⁾ Temperature Range: - 55°C to + 125°C ²⁾					²⁾ ± 1% and ± 5%	tolerance availa	able	

¹⁾Temperature Range: - 55°C to + 125°C

· Consult factory for stocked values

TECHNICAL SPECIFICATIONS 11 Schematic 7 or 8 isolated resistors The DFPxx11 provides the user with 7 or 8 nominally equal resistors with each resistor isolated from all others. Commonly used in the following applications: • "Wired OR" Pull-up • Long-line Impedance Balancing • Power Driven Pull-up • LED Current Limiting • Power Gate Pull-up • ECL Output Pull-down Line Termination • TTL Input Pull-down **12 Schematic** 13 or 15 resistors with one pin common The DFPxx12 provides the user with a choice of 13 or 15 nominally equal resistors, each connected to a common pin (14 or 16). Commonly used in the following applications: MOS/ROM Pull-up/Pull-down TTL Input Pull-down Open Collector Pull-up • Digital Pulse Squaring -DFP1412 -• "Wired OR" Pull-up • TTL Unused Gate Pull-up DFP1612 • High Speed Parallel Pull-up • Power Driven Pull-up





DIMENSIONS in inches [millimeters]





Model number, schematic number, value tolerance, pin 1 indicator, date code.

Per MIL-STD-1276 DFPxx11, DFPxx12 = Type G (hot solder dipped). Hot solder dipped leads supplied as standard finish.

Permanency testing per MIL-STD-202

Per MIL-STD-202, Method 208E.

Epoxy filled ceramic sandwich

MECHANICAL SPECIFICATIONS

Package

Single Resistor

+ 25

+ 70

Ambient Temperature °C

+ 125 + 150

Method 215.

Marking:

to Solvents: Solderability:

Terminals:

12 Schematic

Power Rating (Watts)

0.65

0.50

0.15

- 55

Body:

Derating

Marking Resistance

TECHNICAL SPECIFICATIONS					
PARAMETER	UNIT	DFP14 / 16			
Isolation Resistance 11 Schematic	MΩ	> 100			
Voltage Coefficient of Resistance:	ppm/V	< 50 typical			
Maximum Operating Voltage:	VDC	75			
Operating Temperature Range:	°C	- 55 to + 125			
Storage Temperature Range:	°C	- 55 to + 150			

11 Schematic



Derating

PERFORMANCE

PERFORMANCE		
TEST	CONDITIONS	MAX. ∆R (Typical Test Lots)
Power Conditioning	1.5 x rated power, applied 1.5 hours "ON" and 0.5 hour "OFF" for 100 hours \pm 4 hours at + 25°C ambient temperature	± 0.50% ∆R
Thermal Shock	5 cycles between - 65°C and + 125°C	± 0.50% ΔR
Short Time Overload	2.5 x rated working voltage, 5 seconds	± 0.25% ΔR
Low Temperature Operation	45 minutes at full rated working voltage at - 65°C	± 0.25% ΔR
Moisture Resistance	240 hours with humidity ranging from 80% RH to 98% RH	± 0.50% ΔR
Resistance to Soldering Heat	Leads immersed in + 260° Δ C solder to within 1/16" of body for 10 seconds	± 0.25% ΔR
Shock	Total of 18 shocks at 100 G's	± 0.25% ΔR
Vibration	12 hours at maximum of 20 G's between 10 and 2,000 Hz	± 0.25% ∆R
Load Life	1000 hours at + 70°C, rated power applied 1.5 hours "ON", 0.5 hour "OFF" for full 1000 hour period. Derated according to the curve.	± 0.50% ΔR
Terminal Strength	1.5 pound pull for 30 seconds	± 0.25% ∆R
Insulation Resistance	10,000 Megohm (minimum)	-
Dielectric Withstanding Voltage	No evidence of arcing or damage (200 V RMS for 1 minute)	_