Design Idea DI-69
DPA-Switch™ 15 W Multi-Output DC-DC Converter

Application	Device	Power Output	Input Voltage	Output Voltage	Topology
VoIP Phone	DPA424P	15 W	36-75 VDC	5 V / 7.5 V / 20 V	Forward

Design Highlights

- Low component count
- Built-in accurate OV/UV with single resistor programming
- High efficiency (88%) using synchronous rectification
- Multiple outputs with good cross-regulation
- Built-in output overload, open loop and thermal protection
- 400 kHz switching frequency
- No primary current sense resistor required

Operation

Resistor R1 programs the input under/over voltages to 33 V and 86 V. It also linearly reduces the maximum device duty cycle (DC_{MAX}) with increasing input voltage, helping to prevent core saturation during transients.

Capacitor C1, C2 and L1 provide line filtering. Resistor R2 programs the U1 current limit. The Q22 reflected gate capacitance provides optimum reset for transformer T1. Zener VR1 clamps the peak drain voltage to a safe level during transient conditions.

Resistors R21, R22, C21 and MOSFETs Q21 and Q22 form a capacitively coupled direct driven synchronous rectifier for the main (5 V) output. Zener diode VR21 acts both as a clamp and as a diode to quickly recharge the Q21 drive capacitor C21. Resistor R23 holds Q21 off when no switching signal is present.

The 20 V output is generated from a flyback winding on the L2 inductor, which is rectified and filtered by diode D41 and C41. Zener VR31 and diode D32 provide a pre-load on the 7.5 V output to enhance regulation at light load.

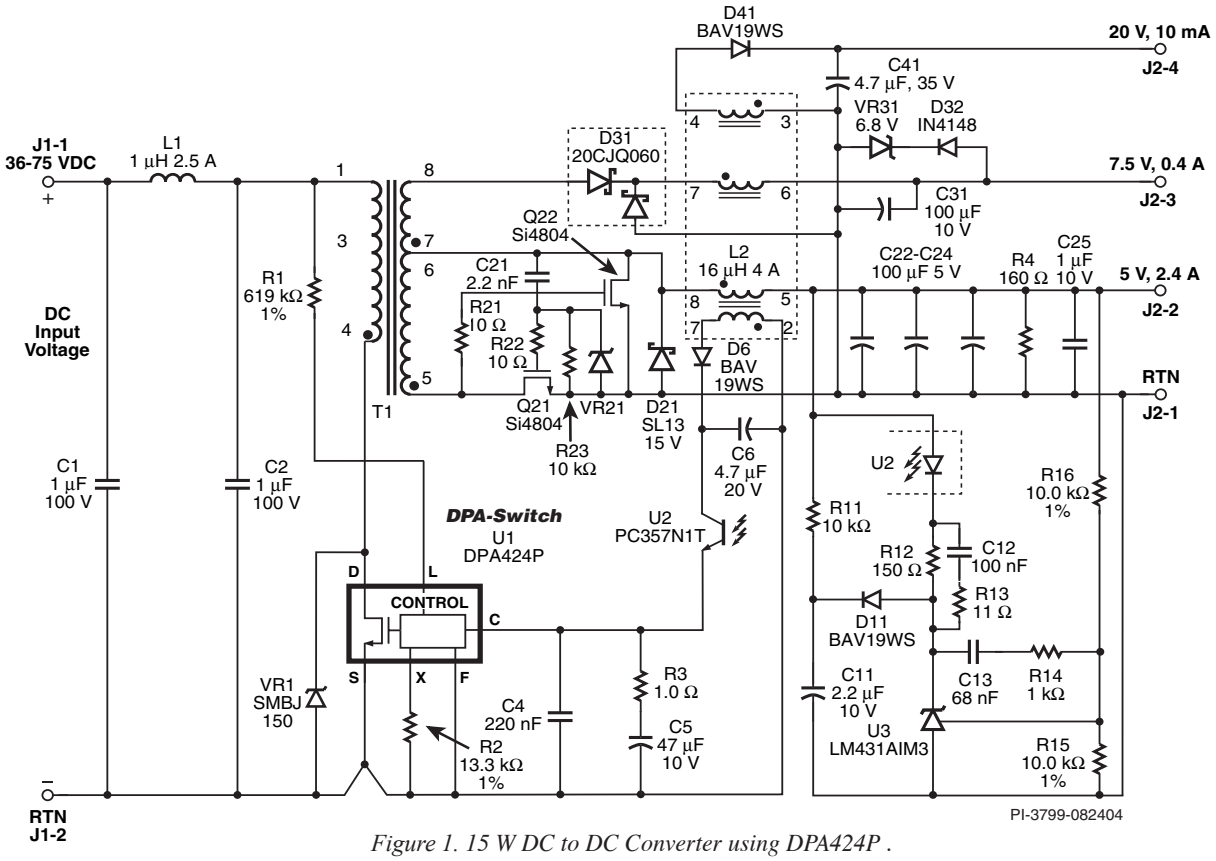

Figure 1. 15 W DC to DC Converter using DPA424P .

Key Design Points

- Zener VR1 safely limits the DRAIN voltage below BV_{DSS}.
- At zero load, maximum input voltage, the bias voltage across C6 should be >8 V (12 V to 15 V under normal conditions).
- The 5 V output is the regulated output. All other outputs are derived from it. Therefore, tight transformer secondary coupling and low PC board trace impedance from the 5 V output to the 7.5 V output are crucial to achieve good cross-regulation.
- The transformer must reset completely under all line and load conditions to prevent core saturation. The gate capacitance of Q22 (with other parasitic circuit capacitances), determines the minimum reset period. The transformer core reset voltage also drives the secondary synchronous rectifier Q22. Efficiency is maximized when Q22 conduction period is maximized. This Q22 conduction period can be extended by adding more capacitance (an R-C snubber across the 5 V winding). The reset period should be set to give as long a reset as possible when operating at low-line (maximum duty cycle) while still guaranteeing complete reset.
- Good layout practices should be followed:
  - Locate C4, C5 and R3 close to U1 with grounds returned to the SOURCE pin.
  - Minimize the primary and secondary loop areas to reduce parasitic leakage inductance.
  - Locate D21 and Q22 return connections very close to each other to provide best cross-regulation between 5 V and 7.5 V.

V_{OUT}	Voltage Range (VDC)	Load Range (%)	Cross-Regulation (%)													
			-6	-5	-4	-3	-2	-1	0	1	2	3	4	5	6	7	8
5	36-72	20-100															
7.5	36-72	0-100															
7	36-72	100															

Table 1. Worst Case Output Cross-Regulation - All Outputs Taken from Minimum to Maximum Load.

TRANSFORMER PARAMETERS	
Core Material	Ferroxcube P/N: PTS14/8-3F3, ungapped
Bobbin	8 pin P1408 surface mount B&B B-096 or equivalent
Winding Details	Primary: 8T + 7T, 27 AWG, 5 V 4T, 4 x 28 AWG 7.5 V 2T, 4 x 28 AWG
Winding Order (pin numbers)	Primary-1 (4-3), 7.5 V (7-8), 5 V (5-6) Primary-2 (3-1)
Primary Inductance	434 µH ±25% @ 100 kHz
Primary Resonant Frequency	3.8 MHz (minimum)
Leakage Inductance	1 µH (maximum)

Table 2. Transformer Design Parameters.

INDUCTOR PARAMETERS	
Core Material	Epcos N87, P/N: B65755-J-R87, Gap for A_L = 160 nH/T^2
Bobbin	8 pin P1408 surface mount B&B B-096 or equivalent
Winding Details	Bias 26T, 34 AWG 5 V 6T, 2 x 28 AWG 7.5 V 12T, 28 AWG 20 V 40T, 34 AWG
Winding Order (pin numbers)	7.5 V (7-6), 5 V (8-5), 20 V (1-2), Bias (4-3)
Inductance	Pin (5-8): 16 µH ±10% @ 100 kHz

Table 3. Inductor Design Parameters.

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