Rev: 072707

DS34T101/DS34T102/DS34T104/DS34T108
Single/Dual/Quad/Octal TDM-Over-Packet Chip

General Description

The IETF PWE^3 SAToP/CESoPSN/TDMoIP/HDLC draft-compliant DS34T108 allows up to eight T1/E1 links or frame-based serial HDLC links to be transported transparently through a switched IP or MPLS packet network. Jitter and wander of recovered clocks conform to G.823/G.824, G.8261, and TDM specifications. This eliminates the need for remote timing sources in cabinets and pedestals.

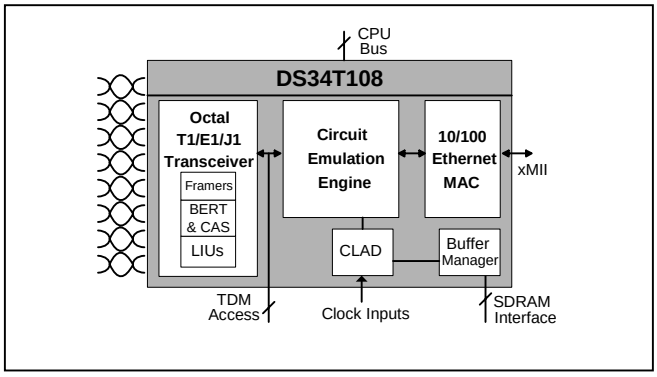
The Ethernet side of the DS34T108 provides high QoS capabilities to its MII/RMII/SSMII port, while the WAN side supports full-featured T1/E1 framers and LIUs. This takes the solution all the way through analog, while preserving options to make use of TDM streams at key intermediate points. The high level of integration that the DS34T108 brings minimizes cost, board space, and time to market.

Applications

TDM Circuit Extension Over PSN
- o Leased—Line Services Over PSN
- o TDM Over G/E—PON
- o TDM Over Cable
- o TDM Over WiMAX

Cellular Backhaul Over PSN
Multiservice Over Unified PSN
HDLC—Based Traffic Transport Over PSN

Functional Diagram



Features

- ♦ **Full-Featured T1/E1/J1 LIU/Framer/TDM-Over-Packet**
- ♦ **Supports Adaptive Clock Recovery, Common Clock (Using RTP), External Clock, and Loopback Timing Modes**
- ♦ **Selectable 32-Bit or 16-Bit Processor Bus**
- ♦ **Clock Rate Adapter for T1/E1 Master Clock**
- ♦ **10/100 Ethernet MAC That Supports MII/RMII/SSMII**
- ♦ **Fully Compatible with IEEE 802.3 Standard**
- ♦ **VLAN Support According to 802.1 p&Q**
- ♦ **Multiprotocol Encapsulation Supports IPv4, IPv6, UDP, RTP, L2TPv3, MPLS, and Metro Ethernet**
- ♦ **End-to-End TDM Synchronization Through the IP/MPLS Domain by Eight Independent On-Chip TDM Clock Recovery Mechanisms**
- ♦ **Single Serial Support for RS-530 and V.35**
- ♦ **Single DS3/E3/STS-1 to Ethernet**
- ♦ **Packet Loss Compensation and Handling of Misordered Packets**
- ♦ **64 Independent Bundle/Connections**
- ♦ **Glueless SDRAM Buffer Management**
- ♦ **1.8V Core, 3.3V I/O**
- ♦ **Complies with IETF PWE3 RFCs and Drafts for CESoPSN, SAToP, TDMoIP, and HDLC**

Features continued in Section 7.

Ordering Information

PART	PORTS	TEMP RANGE	PIN-PACKAGE
DS34T108GN	8	-40°C to +85°C	484 HSBGA
DS34T108GN+	8	-40°C to +85°C	484 HSBGA
DS34T104GN*	4	-40°C to +85°C	484 TEBGA
DS34T104GN+*	4	-40°C to +85°C	484 TEBGA
DS34T102GN*	2	-40°C to +85°C	484 TEBGA
DS34T102GN+*	2	-40°C to +85°C	484 TEBGA
DS34T101GN*	1	-40°C to +85°C	484 TEBGA
DS34T101GN+*	1	-40°C to +85°C	484 TEBGA

+Denotes a lead-free package.
**Future product—Contact factory for availability.*

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1. Introduction

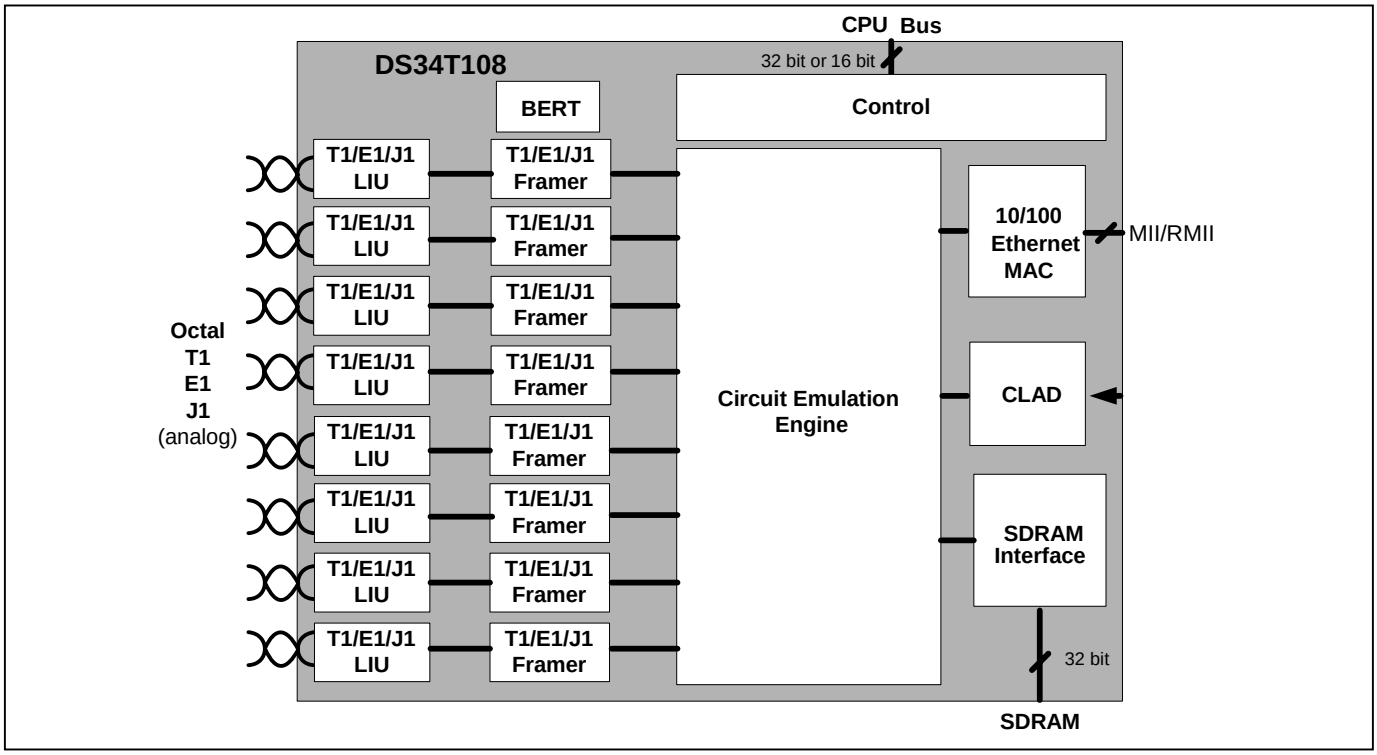
The DS34T108/DS34T104/DS34T102/DS34T101 (DS34T10x) family of products combines LIU, framer, and Pseudo Wire Emulation Edge-to-Edge (PWE3) circuit emulation technology into one die. Dedicated payload-type engines are included for TDMoIP (AAL1, AAL2), CESoPSN, SAToP, and HDLC.

Products in the DS34T10x family provide a transport technology for simple conversion of T1/E1/J1/T3/E3/STS-1 serial TDM to IP, MPLS, or pure Ethernet Layer 2 networks. They carry from the line E1/T1/J1 or they provide a carrier for E3, T3, or STS1 services and serial data across a packet-switched network, transparent to all protocols and signaling. These products enable service providers to migrate to next-generation networks while continuing to provide all their revenue-generating legacy voice and data services. They also benefit data carriers by enabling them to offer lucrative leased-line services and increase revenues from their packet-switched infrastructure by selling voice as well as data services. Finally, they enable enterprises to run voice and video over the same IP/Ethernet-based network that is currently used to run only LAN traffic, thereby minimizing network maintenance and operating costs.

Packet-switched networks, such as IP networks, were not designed to transport TDM data and have no inherent clock distribution mechanism. Hence, when transporting TDM over packet-switched networks, the receiver needs to reconstruct the transmitter's TDM clock. The DS34T10x family ensures that jitter and wander levels of the recovered clock conform to ITU-T G.823/824 and G.8261, even for networks that introduce significant packet delay variation and packet loss.

The Circuit Emulation technology in the DS34T10x products that makes this possible is called TDM-over-Packet (TDMoP) and complements VoIP in those cases where VoIP is not applicable or where VoIP price/performance is not sufficient. Most importantly, TDMoP technology provides higher voice quality with lower latency than VoIP. Unlike VoIP, TDMoP can support all applications that run over E1/T1/J1 circuits, not just voice. TDMoP can provide traditional leased-line services over IP and is transparent to protocols and signaling. Because TDMoP provides an evolutionary, as opposed to revolutionary, approach, investment protection is maximized.

Figure 1-1. Block Diagram



2. Acronyms and Glossary

Listed below are the terms used in this data sheet.

2.5G	2.5 Generation
2G	Second Generation
3G	Third Generation
AAL1	ATM Adaptation Layer 1
AAL2	ATM Adaptation Layer 2
ATM	Asynchronous Transfer Mode
BGA	Ball Grid Array
Bridge	Bridge
Bundle	Bundle
BW	Bandwidth
CAS	Channel Associated Signaling
CCS	Common Channel Signaling
CE	Customer Edge
CESoP	Circuit Emulation Service over Packet
CESoPSN	Circuit Emulation Services over Packet Switched Network
Circuit Switching	Circuit Switching
CLAD	Clock Rate Adapter
CLEC	Competitive Local Exchange Carrier
CPE	Customer Premises Equipment
CSMA	Carrier Sense Multiple Access
CSMA/CD	Carrier Sense Multiple Access with Collision Detection
DS0	Digital Signal Level 0
DS1	Digital Signal 1
DS3	Digital Signal 3
HDLC	High-Level Data Link Control
IEEE 802.3	Institute of Electrical and Electronics Engineers 802.3
IEEE 802.X	Institute of Electrical and Electronics Engineers 802.X
IETF	Internet Engineering Task Force
ILEC	Incumbent Local Exchange Carrier
IP	Internet Protocol
IP Address	Internet Protocol Address
IWF	Interworking Function
LAN	Local Area Network
LEC	Local Exchange Carrier
LIU	Line Interface Unit
MAC	Media Access Control
MAN	Metropolitan Area Network
Message Switching	Message Switching
MII	Medium Independent Interface
MPLS	Multiprotocol Label Switching
OC-3	Optical Carrier Level 3
OCXO	Oven-Controlled Crystal Oscillator
OFE	Optical Front-End
OSI	Open Systems Interconnection
OSI-RM	Open Systems Interconnection—Reference Model
PAD	Packet Assembler/Disassembler
PBX	Private Branch Exchange
PCI	Peripheral Component Interconnect
PCI Express	Peripheral Component Interconnect Express
PCI-X	Peripheral Component Interconnect Extended
PDV	Packet Delay Variation
PE	Provider Edge

PLCC	Plastic Leaded Chip Carrier
PQFP	Plastic Quad Flat Pack
PSN	Packet Switched Network
PSTN	Public Switched Telephone Network
PWE3	Pseudo-Wire Edge-to-Edge Emulation
QoS	Quality of Service
RMII	Reduced Medium Independent Interface
RPR	Resilient Packet Ring
SAToP	Structure-Agnostic TDM over Packet
SDH	Synchronous Digital Hierarchy
SMII	Serial Media Independent Interface
SONET	Synchronous Optical Network
SS7	Signal System 7
SSMII	Source Synchronous Serial Media Independent Interface
STM-1	Synchronous Transfer Module -1
TDM	Time Division Multiplexing
TDMoIP	Time Division Multiplexing over Internet Protocol
TDMoP	Time Division Multiplexing over Packet
TLS	Transport Layer Security
UDP	User Datagram Protocol
VoIP	Voice over IP
VPLS	Virtual Private LAN Services
WAN	Wide Area Network

3. Standards Compliance

The DS34T108 meets all the latest relevant telecommunications specifications. Table 3-1 and Table 3-2 provide the T1 and E1 specifications and sections that are applicable to the DS34T108. The TDM-over-Packet specifications and sections relevant for the DS34T108 are described in Table 3-3.

Table 3-1. T1-Related Telecommunications Specifications

ANS*I T1.102- Digital Hierarchy Electrical Interface.*
AMI Coding.
B8ZS Substitution Definition.
DS1 Electrical Interface. Line rate ±32ppm; pulse amplitude between 2.4V to 3.6V peak; power level between 12.6dBm to 17.9dBm; the T1 pulse mask is provided that we comply. DSX-1 for cross-connects the return loss is greater than -26dB. The DSX-1 cable is restricted up to 655 feet.
This specification also provides cable characteristics of DSX-Cross Connect cable—22 AVG cables of 1000 feet.
ANSI T1.231- Digital Hierarchy- Layer 1 in Service Performance Monitoring
BPV Error Definition; Excessive Zero Definition; LOS description; AIS definition.
ANSI T1.403- Network and Customer Installation Interface- DS1 Electrical Interface
Description of the Measurement of the T1 Characteristics—100Ω. Pulse shape and template compliance according to T1.102; Power level 12.4dBm to 19.7dBm when all ones is transmitted.
LBO for the Customer Interface (CI) is specified as 0dB, -7.5dB and -15dB. Line rate is ±32ppm. Pulse Amplitude is 2.4V to 3.6V.
AIS generation as unframed all ones is defined.
The total cable attenuation is defined as 22dB. The DS34T108 will function with up to -36dB cable loss.
Note that the pulse template defined by T1.403 and T1.102 are different, specifically at times 0.61, -0.27, -34, and 0.77. The DS34T108 is complaint to both templates.
Pub 62411
This specification has tighter jitter tolerance and transfer characteristics than other specifications. The jitter transfer characteristics are tighter than G.736 and jitter tolerance is tighter than G.823.
(ANSI) “Digital Hierarchy – Electrical Interfaces”
(ANSI) “Digital Hierarchy – Formats Specification”
(ANSI) “Digital Hierarchy – Layer 1 In-Service Digital Transmission Performance Monitoring”
(ANSI) “Network and Customer Installation Interfaces – DS1 Electrical Interface”
(AT&T) “Requirements for Interfacing Digital Terminal Equipment to Services Employing the Extended Super frame Format”
(AT&T) “High Capacity Digital Service Channel Interface Specification”
(TTC) “Frame Structures on Primary and Secondary Hierarchical Digital Interfaces”
(TTC) “ISDN Primary Rate User-Network Interface Layer 1 Specification”

Table 3-2. E1-Related Telecommunications Specifications

ITUT G.703 Physical/Electrical Characteristics of G.703 Hierarchical Digital Interfaces
Defines the 2048kbps bit rate—2048 ±50ppm; The transmission media are 75Ω coax or 120Ω twisted pair; peak to peak space voltage is ±0.237V; Nominal pulse width is 244ns.
Return loss 51 to 102Hz is 6dB, 102 to 3072Hz is 8dB, 2048 to 3072Hz is 14dB.
Nominal peak voltage is 2.37V for coax and 3V for twisted pair.
The pulse template for E1 is defined in G.703.
ITUT G.736 Characteristics of Synchronous Digital Multiplex Equipment operating at 2048Kbit/s
The peak-to-peak jitter at 2048kbps must be less than 0.05UI at 20Hz to 100Hz.
Jitter transfer between 2.048 synchronization signal and 2.048 transmission signal is provided.
ITUT G.775
A LOS detection criterion is defined.
ITUT G.823 The control of jitter and wander within digital networks which are based on 2.048Kbit/s hierarchy
G.823 provides the jitter amplitude tolerance at different frequencies, specifically 20Hz, 2.4kHz, 18kHz, and 100kHz.
ETSI 300 233
This specification provides LOS and AIS signal criteria for E1 mode.
Pub 62411
This specification has tighter jitter tolerance and transfer characteristics than other specifications. The jitter transfer characteristics are tighter than G.736 and jitter tolerance is tighter than G.823.
(ITU) “Synchronous Frame Structures used at 1544, 6312, 2048, 8488 and 44736Kbit/s Hierarchical Levels”
(ITU) “Frame Alignment and Cyclic Redundancy Check (CRC) Procedures Relating to Basic Frame Structures Defined in Recommendation G.704”
(ITU) “Characteristics of primary PCM Multiplex Equipment Operating at 2048Kbit/s”
(ITU) Characteristics of a synchronous digital multiplex equipment operating at 2048Kbit/s”
(ITU) “Loss Of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria”
(ITU) “The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048Kbit/s Hierarchy”
(ITU) “Primary Rate User-Network Interface – Layer 1 Specification”
(ITU) “Error Performance Measuring Equipment Operating at the Primary Rate and Above”
(ITU) “In-service code violation monitors for digital systems”
(ETSI) “Integrated Services Digital Network (ISDN); Primary rate User-Network Interface (UNI); Part 1/ Layer 1 specification”
(ETSI) “Transmission and multiplexing; Physical/electrical characteristics of hierarchical digital interfaces for equipment using the 2048Kbit/s-based plesiochronous or synchronous digital hierarchies”
(ETSI) “Integrated Services Digital Network (ISDN); Access digital section for ISDN primary rate”
(ETSI) “Integrated Services Digital Network (ISDN); Attachment requirements for terminal equipment to connect to an ISDN using ISDN primary rate access”
(ETSI) “Business Telecommunications (BT); Open Network Provision (ONP) technical requirements; 2048Kbit/s digital unstructured leased lines (D2048U) attachment requirements for terminal equipment interface”
(ETSI) “Business Telecommunications (BTC); 2048Kbit/s digital structured leased lines (D2048S); Attachment requirements for terminal equipment interface”
(ITU) “Synchronous Frame Structures used at 1544, 6312, 2048, 8488 and 44736Kbit/s Hierarchical Levels”
(ITU) “Frame Alignment and Cyclic Redundancy Check (CRC) Procedures Relating to Basic Frame Structures Defined in Recommendation G.704”

Table 3-3. TDM-over-Packet Related Specifications

Y.1413 TDM-MPLS network interworking – User plane interworking
TDMoMPLS will meet standards for network interworking that covers the Transport label, Interworking label, Common interworking indicators, and Optional timing information. The Common interworking indicators include a Control Field, a Fragmentation Field, Length Indicator and the Sequence number.
TDMoMPLS shall meet standards for Structure Agnostic transport.
TDMoMPLS shall meet standards for Structure Aware transport that contains Structure-locked encapsulation and Structure-indicated encapsulation.
Y.1414 Voice Service – MPLS network interworking
The recommendation focuses on the required functions and procedures necessary for support of narrow-band voice services by MPLS networks. Details of the encapsulation of encoded audio streams in MPLS packets are specified. Clause 10 draft recommendation shall be met.
Y.1452 (Y.VTOIP) Voice trunking over IP
This recommendation specifies a method for transporting multiplexed voice services over UDP/IP.
Y.1453 (Y.TDMIP) TDM-IP interworking – User plane interworking
This recommendation specifies methods for transporting low-rate TDM (T1, E1, T3, E3) over UDP/IP. Y.1453 is a direct extension of Y.1413.
PWE3-CESoPSN Structure-aware TDM Circuit Emulation Service over Packet Switched Network
May 2006 '*draft-ietf-pwe3-cesopsn-07.txt*' revision shall be supported.
The TDM-over-Packet shall meet Basic NxDS0 service, and "Trunk-specific" NxDS0 service with CAS.
The TDM-over-Packet shall meet CESoPSN packet format for an IPv4/IPv6 PSN, CESoPSN Packet Format for an MPLS PSN. Shall also meet CESoPSN Payload Layer.
PWE3-SAToP Structure-Agnostic TDM over Packet
June 2006 '*rfc4553.txt*' revision shall be supported.
The TDM-over-Packet shall meet Basic SAToP Packet format, SAToP Packet format for an IPv4/IPv6, SAToP Packet format for a MPLS PSN, and SAToP Payload Layer. SATop Control Word.
PWE3-TDMoIP
December 2006 '*draft-ietf-pwe3-tdmoip-06.txt*' revision shall be supported.
PWE3-HDLC
September 2006 '*rfc4618.txt*' revision shall be supported. (excluding clause 4.3 – PPP)
IEEE 802.3
This standard covers the MAC interface to a PHY for MII.
MPLS-Frame Relay Alliance Implementation Agreements 4.1
The purpose of this Implementation Agreement (IA) is to define network interworking between TDM circuits (n x 64 kbps, E1/T1/E3/T3) over MPLS Label Switched Paths (LSPs) by using AAL1 encapsulation.
MPLS-Frame Relay Alliance Implementation Agreements 5.1
This specification defines MPLS support for the transport of AAL type 2 CPS-Packets. Frame formats and procedures required for this transport are described in this Implementation Agreement. This specification addresses the transport of any AAL type 2 CPS-Packets regardless of the application data that is transported.
MPLS-Frame Relay Alliance Implementation Agreements 8.0.0
This document describes a method for encapsulating TDM signals belonging to the PDH hierarchy (T1, E1, T3, E3, Nx64kbps) as pseudo-wires over a MPLS network.
MEF 8 – Metro Ethernet Forum 8 - Implementation Agreement for the Emulation of PDH Circuits over Metro Ethernet Networks
This document provides an implementation agreement for the emulation of PDH services across a Metro Ethernet Network. Specifically it covers emulation of Nx64kbps, DS1, E1, DS3 and E3 circuits. Generically this is referred to as Circuit Emulation Services over Ethernet (CESoETH).
G.823/G.824 Jitter & Wander Requirements
G.8261/Y.1361 (G.pactiming) Timing and Synchronization Aspects in Packet Networks
This recommendation defines synchronization aspects in packet networks and specifies the maximum network limits of jitter and wander that shall not be exceeded and the minimum equipment tolerance to jitter and wander than shall be provided at the boundary of these packet networks at TDM interfaces. It also outlines the minimum requirements for the synchronization function of network elements.

4. Detailed Description

The DS34T108 is an 8-port device featuring independent transceivers that can be software configured for T1/J1 or E1. The DS34T104/DS34T102/DS34T101 have the same functionality as the DS34T108, the product reference throughout this document, but with fewer ports. Each transceiver, composed of an LIU, framer, HDLC controller, elastic store, connects to the TDM-over-Packet (TDMoP) block for a complete monolithic solution to IP or MPLS or Ethernet Layer 2 networks. The internal MAC supports connectivity to a single 10/100Mbps, MII//RMII/SSMII. The DS34T108 is controlled via a 16-bit or 32-bit parallel port or via an SPI serial port.

The LIU is composed of a transmit interface, receive interface, and a jitter attenuator. Internal impedance matching is provided for both transmit and receive paths, reducing external component count. The transmit interface is responsible for generating the necessary waveshapes for driving the network and providing the correct source impedance depending on the type of media used. T1 waveform generation includes DSX-1 line build-outs as well as CSU line build-outs of 0dB, -7.5dB, -15dB, and -22.5dB. E1 waveform generation includes G.703 waveshapes for both 75Ω coax and 120Ω twisted cables. The receive interface provides network termination and recovers clock and data from the network. The receive sensitivity adjusts automatically to the incoming signal level and can be programmed for 0dB to -43dB or 0dB to -12dB for E1 applications and 0dB to -15dB or 0dB to -36dB for T1 applications. The jitter attenuator removes phase jitter from the transmitted or received signal. The crystal-less jitter attenuator can be placed in either the transmit or the receive data paths and requires only a T1/J1 or E1 clock rate, a SONET/SDH reference frequency of 19.44/38.88/77.76MHz, or a GPS reference frequency of 10MHz for both T1/J1 and E1 applications.

On the transmit side, clock, data, and frame-sync signals are provided to the framer by the backplane interface section. The framer inserts the appropriate synchronization framing patterns, alarm information, calculates and inserts the CRC codes, and provides the B8ZS/HDB3 (zero code suppression) and AMI line coding. The receive-side framer decodes AMI, B8ZS, and HDB3 line coding, synchronizes to the data stream, reports alarm information, counts framing/coding/CRC errors, and provides clock, data, and frame-sync signals to the backplane interface section.

Both transmit and receive paths have access to an HDLC controller. The HDLC controller transmits and receives data via the framer block. The HDLC controller can be assigned to any time slot, a portion of a time slot or to FDL (T1) or Sa bits (E1). Each controller has 64-byte FIFOs, reducing the amount of processor overhead required to manage the flow of data.

The TDM-over-Packet (TDMoP) core is the building block for circuit emulation and other network applications. It performs transparent transport of legacy TDM traffic over Packet Switched Networks (PSNs). The TDMoP core implements payload methods such as AAL1 for circuit emulation, AAL2-like method for loop emulation, HDLC method, structure-agnostic SAToP method, and the structure-aware CESoPSN method.

The AAL1 payload-type machine converts E1/T1/E3/T3/STS-1/serial data flows into IP, MPLS or Ethernet packets, and vice versa, according to ITU-T Y.1413, Y.1453, MEF 8, MFA 4.1, and the IETF PWE3 TDMoIP draft. It supports E1/T1 structured mode with/without CAS, using a time slot size of 8 bits, or unstructured mode (carrying serial interfaces, unframed E1/T1 or E3/T3/STS-1 traffic).

The AAL2 payload-type machine converts E1/T1 data flows into IP, MPLS or Ethernet packets, and vice versa, implementing dynamic time slot allocation. It supports E1/T1 structured mode with/without CAS with 8-bit time slot resolution, according to ITU-T Y.1414 (clause 10), Y.1452, MFA 5.1 and the IETF PWE3 TDMoIP draft.

The HDLC payload-type machine converts and terminates HDLC-based E1/T1/serial flow into IP/MPLS packets and vice versa, according to the IETF RFC 4618 (excluding clause 5.3—PPP) and TDMoIP draft. It supports 2-, 7- and 8-bit time slot resolution (i.e., 16kbps, 56kbps, and 64kbps, respectively), as well as N × 64 kbps bundles (n = 1 to 32). Supported applications of this machine include trunking of HDLC-based traffic (such as frame relay) implementing dynamic bandwidth allocation over IP/MPLS networks, and HDLC-based signaling interpretation (such as ISDN D-channel signaling termination—BRI or PRI, V5.1/2, or GR-303).

The SAToP payload-type machine converts unframed E1/T1/E3/T3 data flows into IP, MPLS, or Ethernet packets, and vice versa, according to ITU-T Y.1413, Y.1453, MEF 8, MFA 8.0.0, and IETF RFC 4553. It supports E1/T1/E3/T3 with no regard for the TDM structure. If TDM structure exists it is ignored, allowing it to be the simplest way of making payload. The size of the payload is programmable for different services. This emulation suits applications where the provider edges have no need to interpret TDM data or to participate in the TDM signaling. The PSN network must have almost no packet loss and a very low PDV for this method.

The CESoPSN payload-type machine converts structured E1/T1/E3/T3 data flows into IP, MPLS or Ethernet packets, and vice versa, with static assignment of time slots inside a bundle according to ITU-T Y.1413, Y.1453, MEF 8, MFA 8.0.0, and the IETF PWE3 CESoPSN draft. It supports E1/T1/E3/T3 while taking into account the TDM structure. The level of structure must be chosen for proper payload conversion such as the framing type (i.e., frame, multiframe). This method is less sensitive to PSN impairments, but lost packets could still cause service interruption. The payload is simply encapsulated into 24 bytes for T1 and 32 bytes for E1.

5. Application Examples

In Figure 5-1, DS34T108 is used to allow TDM services over a packet-switched metropolitan network, using various access methods (G/E PON, fiber optic, wireless, cable).

Figure 5-1. Metropolitan Legacy Service Over Packet-Switched Network

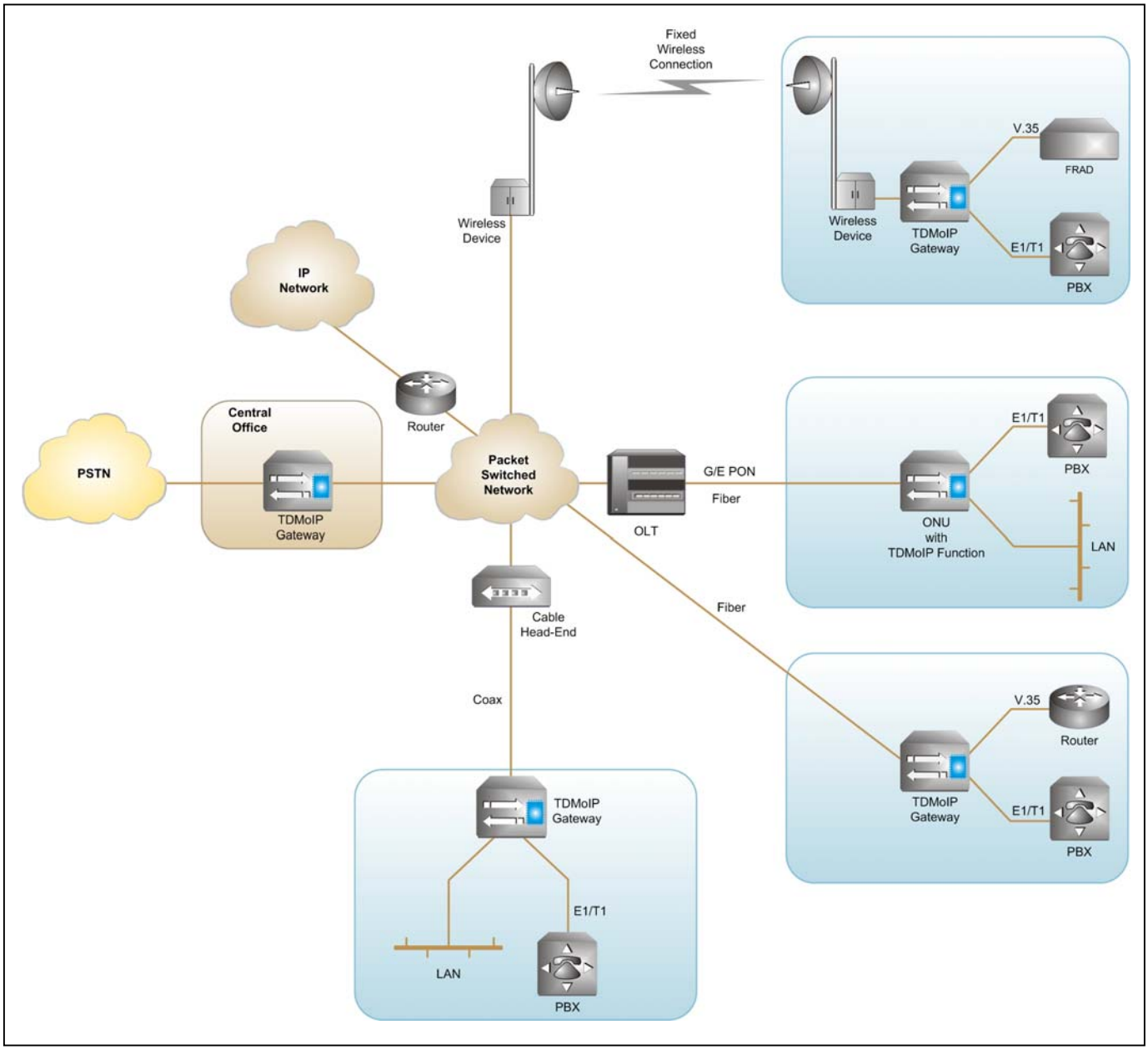
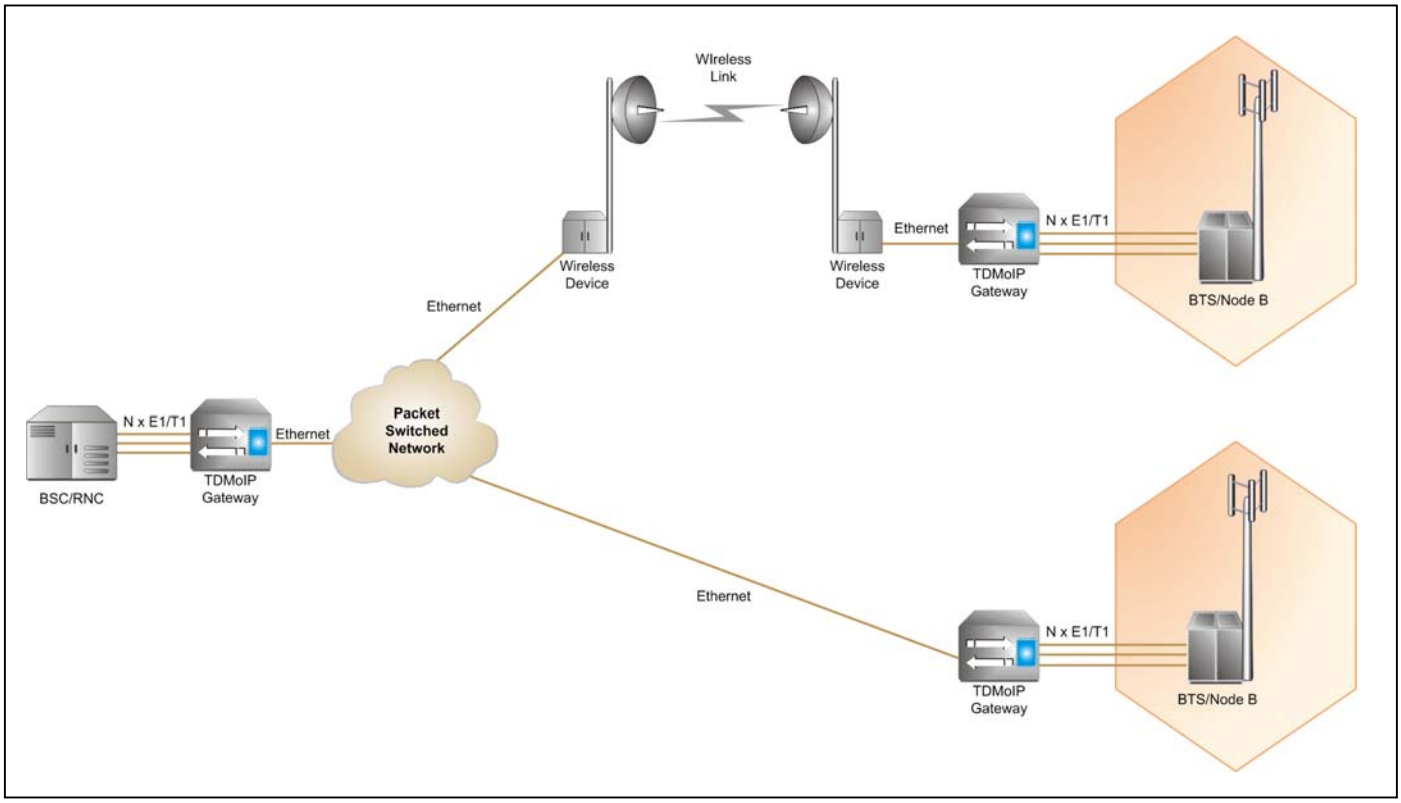


Figure 5-2. Cellular 2/3G Backhaul Over Packet-Switched Networks



5.1.1 Other Possible Applications

5.1.1.1 Point-to-Multipoint TDM Connectivity over IP/Ethernet

The TDM-over-Packet chip supports DS0-level multiple bundles/connections with and without CAS (Channel Associated Signaling). There is no need for an external TDM cross-connect, as the packet domain can be used as a virtual cross-connect; any bundle of time slots can be directed to another remote location on the packet domain.

5.1.1.2 HDLC Transport over IP/MPLS

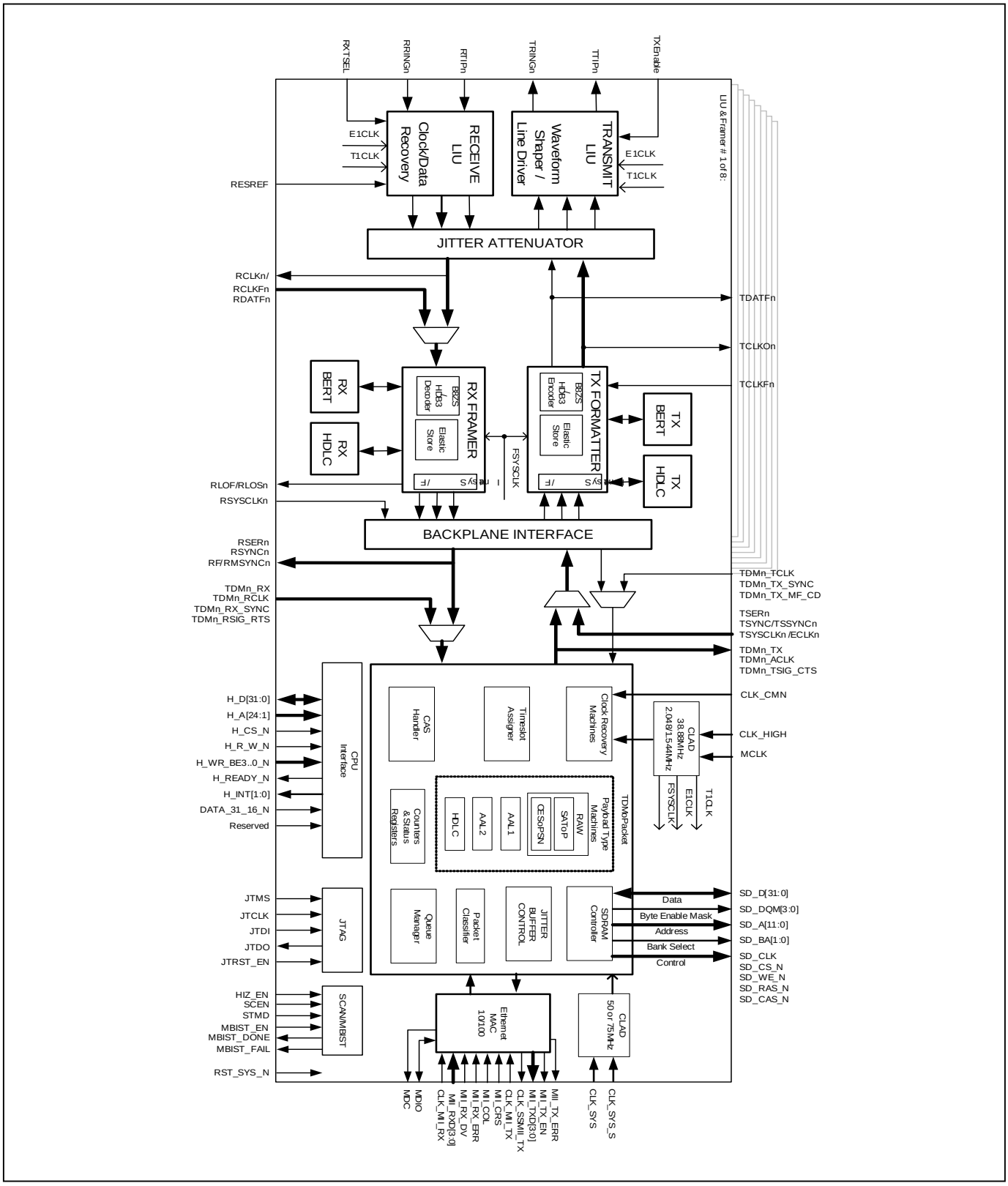
TDM traffic streams often contain HDLC-based control and data traffic. These data streams, when transported over a packet domain, should be treated differently than the time-sensitive TDM payload. The DS34T108 includes HDLC controller capability, which enables termination of the HDLC frames. HDLC-based control protocols, such as ISDN BRI and PRI, SS7, etc., and other frame-based traffic, can be managed and transported.

5.1.1.3 Using a Packet Backplane for Multiservice Concentrators

A communications device with all the above-mentioned capabilities can use a packet-based backplane instead of the more expensive TDM bus option. This enables a cost-effective and future-proof design of communication platforms with full support for both legacy and next-generation services.

6. Block Diagram

Figure 6-1. DS34T108 Functional Block Diagram



7. Feature Highlights

The following sections describe the features provided by the 8-port DS34T108.

7.1 Global Features

- The DS34T108 chip offers:
  - Eight E1/T1 LIUs/framers/TDMoP interfaces or
  - One E3/DS3/STS-1 TDMoP interface or
  - One serial TDMoP interface for V.35 and RS530
- Ethernet interface
  - One 10/100Mbps, MII/RMII/SSMII
  - Half/full duplex
  - VLAN support according to 802.1 p&Q
  - Fully compatible with IEEE 802.3 standard
- End-to-end TDM synchronization through the IP/MPLS domain by eight independent on-chip TDM clock recovery mechanisms, on a per-port basis
- 64 independent bundles/connections, each with its own:
  - Transmit and receive queues
  - Configurable jitter-buffer depth
  - Connection level redundancy, with traffic duplication option
- 64 Internal bundle cross-connect capability, with DS0 resolution
- Any framer receiver port to any TDM interface receiver to maintain bundle connectivity
- Any transmit TDM interface to any framer transmit port to maintain bundle connectivity
- Packet loss compensation and handling of misordered packets
- Glueless SDRAM interface
- Complies with MPLS-Frame Relay Alliance Implementation Agreements 4.1, 5.1, and 8.0
- Meets ITU standards Y.1413 and Y.1414
- Complies with Metro Ethernet Forum 3 & 8
- Conforms to drafts submitted to IETF
- 23mm x 23 mm, 484-pin HSBGA package (1mm pitch)
- IEEE 1146.1 JTAG boundary scan
- 1.8V and 3.3V Operation with 5.0V tolerant I/O

7.2 Line Interface

- Requires a single 38.88Mz, 19.44MHz, 77.76MHz, or 10MHz clock high synthesis (CLK_HIGH) input for both E1 and T1 operation. Optionally, a 1.544MHz or 2.048MHz master clock (MCLK) also can be used for LIU clock recovery
- Fully software configurable
- Short- and long-haul applications
- Ranges include 0dB to -43dB, 0dB to -30dB, 0dB to 20dB, and 0dB to -12dB for E1; 0dB to -36dB, 0dB to 30dB, 0dB to 20dB, and 0dB to -15dB for T1
- Receiver signal level indication from -2.5dB to -36dB in T1 mode and -2.5dB to -44dB in E1 mode in 2.5dB increments
- Internal receive termination option for 75Ω, 100Ω, 110Ω, and 120Ω lines
- Monitor application gain settings of 14dB, 20dB, 26dB, and 32dB
- G.703 receive synchronization signal mode
- Flexible transmit waveform generation
- T1 DSX-1 line build-outs
- T1 CSU line build-outs of 0dB, -7.5dB, -15dB, and -22.5dB

- E1 waveforms include G.703 waveshapes for both 75Ω coax and 120Ω twisted cables
- Analog loss of signal detection
- AIS generation independent of loopbacks
- Alternating ones and zeros generation
- Receiver power-down
- Transmitter power-down
- Transmitter short-circuit limiter with current limit exceeded indication
- Transmit open-circuit-detected indication

7.3 Clock Synthesizer

- Internal clock synthesis for the E1 and T1 from an input of 38.88Mz, 19.44MHz, 77.76MHz, or 10MHz clock source.

7.4 Jitter Attenuator

- 32-bit or 128-bit crystal-less jitter attenuator
- Can be placed in either the receive or transmit path or disabled
- Limit trip indication

7.5 Framer/Formatter

- Fully independent transmit and receive functionality
- Full receive and transmit path transparency
- T1 framing formats D4 and ESF per T1.403, and expanded SLC-96 support (TR-TSY-008)
- E1 FAS framing and CRC-4 multiframe per G.704/G.706, and G.732 CAS multiframe
- Transmit side synchronizer
- Transmit midpath CRC recalculate (E1)
- Detailed alarm and status reporting with optional interrupt support
- Large path and line error counters
- T1: BPV, CV, CRC6, and framing bit errors
- E1: BPV, CV, CRC4, E-bit, and frame alignment errors
- Timed or manual update modes
- DS1 Idle Code Generation on a per-channel basis in both transmit and receive paths
  - User-defined code generation
  - Digital milliwatt code generation
- ANSI T1.403-1999 Support
- G.965 V5.2 link detect
- Ability to monitor one DS0 channel in both the transmit and receive paths
- In-band repeating pattern generators and detectors
- Three independent generators and detectors
- Patterns from 1 to 8 bits or 16 bits in Length
- Bit oriented code (BOC) support
- Software or hardware based signaling support
- Interrupt generated on change of signaling data
- Optional receive signaling freeze on loss of frame, loss of signal, or frame slip
- Hardware pins provided to indicate loss of frame (LOF), loss of signal (LOS), loss of transmit clock (LOTC), or signaling freeze condition
- Automatic RAI generation to ETS 300 011 specifications

- RAI-CI and AIS-CI support
- Expanded access to Sa and Si bits
- Option to extend carrier loss criteria to a 1ms period as per ETS 300 233
- Japanese J1 support
- Ability to calculate and check CRC6 according to the Japanese standard
- Ability to generate Yellow Alarm according to the Japanese standard
- T1 to E1 conversion

7.6 Framer System Ports

- Independent two-frame receive and transmit elastic stores
- Independent control and clocking
- Controlled slip capability with status
- Supports T1 to CEPT (E1) conversion
- Ability to pass the T1 F-bit position through the elastic stores in the 2.048MHz backplane mode
- Hardware signaling capability
- Receive signaling reinsertion to a backplane multiframe sync
- Availability of signaling in a separate PCM data stream
- BERT testing to the system interface

7.7 TDM-over-Packet Engine

TDM-over-Packet enables transport of legacy TDM services – E1/T1, E3/T3, STS-1, or serial data (on the user side) over packet switched networks – IP, MPLS or Ethernet (on the network side). This module implements the following payload methods of TDM transfer over IP, MPLS or Ethernet networks:

- SAToP (Structure-Agnostic TDM over Packet)
- Structure-aware format for structured E1/T1 with or without CAS (CESoPSN)
- AAL1 format (constant rate/static allocation of time slots)
- AAL2 format (dynamic allocation of time slots)
- HDLC termination for efficient transfer of frame-based traffic.

A dedicated payload type engine implements each per the following method:

- SAToP hardware engine converts unframed E1/T1/E3/T3/STS-1 or serial data flows into IP, MPLS, or Ethernet packets and vice versa according to ITU-T Y.1413, MEF 8, MFA 8.0.0 and the IETF PWE3 SAToP draft.
- CESoPSN hardware engine converts structured E1/T1 data flows into IP, MPLS or Ethernet packets and vice versa with static assignment of time slots inside a bundle according to ITU-T Y.1413, MEF 8, MFA 8.0.0, and the IETF PWE3 CESoPSN draft.
- AAL1 hardware engine converts E1/T1/E3/T3/STS-1 or serial data flows into IP, MPLS or Ethernet packets, and vice versa, according to ITU-T Y.1413, MEF 8, MFA 4.1 and the IETF PWE3 TDMoIP draft. For E1/T1 it supports structured mode with/without CAS using 8-bit time slot resolution, while implementing static time slot allocation. For E1/T1, E3/T3/STS-1 or serial interface it supports unstructured mode.
- AAL2 hardware engine converts E1/T1 data flows into IP/MPLS/Ethernet packets, and vice versa, while implementing dynamic time slot allocation. It supports E1/T1 structured mode with/without CAS using 8-bit time slot resolution, according to ITU-T Y.1414 (clause 10), MFA 5.1 and the IETF PWE3 TDMoIP draft.
- HDLC hardware engine converts and terminates HDLC-based E1/T1/serial flow into IP/MPLS/Ethernet packets and vice versa. It supports 2-, 7- and 8-bit time slot resolution (i.e., 16kbps, 56kbps, and 64kbps, respectively), as well as N x 64kbps bundles. This is useful in applications where HDLC-based signaling interpretation is required (such as ISDN D channel signaling termination, V.51/2, or GR-303), or for trunking packet-based applications (such as Frame Relay), according to the IETF PWE3 HDLC draft.

7.7.1 TDM-over-Packet User Interfaces

The user side consists of either a single high-speed E3, T3 or STS-1, or eight I/Fs, each independently supporting E1, T1 or serial data transfer.

For the E3/T3/STS-1 option, the AAL1 or SAToP method is used.

For the E1/T1 option, the module supports the following operation modes:

- Unframed—E1/T1 pass-through mode (AAL1, SAToP, or HDLC payload type method)
- Structured—fractional E1/T1 support (all payload type methods)
- Structured with CAS—fractional E1/T1 with CAS support (CESoPSN, AAL1, or AAL2 payload type method)

The serial interface option supports synchronous data transfer (for interfaces such as V.35) over the IP/MPLS/Ethernet network for legacy data services (such as frame relay or arbitrary continuous bit stream).

The serial port option supports the following synchronous serial data formats:

- Arbitrary continuous bit stream (using AAL1 or SAToP payload type method)
- In single-interface high-speed mode, the first interface operates at up to STS-1 rate (51.84Mbps) and the other interfaces are disabled. In this mode, the whole traffic is transferred using a single bundle/connection.
- In eight-interface low-speed mode each interface can operate at the rate of N x 64kbps, where N = 1 to 63, with an aggregate rate of 18.6Mbps.
- HDLC-based traffic (such as frame relay transferred using HDLC payload type method). Only the eight-interface low-speed mode is available (N x 64kbps, where N = 1 to 63, with an aggregate rate of 18.6Mbps).

All serial interface modes can work with a gapped clock.

7.7.2 Network Port

The chip features one 10/100 Ethernet port with the option of MII/RMII/SSMII. The port can work in half/full-duplex mode and supports VLAN tagging and priority labeling according to 802.1 p&Q, including VLAN stacking.

7.7.3 Bundles

A bundle is defined as a stream of bits that have originated from the same physical interface and that are transmitted from a TDM-over-Packet source device to a TDM-over-Packet destination device. For example, bundles can comprise any number of 64kbps time slots originating from a single E1 or an entire T3 or E3. Bundles are single-direction streams, frequently coupled with bundles in the opposite direction to enable full-duplex communications. More than one bundle can be transmitted between two TDM-over-Packet edge devices.

The chip supports up to 64 bundles; each can be assigned to any port. The bundles are configured independently, each with its own:

- Transmit and receive queues
- Configurable receive-buffer depth
- Optional connection level redundancy (SAToP, AAL1, CESoPSN only)

The bundles can be assigned to one of the payload type machines or to the CPU. For E1/T1, the chip provides internal bundle cross-connect functionality, with DS0 resolution.

7.7.4 Clock Recovery

Sophisticated TDM clock recovery mechanisms, one for each E1/T1 interface, allow end-to-end TDM clock synchronization, despite packet delay variation of IP/MPLS/Ethernet network.

TDM-over-Packet supports the following clock recovery modes:

- Adaptive clock recovery
- Common clock (using RTP)
- External clock
- Loopback clock

The clock recovery mechanisms provide both fast frequency acquisition and highly accurate phase tracking.

- Jitter and wander of the recovered clock are maintained at levels that conform to G.823/G.824 traffic or synchronization interfaces. For adaptive clock recovery, the recovered clock performance depends on packet network characteristics.
- Short-term frequency accuracy (1 second) is better than 16ppb (using OCXO reference) or 100ppb (using TCXO reference)
- Capture range is ±90ppm
- Internal synthesizer resolution of 0.5ppb
- High resilience to the packet loss and misordering, up to 2% of packet loss/misordering without degradation of clock recovery performance
- Robust to sudden significant constant delay changes
- Automatic transition to hold-over is performed upon link-break events.

7.7.5 Delay Variation Compensation

The TDM-over-Packet module provides large configurable jitter buffers, on a per-bundle basis, that compensate for the delay variation introduced by the IP/MPLS/Ethernet network, with the following depths:

- E1: Up to 256ms
- T1 Unframed: Up to 340ms
- T1 Framed: Up to 256ms
- T1 Framed with CAS: Up to 192ms
- E3: Up to 60ms
- T3: Up to 45ms
- STS-1: Up to 40ms

For the SAToP and CESoPSN bundles, TDM-over-Packet performs packet reordering within the range of the jitter buffer.

Packet loss is compensated by inserting either a preconfigured conditioning value or the last received value.

7.7.6 CAS Support

A CAS handler terminates the E1/T1 CAS when using AAL1/AAL2/CESoPSN in structured-with-CAS mode. This eliminates the need for CPU intervention.

7.8 Test and Diagnostics

- IEEE 1149.1 Support
- Per-channel programmable on-chip bit error-rate testing (BERT)
- Pseudorandom patterns including QRSS
- User-defined repetitive patterns
- Error insertion single and continuous
- Total-bit and errored-bit counts
- Payload error insertion
- Error insertion in the payload portion of the T1 & E1 frame in the transmit path

- Errors can be inserted over the entire frame or selected channels
- Insertion options include continuous and absolute number with selectable insertion rates
- F-bit corruption for line testing
- Loopbacks (remote, local, analog, and per-channel loopback)
- MBIST

7.9 Control Port

The CPU interface provides a connection to a host with a 16/32-bit data bus. This allows configuration of chip control registers and statistics collection using the chip counters and status registers. It also provides access to the CPU transmit and received buffers allocated in the SDRAM, used for packets that are directed to/originate from the CPU (such as ARP, SNMP, etc.).

- 32- or 16-bit parallel control port
- Software reset supported
- Hardware reset pin
- Software access to device ID and silicon revision

8. Overview of Major Operational Modes

This section provides a high-level overall description of the DS34T108 and its functional interfaces and capabilities.

8.1 Internal Mode Configured as One-Clock Mode

The default mode of the DS34T108 is internal mode and one-clock mode. Internal mode is used to internally connect the framer and the TDM-over-Packet blocks. Internal mode additionally sets many unused output port/interface pins to drive low. Unused input port/interface pins become inactive. This is due to the signals now being connected internally. Figure 8-1 represents the block diagram of this mode.

One-clock mode refers to both the transmit and the receive interfaces using a single recovery clock for the framer port and TDM-over-Packet interface. Transmit and the receiver are therefore synchronized together. This mode requires the elastic store of the receiver framer to be enabled. Registers additionally allow the selection of any one clock and transmit synchronization pulse to connect to any port. Figure 8-2 represents the internal connections for a single port/interface.

Figure 8-1. Internal Mode

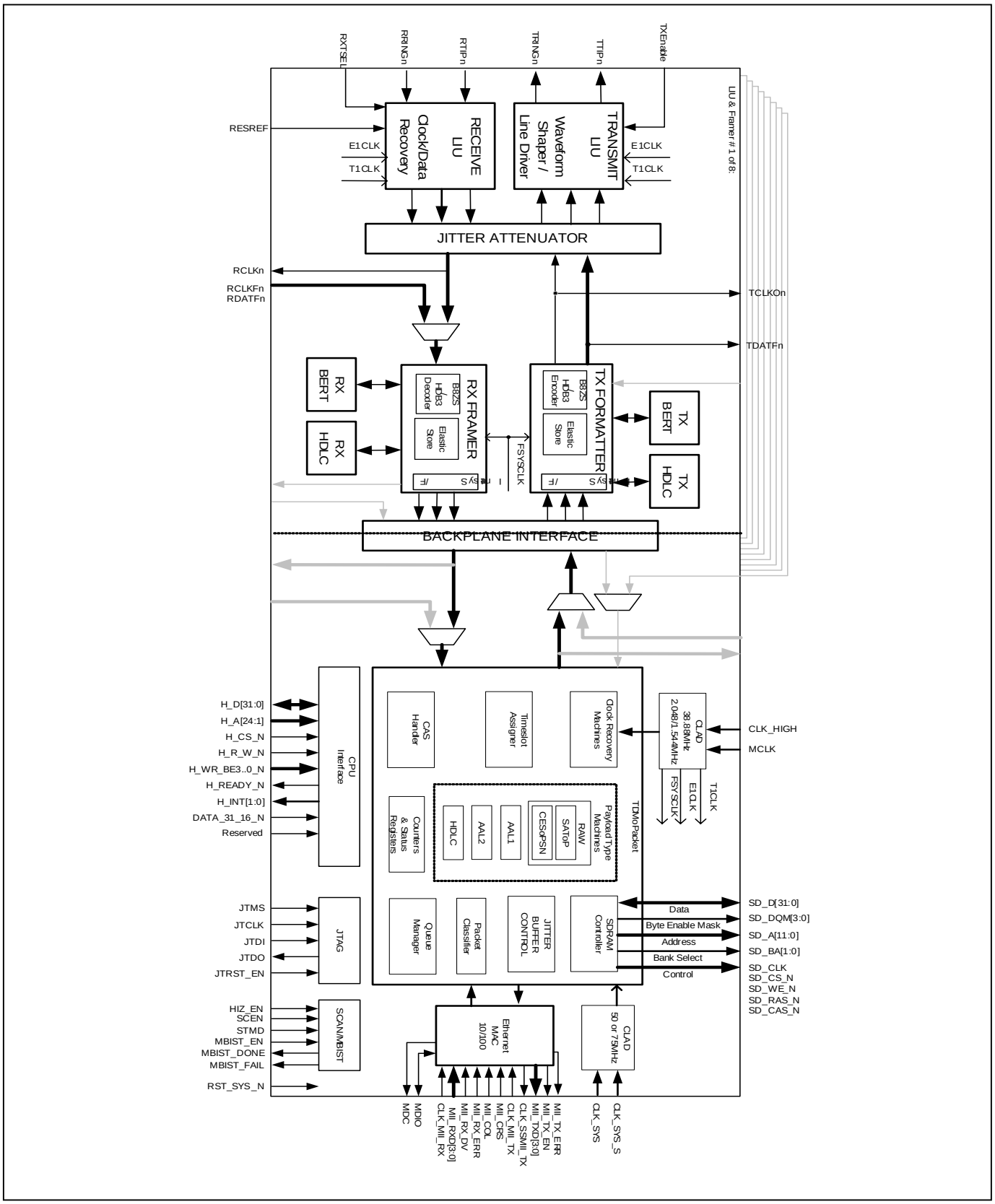
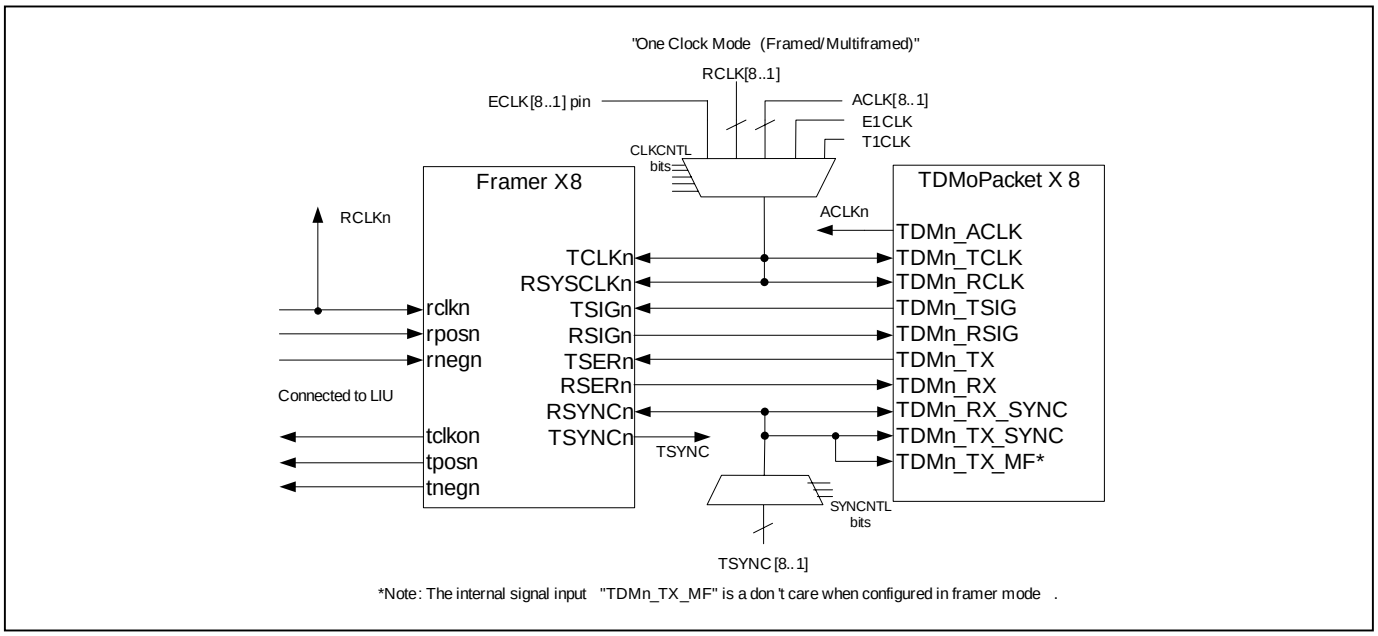


Figure 8-2. Internal One-Clock Mode



8.2 Internal Mode Configured as Two-Clock Mode

Internal two-clock mode configures the port/interfaces to have separate clocking between transmit and receive port/interfaces.

Figure 8-3 represent a single internal two-clock mode port/interface connection for framed and multiframed applications. In this mode, the elastic store should not be enabled. The receive frame synchronization pulse or receive multiframe synchronization are delivered from the framer to the TDM-over-Packet block based on RCLKFn. The transmit synchronization pulse also comes from the framer with TSYNC configured for framer pulses or multiframe pulses based on the TCLKF input.

The user may not need to use the framer during particular applications. If this is the case, the user should set the GCR1.UNFRMMODE bit. This selects internal two-clock mode for unframed applications as shown in Figure 8-4.

Figure 8-3. Internal Two-Clock Mode (Framed)

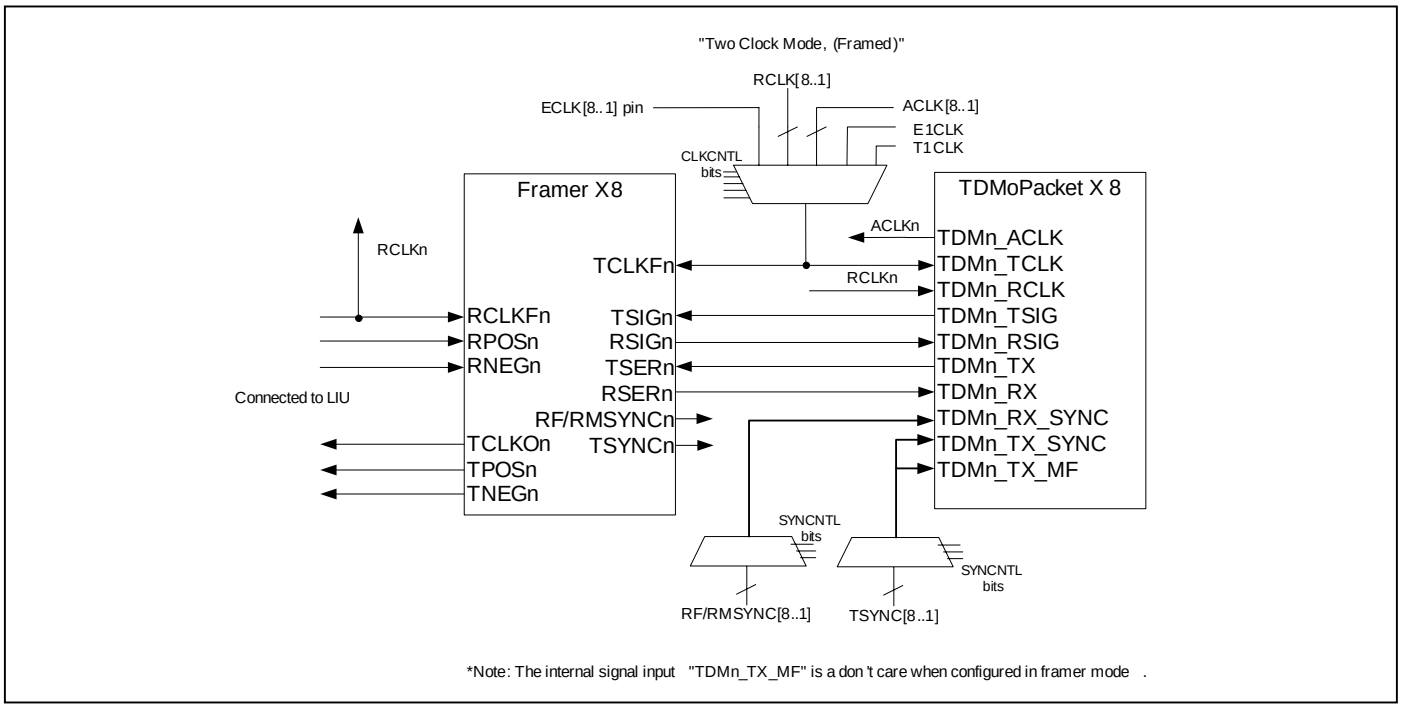
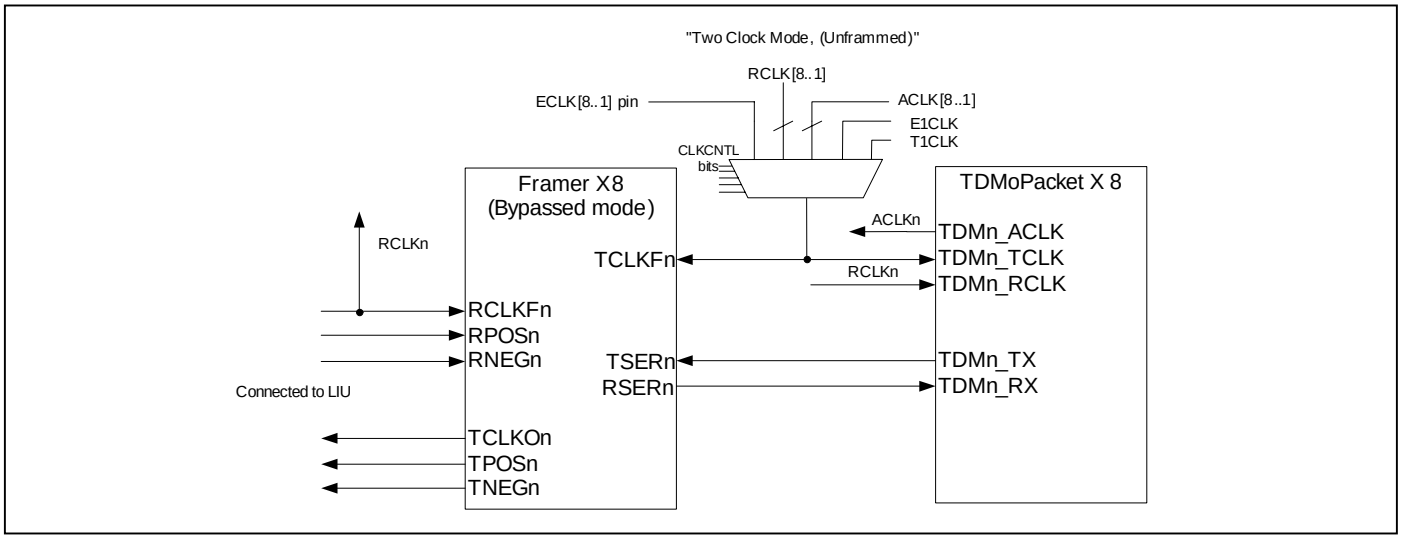


Figure 8-4. Internal Two-Clock Mode (Unframed)



8.3 External Mode

External mode activates all the port interface pins for utilization of when the user wants to custom wire the connections between the framer and TDM-over-Packet externally. Many applications that require a network processor would need wiring like this to be applied between these two points. Refer to the full data sheet for more information.

9. Functional Description and Device Registers

Refer to the full data sheet for this information.

10. Pin Description

10.1 Short Pin Descriptions

In the type column, of the short pin description, the following abbreviations are used: I (Input), Ipu (Input with Pullup), Ipd (Input with Pulldown), Ia (Analog Input), O (Output), Oz (Output Tri-Stateable), Oa (Analog Output), IO (Bidirectional Inout), IOpd (Bidirectional with Pulldown), and IOpu (Bidirectional with Pullup).

Table 10-1. DS34T108 Short Pin Descriptions

NAME	TYPE	FUNCTION
SD_D[31:0]	IO	Synchronous DRAM Data Bus
SD_DQM[3:0]	O	Byte Enable Mask
SD_A[11:0]	O	SDRAM Address Bus
SD_BA[1:0]	O	SDRAM Bank Select
SD_CLK	O	SDRAM Clock
SD_CS_N	O	SDRAM Chip Select (Active Low)
SD_WE_N	O	SDRAM Write Enable (Active Low)
SD_RAS_N	O	SDRAM Row Address Strobe Enable (Active Low)
SD_CAS_N	O	SDRAM Column Address Strobe (Active Low)
TDM1_TX	O	TDM1 Transmit
TDM1_RX	Ipu	TDM1 Receive
TDM1_TCLK	Ipu	TDM1 Transmit Clock
TDM1_RCLK	Ipu	TDM1 Receive Clock
TDM1_ACLK	O	TDM1 Recovery Clock
TDM1_TX_SYNC	Ipd	TDM1 Transmit/Receive Sync Pulse
TDM1_TX_MF_CD	IOpd	TDM1 Transmit Multiframe Sync Pulse/Carrier Detect
TDM1_RX_SYNC	Ipd	TDM1 Receive Multiframe Sync Pulse/Sync Pulse
TDM1_TSIG_CTS	O	TDM1 Transmit Signaling/Clear to Send
TDM1_RSIG_RTS	Ipu	TDM1 Receive Signaling/Request To Send
TDM2_TX	O	TDM2 Transmit
TDM2_RX	Ipu	TDM2 Receive
TDM2_TCLK	Ipu	TDM2 Transmit Clock
TDM2_RCLK	Ipu	TDM2 Receive Clock
TDM2_ACLK	O	TDM2 Recovery Clock
TDM2_TX_SYNC	Ipd	TDM2 Transmit/Receive Sync Pulse
TDM2_TX_MF_CD	IOpd	TDM2 Transmit Multiframe Sync Pulse/Carrier Detect
TDM2_RX_SYNC	Ipd	TDM2 Receive Multiframe Sync Pulse/Sync Pulse
TDM2_TSIG_CTS	O	TDM2 Transmit Signaling/Clear to Send
TDM2_RSIG_RTS	Ipu	TDM2 Receive Signaling/Request To Send
TDM3_TX	O	TDM3 Transmit

NAME	TYPE	FUNCTION
TDM3_RX	Ipu	TDM3 Receive
TDM3_TCLK	Ipu	TDM3Transmit Clock
TDM3_RCLK	Ipu	TDM3 Receive Clock
TDM3_ACLK	O	TDM3 Recovery Clock
TDM3_TX_SYNC	Ipd	TDM3 Transmit/Receive Sync Pulse
TDM3_TX_MF_CD	IOpd	TDM3 Transmit Multiframe Sync Pulse/Carrier Detect
TDM3_RX_SYNC	Ipd	TDM3 Receive Multiframe Sync Pulse/Sync Pulse
TDM3_TSIG_CTS	O	TDM3 Transmit Signaling/Clear to Send
TDM3_RSIG_RTS	Ipu	TDM3 Receive Signaling/Request To Send
TDM4_TX	O	TDM4 Transmit
TDM4_RX	Ipu	TDM4 Receive
TDM4_TCLK	Ipu	TDM4Transmit Clock
TDM4_RCLK	Ipu	TDM4 Receive Clock
TDM4_ACLK	O	TDM4 Recovery Clock
TDM4_TX_SYNC	Ipd	TDM4 Transmit/Receive Sync Pulse
TDM4_TX_MF_CD	IOpd	TDM4 Transmit Multiframe Sync Pulse/Carrier Detect
TDM4_RX_SYNC	Ipd	TDM4 Receive Multiframe Sync Pulse/Sync Pulse
TDM4_TSIG_CTS	O	TDM4 Transmit Signaling/Clear to Send
TDM4_RSIG_RTS	Ipu	TDM4 Receive Signaling/Request To Send
TDM5_TX	O	TDM5 Transmit
TDM5_RX	Ipu	TDM5 Receive
TDM5_TCLK	Ipu	TDM5Transmit Clock
TDM5_RCLK	Ipu	TDM5 Receive Clock
TDM5_ACLK	O	TDM5 Recovery Clock
TDM5_TX_SYNC	Ipd	TDM5 Transmit/Receive Sync Pulse
TDM5_TX_MF_CD	IOpd	TDM5 Transmit Multiframe Sync Pulse/Carrier Detect
TDM5_RX_SYNC	Ipd	TDM5 Receive Multiframe Sync Pulse/Sync Pulse
TDM5_TSIG_CTS	O	TDM5 Transmit Signaling/Clear to Send
TDM5_RSIG_RTS	Ipu	TDM5 Receive Signaling/Request To Send
TDM6_TX	O	TDM6 Transmit
TDM6_RX	Ipu	TDM6 Receive
TDM6_TCLK	Ipu	TDM6Transmit Clock
TDM6_RCLK	Ipu	TDM6 Receive Clock
TDM6_ACLK	O	TDM6 Recovery Clock
TDM6_TX_SYNC	Ipd	TDM6 Transmit/Receive Sync Pulse
TDM6_TX_MF_CD	IOpd	TDM6 Transmit Multiframe Sync Pulse/Carrier Detect
TDM6_RX_SYNC	Ipd	TDM6 Receive Multiframe Sync Pulse/Sync Pulse
TDM6_TSIG_CTS	O	TDM6 Transmit Signaling/Clear to Send
TDM6_RSIG_RTS	Ipu	TDM6 Receive Signaling/Request To Send

NAME	TYPE	FUNCTION
TDM7_TX	O	TDM7 Transmit
TDM7_RX	Ipu	TDM7 Receive
TDM7_TCLK	Ipu	TDM7Transmit Clock
TDM7_RCLK	Ipu	TDM7 Receive Clock
TDM7_ACLK	O	TDM7 Recovery Clock
TDM7_TX_SYNC	Ipd	TDM7 Transmit/Receive Sync Pulse
TDM7_TX_MF_CD	IOpd	TDM7 Transmit Multiframe Sync Pulse/Carrier Detect
TDM7_RX_SYNC	Ipd	TDM7 Receive Multiframe Sync Pulse/Sync Pulse
TDM7_TSIG_CTS	O	TDM7 Transmit Signaling/Clear to Send
TDM7_RSIG_RTS	Ipu	TDM7 Receive Signaling/Request To Send
TDM8_TX	O	TDM8 Transmit
TDM8_RX	Ipu	TDM8 Receive
TDM8_TCLK	Ipu	TDM8Transmit Clock
TDM8_RCLK	Ipu	TDM8 Receive Clock
TDM8_ACLK	O	TDM8 Recovery Clock
TDM8_SYNC	Ipd	TDM8 Transmit/Receive Sync Pulse
TDM8_TX_MF_CD	IOpd	TDM8 Transmit Multiframe Sync Pulse/Carrier Detect
TDM8_RX_MF	Ipd	TDM8 Receive Multiframe Sync Pulse
TDM8_TSIG_CTS	O	TDM8 Transmit Signaling/Clear to Send
TDM8_RSIG_RTS	Ipu	TDM8 Receive Signaling/Request To Send
CLK_MII_RX	I	Clock Media Independent Interface Receive
MII_RXD[0]	I	Media Independent Interface Receive Data 0
MII_RXD[1]	I	Media Independent Interface Receive Data 1
MII_RXD[2]	I	Media Independent Interface Receive Data 2
MII_RXD[3]	I	Media Independent Interface Receive Data 3
MII_RX_DV	I	Media Independent Interface Receive Data Valid
MII_RX_ERR	I	Media Independent Interface Receive Error
MII_COL	I	Media Independent Interface Collision
MII_CRS	I	Media Independent Interface carrier sense.
CLK_MII_TX	I	Clock Media Independent Interface Transmit
CLK_SSMII_TX	O	Clock Source Synchronous Serial Media Independent Interface Transmit
MII_TXD[0]	O	Media Independent Interface Transmit Data 0
MII_TXD[1]	O	Media Independent Interface Transmit Data 1
MII_TXD[2]	O	Media Independent Interface Transmit Data 2
MII_TXD[3]	O	Media Independent Interface Transmit Data 3
MII_TX_EN	O	Media Independent Interface Transmit Enable
MII_TX_ERR	O	Media Independent Interface Transmit Error
MDIO	IOpu	Management Data Input/Output
MDC	O	Management Data Clock

NAME	TYPE	FUNCTION
TTIP1 TTIP2 TTIP3 TTIP4 TTIP5 TTIP6 TTIP7 TTIP8	Oa	Transmit Bipolar Tip for Channels 1–8
TRING1 TRING2 TRING3 TRING4 TRING5 TRING6 TRING7 TRING8	Oa	Transmit Bipolar Ring for Channels 1–8
TXENABLE	I	Transmit Enable for All Channels 1–8
RTIP1 RTIP2 RTIP3 RTIP4 RTIP5 RTIP6 RTIP7 RTIP8	Ia	Receive Bipolar Tip for Channels 1–8
RRING1 RRING2 RRING3 RRING4 RRING5 RRING6 RRING7 RRING8	Ia	Receive Bipolar Ring for Channels 1–8
RXTSEL	I	Receive Termination Selection
RCLKF1/RCLK1 RCLKF2/RCLK2 RCLKF3/RCLK3 RCLKF4/RCLK4 RCLKF5/RCLK5 RCLKF6/RCLK6 RCLKF7/RCLK7 RCLKF8/RCLK8	IO	Receive Framer Clock/Receive Clock
TCLKF1 TCLKF2 TCLKF3 TCLKF4 TCLKF5 TCLKF6 TCLKF7 TCLKF8	I	Transmit Clock Input for the Formatter

NAME	TYPE	FUNCTION
TCLKO1 TCLKO2 TCLKO3 TCLKO4 TCLKO5 TCLKO6 TCLKO7 TCLKO8	O	Transmit Clock Output
RSER1 RSER2 RSER3 RSER4 RSER5 RSER6 RSER7 RSER8	O	Receive Serial Data Output
TDATF1 TDATF2 TDATF3 TDATF4 TDATF5 TDATF6 TDATF7 TDATF8	O	Transmit Data Formatter Output
RSYNC1 RSYNC2 RSYNC3 RSYNC4 RSYNC5 RSYNC6 RSYNC7 RSYNC8	IO	Receive Sync
RSYSCLK1 RSYSCLK2 RSYSCLK3 RSYSCLK4 RSYSCLK5 RSYSCLK6 RSYSCLK7 RSYSCLK8	I	Receive System Clock
RF/RMSYNC1 RF/RMSYNC2 RF/RMSYNC3 RF/RMSYNC4 RF/RMSYNC5 RF/RMSYNC6 RF/RMSYNC7 RF/RMSYNC8	O	Frame Synchronization/Receive Multiframe Synchronization

NAME	TYPE	FUNCTION
RLOF/RLOS1 RLOF/RLOS2 RLOF/RLOS3 RLOF/RLOS4 RLOF/RLOS5 RLOF/RLOS6 RLOF/RLOS7 RLOF/RLOS8	O	Receive Loss of Frame/Receive Loss of Signal
TSER1 TSER2 TSER3 TSER4 TSER5 TSER6 TSER7 TSER8	I	Transmit Serial Data
RDATF1 RDATF2 RDATF3 RDATF4 RDATF5 RDATF6 RDATF7 RDATF8	I	Receive Data Framer Input/Transmit Signaling
TSYNC/TSSYNC1 TSYNC/TSSYNC2 TSYNC/TSSYNC3 TSYNC/TSSYNC4 TSYNC/TSSYNC5 TSYNC/TSSYNC6 TSYNC/TSSYNC7 TSYNC/TSSYNC8	IO	Transmit Synchronization/Transmit System Synchronization In
TSYSCLK1/ECLK1 TSYSCLK2/ECLK2 TSYSCLK3/ECLK3 TSYSCLK4/ECLK4 TSYSCLK5/ECLK5 TSYSCLK6/ECLK6 TSYSCLK7/ECLK7 TSYSCLK8/ECLK8	I	Transmit System Clock
CLK_SYS_S	I	System Clock Selection
CLK_SYS	I	System Clock
CLK_HIGH	I	Clock High Synthesis
MCLK	I	Master Clock
CLK_CMN	I	Common Clock
H_D[31:1]	IO	Host Data Bus
H_D[0]/SPI_MISO	IO	Host Data LSB
H_AD[24:1]	I	Host Address Bus
H_CS_N	I	Host Chip Select
H_R_W_N/SPI_CP	I	Host Read/Write

NAME	TYPE	FUNCTION
H_WR_BE0_N/ SPI_CLK	I	H_D[7:0] Write Enable, Active Low
H_WR_BE1_N/ SPI_MOSI	I	H_D[15:8] Write Enable, Active Low
H_WR_BE2_N/ SPI_SEL_N	I	H_D[23:16] Write Enable, Active Low
H_WR_BE3_N/ SPI_CI	I	H_D[31:24] Write Enable, Active Low
H_READY_N	Oz	Host Ready
H_INT[1] H_INT[0]	O	Host Interrupt
DAT_32_16_N	Ipu	Data 32/16-Bit Select
H_CPU_SPI_N	Ipu	CPU or SPI Mode
RST_SYS_N	Ipu	System Reset
RESREF	I	Resistance Reference
JTMS	Ipu	JTAG Test Mode Select
JTCLK	Ipd	JTAG Test Clock
JTDI	Ipu	JTAG Test data In
JTDO	Oz	JTAG Test Data Out
JTRST	Ipu	JTAG Test Reset
SCEN	Ipd	Used for factory tests.
STMD	Ipd	Used for factory tests.
HIZ_N	I	Used for factory tests.
MBIST_EN	I	Used for factory tests.
MBIST_DONE	O	Used for factory tests.
MBIST_FAIL	O	Used for factory tests
TEST_CLK	O	Used for factory tests.
TST_CLD	I	Used for factory tests. DS34T104 only.
TST_TA	O	Used for factory tests. DS34T104 only.
TST_TB	O	Used for factory tests. DS34T104 only.
TST_TC	O	Used for factory tests. DS34T104 only.
TST_RA	O	Used for factory tests. DS34T104 only.
TST_RB	O	Used for factory tests. DS34T104 only.
TST_RC	O	Used for factory tests. DS34T104 only.
DVSS	—	Digital Core Ground for Framers and TDM-over-Packet (31 pins)
DVDDC	—	1.8V Core Supply Voltage for Framers and TDM-over-Packet (17 pins)
DVDDIO	—	3.3V Supply Voltage for I/O (16 pins)
DVDDLIU	—	3.3V Supply Voltage for LIUs (2 pins)
DVSSLIU	—	Digital Ground for the LIUs (2 pins)
ATVDDn	—	3.3V Power Supply for the Transmitter (8 pins)

NAME	TYPE	FUNCTION
ATVSSn	—	Analog Ground for Transmitters (8 pins)
ARVDDn	—	3.3V Analog Receive Power Supply (8 pins)
ARVSSn	—	Analog Receive GND (8 pins)
ACVDD2	—	Analog CLAD 1.8V Supply 2
ACVSS2	—	Analog CLAD GND 2
ACVDD1	—	Analog CLAD 1.8V Supply 1
ACVSS1	—	Analog CLAD GND 1

Note: *Pins with names ending in an asterisk (*) or "_N" are active low.*

10.2 Detailed Pin Descriptions

In the detailed pin description table, the type column defines the drive current for any type of output pin. Also in the detailed pin description table, the type column uses the following abbreviations: I (Input), Ipu (Input with Pullup), Ipd (Input with Pulldown), Ia (Analog Input), O (Output), Oz (Output Tri-Stateable), Oa (Analog output), IO (Bidirectional Inout), IOpd (Bidirectional with Pulldown), and IOpu (Bidirectional with Pullup).

Table 10-2. Detailed Pin Descriptions

NAME	TYPE	FUNCTION
SDRAM PINS		
SD_D[31:0]	IO 8mA	Synchronous DRAM Data Bus **SD_D[31:0]:** Data bus towards SDRAM. MSB is SD_D[31].
SD_DQM[3:0]	O 8mA	Byte Enable Mask **SD_DQM[3:0]:** Byte enable towards SDRAM. Serves as a mask. SD_DQM[0] is connected to the least significant byte at SDRAM, while SD_DQM[3] is connected to the most significant byte at SDRAM.
SD_A[11:0]	O 8mA	SDRAM Address Bus **SD_A[11:0]:** Address bus towards SDRAM. MSB is SD_A[11].
SD_BA[1:0]	O 8mA	SDRAM Bank Select **SD_BA[1:0]:** SDRAM bank select. Selects one bank out of four banks at SDRAM.
SD_CLK	O 8mA	SDRAM Clock **SD_CLK:** Drives the SDRAM clock towards the SDRAM.
SD_CS_N	O 8mA	SDRAM Chip Select (Active Low) **SD_CS_N:** SDRAM chip select towards SDRAM.
SD_WE_N	O 8mA	SDRAM Write Enable (Active Low) **SD_WE_N:** Write enable towards SDRAM.
SD_RAS_N	O 8mA	SDRAM Row Address Strobe Enable (Active Low) **SD_RAS_N:** Row address strobe towards SDRAM.
SD_CAS_N	O 8mA	SDRAM Column Address Strobe (Active Low) **SD_CAS_N:** Column address strobe towards SDRAM.
TDM-OVER-PACKET INTERFACE PINS		
TDM1_TX	O 8mA	TDM1 Transmit **TDM1_TX:** First interface serial transmit line. Also used in high-speed E3/T3/STS1 mode.
TDM1_RX	Ipu	TDM1 Receive **TDM1_RX:** First interface serial receive line. This pin is active in external mode only. Also used in high-speed E3/T3/STS1 mode.

NAME	TYPE	FUNCTION
TDM1_TCLK	Ipu	TDM1 Transmit Clock **TDM1_TCLK:** Used for clocking TDM1_TX and TDM1_RX lines in one-clock mode, or TDM1_TX in two-clock mode. This pin is active in external mode only. Also used in high-speed E3/T3/STS1 mode.
TDM1_RCLK	Ipu	TDM1 Receive Clock **TDM1_RCLK:** Used for clocking TDM1_RX line in two-clock mode. Not used in one-clock mode. This pin is active in external mode only. Also used in high-speed E3/T3/STS1 mode.
TDM1_ACLK	O 8mA	TDM1 Recovery Clock **TDM1_ACLK:** First interface recovered clock. Also used in high-speed E3/T3/STS1 mode.
TDM1_TX_SYNC	Ipd	TDM1 Transmit/Receive Sync Pulse **TDM1_TX_SYNC:** First interface transmit frame sync pulse. Used as both transmit and receive frame sync pulse in one-clock mode. Used as transmit frame sync in two-clock mode. The pulse frequency can be once every N x 125µs, i.e., every 2ms. This pin is active in external mode only.
TDM1_TX_MF_CD	IOpd	TDM1 Transmit Multiframe Sync Pulse/Carrier Detect **TDM1_TX_MF_CD:** First interface transmit multiframe sync pulse input for framed interface (PCM), or carrier detect output in case of serial interface. This pin is active in external mode only.
TDM1_RX_SYNC	Ipd	TDM1 Receive Multiframe Sync Pulse **TDM1_RX_SYNC:** First interface receive multiframe sync pulse or frame sync pulse input. When used as frame sync pulse the pulse frequency can be once every N x 125µs, i.e., every 2ms. This pin is active in external mode only.
TDM1_TSIG_CTS	O 8mA	TDM1 Transmit Signaling/Clear to Send **TDM1_TSIG_CTS:** First interface transmit signaling, or Clear To Send in case of serial interface.
TDM1_RSIG_RTS	Ipu	TDM1 Receive Signaling/Request To Send **TDM1_RSIG_RTS:** First interface serial Rx signaling input or Request To Send input in case of serial interface. This pin is active in external mode only.
TDM2_TX	O 8mA	TDM2 Transmit **TDM2_TX:** Second Interface serial transmit line.
TDM2_RX	Ipu	TDM2 Receive **TDM2_RX:** Second interface serial receive line. This pin is active in external mode only. This pin is active in external mode only.
TDM2_TCLK	Ipu	TDM2 Transmit Clock **TDM2_TCLK:** Used for clocking TDM2_TX and TDM2_RX lines in one-clock mode, or TDM2_TX in two-clock mode. This pin is active in external mode only. This pin is active in external mode only.
TDM2_RCLK	Ipu	TDM2 Receive Clock **TDM2_RCLK:** Used for clocking TDM2_RX line in two-clock mode. Not used in one-clock mode. This pin is active in external mode only.
TDM2_ACLK	O 8mA	TDM2 Recovery Clock **TDM2_ACLK:** Second interface recovered clock.
TDM2_TX_SYNC	Ipd	TDM2 Transmit/Receive Sync Pulse **TDM2_TX_SYNC:** Second interface transmit frame sync pulse. Used as both transmit and receive frame sync pulse in one-clock mode. Used as transmit frame sync in two-clock mode. The pulse frequency can be once every N x 125µs, i.e., every 2ms. This pin is active in external mode only.
TDM2_TX_MF_CD	IOpd	TDM2 Transmit Multiframe Sync Pulse/Carrier Detect **TDM2_TX_MF_CD:** Second interface transmit multiframe sync pulse input for framed interface (PCM), or carrier detect output in case of serial interface. This pin is active in external mode only.

NAME	TYPE	FUNCTION
TDM2_RX_SYNC	Ipd	TDM2 Receive Multiframe Sync Pulse **TDM2_RX_SYNC:** Second interface receive multiframe sync pulse or frame sync pulse input. When used as frame sync pulse the pulse frequency can be once every N x 125µs, i.e., every 2ms. This pin is active in external mode only.
TDM2_TSIG_CTS	O 8mA	TDM2 Transmit Signaling/Clear to Send **TDM2_TSIG_CTS:** Second interface transmit signaling, or Clear to Send in case of serial interface.
TDM2_RSIG_RTS	Ipu	TDM2 Receive Signaling/Request To Send **TDM2_RSIG_RTS:** Second interface serial Rx signaling input or Request To Send input in case of serial interface. This pin is active in external mode only.
TDM3_TX	O 8mA	TDM3 Transmit **TDM3_TX:** Third Interface serial transmit line.
TDM3_RX	Ipu	TDM3 Receive **TDM3_RX:** Third interface serial receive line. This pin is active in external mode only.
TDM3_TCLK	Ipu	TDM3 Transmit Clock **TDM3_TCLK:** Used for clocking TDM3_TX and TDM3_RX lines in one-clock mode, or TDM3_TX in two-clock mode. This pin is active in external mode only.
TDM3_RCLK	Ipu	TDM3 Receive Clock **TDM3_RCLK:** Used for clocking TDM3_RX line in two-clock mode. Not used in one-clock mode. This pin is active in external mode only.
TDM3_ACLK	O 8mA	TDM3 Recovery Clock **TDM3_ACLK:** Third interface recovered clock.
TDM3_TX_SYNC	Ipd	TDM3 Transmit/Receive Sync Pulse **TDM3_TX_SYNC:** First interface transmit frame sync pulse. Used as both transmit and receive frame sync pulse in one-clock mode. Used as transmit frame sync in two-clock mode. The pulse frequency can be once every N x 125µs, i.e., every 2ms. This pin is active in external mode only.
TDM3_TX_MF_CD	IOpd	TDM3 Transmit Multiframe Sync Pulse/Carrier Detect **TDM3_TX_MF_CD:** Third interface transmit multiframe sync pulse input for framed interface (PCM), or carrier detect output in case of serial interface. This pin is active in external mode only.
TDM3_RX_SYNC	Ipd	TDM3 Receive Multiframe Sync Pulse **TDM3_RX_SYNC:** Third interface receive multiframe sync pulse or frame sync pulse input. When used as frame sync pulse the pulse frequency can be once every N x 125µs, i.e., every 2ms. This pin is active in external mode only.
TDM3_TSIG_CTS	O 8mA	TDM3 Transmit Signaling/Clear to Send **TDM3_TSIG_CTS:** Third interface transmit signaling, or Clear to Send in case of serial interface.
TDM3_RSIG_RTS	Ipu	TDM3 Receive Signaling/Request To Send **TDM3_RSIG_RTS:** Third interface serial Rx signaling input or Request To Send input in case of serial interface. This pin is active in external mode only.
TDM4_TX	O 8mA	TDM4 Transmit **TDM4_TX:** Fourth Interface serial transmit line.
TDM4_RX	Ipu	TDM4 Receive **TDM4_RX**: Fourth interface serial receive line. This pin is active in external mode only.
TDM4_TCLK	Ipu	TDM4Transmit Clock **TDM4_TCLK:** Used for clocking TDM4_TX and TDM4_RX lines in one-clock mode, or TDM4_TX in two-clock mode. This pin is active in external mode only.
TDM4_RCLK	Ipu	TDM4 Receive Clock **TDM4_RCLK:** Used for clocking TDM4_RX line in two-clock mode. Not used in one-clock mode. This pin is active in external mode only.

NAME	TYPE	FUNCTION
TDM4_ACLK	O 8mA	TDM4 Recovery Clock **TDM4_ACLK:** Fourth interface recovered clock.
TDM4_TX_SYNC	Ipd	TDM4 Transmit/Receive Sync Pulse **TDM4_TX_SYNC:** Fourth interface transmit frame sync pulse. Used as both transmit and receive frame sync pulse in one-clock mode. Used as transmit frame sync in two-clock mode. The pulse frequency can be once every N x 125µs, i.e., every 2ms. This pin is active in external mode only.
TDM4_TX_MF_CD	IOpd	TDM4 Transmit Multiframe Sync Pulse/Carrier Detect **TDM4_TX_MF_CD:** Fourth interface transmit multiframe sync pulse input for framed interface (PCM), or carrier detect output in case of serial interface. This pin is active in external mode only.
TDM4_RX_SYNC	Ipd	TDM4 Receive Multiframe Sync Pulse **TDM4_RX_SYNC:** Fourth interface receive multiframe sync pulse or frame sync pulse input. When used as frame sync pulse the pulse frequency can be once every N x 125µs, i.e., every 2ms. This pin is active in external mode only.
TDM4_TSIG_CTS	O 8mA	TDM4 Transmit Signaling/Clear to Send **TDM4_TSIG_CTS_D2A4:** Fourth interface transmit signaling, or Clear to Send in case of serial interface.
TDM4_RSIG_RTS	Ipu	TDM4 Receive Signaling/Request To Send **TDM4_RSIG_RTS:** Fourth interface serial Rx signaling input or Request To Send input in case of serial interface. This pin is active in external mode only.
TDM5_TX	O 8mA	TDM5 Transmit **TDM5_TX:** Fifth Interface serial transmit line.
TDM5_RX	Ipu	TDM5 Receive **TDM5_RX:** Fifth interface serial receive line. This pin is active in external mode only.
TDM5_TCLK	Ipu	TDM5Transmit Clock **TDM5_TCLK:** Used for clocking TDM5_TX and TDM5_RX lines in one-clock mode, or TDM5_TX in two-clock mode. This pin is active in external mode only.
TDM5_RCLK	Ipu	TDM5 Receive Clock **TDM5_RCLK:** Used for clocking TDM5_RX line in two-clock mode. Not used in one-clock mode. This pin is active in external mode only.
TDM5_ACLK	O 8mA	TDM5 Recovery Clock **TDM5_ACLK:** Fifth interface recovered clock.
TDM5_TX_SYNC	Ipd	TDM5 Transmit/Receive Sync Pulse **TDM5_TX_SYNC:** Fifth interface transmit frame sync pulse. Used as both transmit and receive frame sync pulse in one-clock mode. Used as transmit frame sync in two-clock mode. The pulse frequency can be once every N x 125µs, i.e., every 2ms. This pin is active in external mode only.
TDM5_TX_MF_CD	IOpd	TDM5 Transmit Multiframe Sync Pulse/Carrier Detect **TDM5_TX_MF_CD:** Fifth interface transmit multiframe sync pulse input for framed interface (PCM), or Carrier Detect output in case of serial interface. This pin is active in external mode only.
TDM5_RX_SYNC	Ipd	TDM5 Receive Multiframe Sync Pulse **TDM5_RX_SYNC:** First interface receive multiframe sync pulse or frame sync pulse input. When used as frame sync pulse the pulse frequency can be once every N x 125µs, i.e., every 2ms. This pin is active in external mode only.
TDM5_TSIG_CTS	O 8mA	TDM5 Transmit Signaling/Clear to Send **TDM5_TSIG_CTS:** Fifth interface transmit signaling, or Clear to Send in case of serial interface.
TDM5_RSIG_RTS	Ipu	TDM5 Receive Signaling/Request To Send **TDM5_RSIG_RTS:** Fifth interface serial Rx signaling input or Request To Send input in case of serial interface. This pin is active in external mode only.

NAME	TYPE	FUNCTION
TDM6_TX	O 8mA	TDM6 Transmit **TDM6_TX:** Sixth Interface serial transmit line.
TDM6_RX	Ipu	TDM6 Receive **TDM6_RX:** Sixth interface serial receive line. This pin is active in external mode only.
TDM6_TCLK	Ipu	TDM6Transmit Clock **TDM6_TCLK:** Used for clocking TDM6_TX and TDM6_RX lines in one-clock mode, or TDM6_TX in two-clock mode. This pin is active in external mode only.
TDM6_RCLK	Ipu	TDM6 Receive Clock **TDM6_RCLK:** Used for clocking TDM6_RX line in two-clock mode. Not used in one-clock mode. This pin is active in external mode only.
TDM6_ACLK	O 8mA	TDM6 Recovery Clock **TDM6_ACLK:** Sixth interface recovered clock.
TDM6_TX_SYNC	Ipd	TDM6 Transmit/Receive Sync Pulse **TDM6_TX_SYNC:** Sixth interface transmit frame sync pulse. Used as both transmit and receive frame sync pulse in one-clock mode. Used as transmit frame sync in two-clock mode. The pulse frequency can be once every N x 125μs, i.e., every 2ms. This pin is active in external mode only.
TDM6_TX_MF_CD	IOpd	TDM6 Transmit Multiframe Sync Pulse/Carrier Detect **TDM6_TX_MF_CD:** Sixth interface transmit multiframe sync pulse input for framed interface (PCM), or carrier detect output in case of serial interface. This pin is active in external mode only.
TDM6_RX_SYNC	Ipd	TDM6 Receive Multiframe Sync Pulse **TDM6_RX_SYNC:** Sixth interface receive multiframe sync pulse or frame sync pulse input. When used as frame sync pulse the pulse frequency can be once every N x 125μs, i.e., every 2ms. This pin is active in external mode only.
TDM6_TSIG_CTS	O 8mA	TDM6 Transmit Signaling/Clear to Send **TDM6_TSIG_CTS:** Sixth interface transmit signaling, or Clear to Send in case of serial interface.
TDM6_RSIG_RTS	Ipu	TDM6 Receive Signaling/Request To Send **TDM6_RSIG_RTS:** Sixth interface serial Rx signaling input or Request To Send input in case of serial interface. This pin is active in external mode only.
TDM7_TX	O 8mA	TDM7 Transmit **TDM7_TX:** Seventh Interface serial transmit line.
TDM7_RX	Ipu	TDM7 Receive **TDM7_RX:** Seventh interface serial receive line. This pin is active in external mode only.
TDM7_TCLK	Ipu	TDM7Transmit Clock **TDM7_TCLK:** Used for clocking TDM7_TX and TDM7_RX lines in one-clock mode, or TDM7_TX in two-clock mode. This pin is active in external mode only.
TDM7_RCLK	Ipu	TDM7 Receive Clock **TDM7_RCLK:** Used for clocking TDM7_RX line in two-clock mode. Not used in one-clock mode. This pin is active in external mode only.
TDM7_ACLK	O 8mA	TDM7 Recovery Clock **TDM7_ACLK:** Seventh interface recovered clock.
TDM7_TX_SYNC	Ipd	TDM7 Transmit/Receive Sync Pulse **TDM7_TX_SYNC:** Seventh interface transmit frame sync pulse. Used as both transmit and receive frame sync pulse in one-clock mode. Used as transmit frame sync in two-clock mode. The pulse frequency can be once every N x 125μs, i.e., every 2ms. This pin is active in external mode only.
TDM7_TX_MF_CD	IOpd	TDM7 Transmit Multiframe Sync Pulse/Carrier Detect **TDM7_TX_MF_CD:** Fifth interface transmit multiframe sync pulse input for framed interface (PCM), or carrier detect output in case of serial interface. This pin is active in external mode only.

NAME	TYPE	FUNCTION
TDM7_RX_SYNC	Ipd	TDM7 Receive Multiframe Sync Pulse **TDM7_RX_SYNC:** Seventh interface receive multiframe sync pulse or frame sync pulse input. When used as frame sync pulse the pulse frequency can be once every N x 125µs, i.e., every 2ms. This pin is active in external mode only.
TDM7_TSIG_CTS	O 8mA	TDM7 Transmit Signaling/Clear to Send **TDM7_TSIG_CTS:** Seventh interface transmit signaling, or Clear to Send in case of serial interface.
TDM7_RSIG_RTS	Ipu	TDM7 Receive Signaling/Request To Send **TDM7_RSIG_RTS:** Seventh interface serial Rx signaling input or Request To Send input in case of serial interface. This pin is active in external mode only.
TDM8_TX	O 8mA	TDM8 Transmit **TDM8_TX:** Eighth interface serial transmit line.
TDM8_RX	Ipu	TDM8 Receive **TDM8_RX:** Eighth interface serial receive line. This pin is active in external mode only.
TDM8_TCLK	Ipu	TDM8 Transmit Clock **TDM8_TCLK:** Used for clocking TDM8_TX and TDM8_RX lines in one-clock mode, or TDM8_TX in two-clock mode. This pin is active in external mode only.
TDM8_RCLK	Ipu	TDM8 Receive Clock **TDM8_RCLK:** Used for clocking TDM8_RX line in two-clock mode. Not used in one-clock mode. This pin is active in external mode only.
TDM8_ACLK	O 8mA	TDM8 Recovery Clock **TDM8_ACLK:** Eighth interface recovered clock.
TDM8_TX_SYNC	Ipd	TDM8 Transmit/Receive Sync Pulse **TDM8_TX_SYNC:** Eighth interface transmit frame sync pulse. Used as both transmit and receive frame sync pulse in one-clock mode. Used as transmit frame sync in two-clock mode. The pulse frequency can be once every N x 125µs, i.e., every 2ms. This pin is active in external mode only.
TDM8_TX_MF_CD	IOpd	TDM8 Transmit Multiframe Sync Pulse/Carrier Detect **TDM8_TX_MF_CD:** Eighth interface transmit multiframe sync pulse input for framed interface (PCM), or carrier detect output in case of serial interface. This pin is active in external mode only.
TDM8_RX_SYNC	Ipd	TDM8 Receive Multiframe Sync Pulse **TDM8_RX_SYNC:** First interface receive multiframe sync pulse or frame sync pulse input. When used as frame sync pulse the pulse frequency can be once every N x 125µs, i.e., every 2ms. This pin is active in external mode only.
TDM8_TSIG_CTS	O 8mA	TDM8 Transmit Signaling/Clear to Send **TDM8_TSIG_CTS:** Eighth interface transmit signaling, or Clear to Send in case of serial interface. This pin is active in external mode only.
TDM8_RSIG_RTS	Ipu	TDM8 Receive Signaling/Request To Send **TDM8_RSIG_RTS:** Eighth interface serial Rx signaling input or Request To Send input in case of serial interface. This pin is active in external mode only.
MAC(10/100) PINS		
CLK_MII_RX	I	Clock Media Independent Interface Receive **CLK_MII_RX:** MII receive clock or SSMII receive clock.
MII_RXD[0]	I	Media Independent Interface Receive Data 0 **MII_RXD[0]:** MII receive data ‘0’ or SSMII receive data.
MII_RXD[1]	I	Media Independent Interface Receive Data 1 **MII_RXD[1]:** MII receive data ‘1’ or receive data SSMII sync.
MII_RXD[2]	I	Media Independent Interface Receive Data 2 **MII_RXD[2]:** MII receive data ‘2’ or RMII receive data ‘0.’
MII_RXD[3]	I	Media Independent Interface Receive Data 3 **MII_RXD[3]:** MII receive data ‘3’ or RMII receive data ‘1.’

NAME	TYPE	FUNCTION
MII_RX_DV	I	Media Independent Interface Receive Data Valid **MII_RX_DV:** MII receive data valid, or RMII carrier sense/data valid.
MII_RX_ERR	I	Media Independent Interface Receive Error **MII_RX_ERR:** MII receive error, or RMII receive error.
MII_COL	I	Media Independent Interface Collision **MII_COL:** MII collision detection.
MII_CRS	I	Media Independent Interface carrier sense. **MII_CRS:** MII carrier sense.
CLK_MII_TX	I	Clock Media Independent Interface Transmit **CLK_MII_TX:** MII transmit clock or RMII ref clock or SSMII ref clock.
CLK_SSMII_TX	O 12mA	Clock Source Synchronous Serial Media Independent Interface Transmit **CLK_SSMII_TX:** SSMII transmit clock (125MHz).
MII_TXD[0]	O 8mA	Media Independent Interface Transmit Data 0 **MII_TXD[0]:** MII transmit data ‘0’, or SSMII transmit data.
MII_TXD[1]	O 8mA	Media Independent Interface Transmit Data 1 **MII_TXD[1]:** MII transmit data ‘0’, or SSMII transmit sync.
MII_TXD[2]	O 8mA	Media Independent Interface Transmit Data 2 **MII_TXD[2]:** MII transmit data ‘2’ or RMII transmit data ‘0.’
MII_TXD[3]	O 8mA	Media Independent Interface Transmit Data 3 **MII_TXD[3]:** MII transmit data ‘3’, or RMII transmit data ‘1.’
MII_TX_EN	O 8mA	Media Independent Interface Transmit Enable **MII_TX_EN:** MII transmit enable or RMII transmit enable.
MII_TX_ERR	O 8mA	Media Independent Interface Transmit Error **MII_TX_ERR:** MII transmit error.
MDIO	IOpu 8mA	Management Data Input/Output **MDIO:** Management data, synchronized to MDC.
MDC	O 8mA	Management Data Clock **MDC:** Management data clock.
FRAMER AND LIU PORT PINS		
TTIP1 TTIP2 TTIP3 TTIP4 TTIP5 TTIP6 TTIP7 TTIP8	Oa	Transmit Bipolar Tip for Channels 1–8 **TTIPn:** These pins are differential line driver tip outputs. The differential outputs of TTIPn and TRINGn can provide internal matched impedance for E1 75Ω, E1 120Ω, T1 100Ω, or J1 110Ω. **Note:** All these pins can be tri-stated when the TXENABLE pin is low.
TRING1 TRING2 TRING3 TRING4 TRING5 TRING6 TRING7 TRING8	Oa	Transmit Bipolar Ring for Channels 1–8 **TRINGn:** These pins are differential line driver ring outputs. The differential outputs of TTIPn and TRINGn can provide internal matched impedance for E1 75Ω, E1 120Ω, T1 100Ω, or J1 110Ω. **Note:** All these pins can be tri-stated when the TXENABLE pin is low.
TXENABLE	I	Transmit Enable for all Channels 1–8 **TXENABLE:** If this pin is pulled low all the transmitter outputs (TTIP and TRING) are high impedance. In addition, the register settings for tri-state control of TTIP/TRING are ignored if TXENABLE is low. If TXENABLE is high, the particular driver can be tri-stated if the TXEN bit is set in the LMCR register.

NAME	TYPE	FUNCTION
RTIP1 RTIP2 RTIP3 RTIP4 RTIP5 RTIP6 RTIP7 RTIP8	Ia	Receive Bipolar Tip for Channels 1–8 **RTIPn:** Receive analog input for differential receiver. Data and clock are recovered and output at RPOS/RNEG and RCLK pins, respectively. The differential inputs of RTIPn and RRINGn can provide internal matched impedance for E1 75Ω, E1 120Ω, T1 100Ω, or J1 110Ω.
RRING1 RRING2 RRING3 RRING4 RRING5 RRING6 RRING7 RRING8	Ia	Receive Bipolar Ring for Channels 1–8 **RRINGn:** Receive analog input for differential receiver. Data and clock are recovered and output at RPOS/RNEG and RCLK pins, respectively. The differential inputs of RTIPn and RRINGn can provide internal matched impedance for E1 75Ω, E1 120Ω, T1 100Ω, or J1 110Ω.
RXTSEL	I	Receive Termination Selection **RXTSEL:** The input selects internal termination when high and external termination when low for the all the receivers when the RHPM bit is set in the LTRCR register.
RCLKF1/RCLK1 RCLKF2/RCLK2 RCLKF3/RCLK3 RCLKF4/RCLK4 RCLKF5/RCLK5 RCLKF6/RCLK6 RCLKF7/RCLK7 RCLKF8/RCLK8	IO 8mA	Receive Framer Clock **RCLKFn:** When the LIUs are disabled (GCR2.LIUDn bits), RCLKFn can be 1.544MHz (T1) or 2.048MHz (E1) input clock that is used to clock data through the receive-side framer. RSER data is output on the rising edge of RCLKFn. RCLKFn is used to output RSER when the elastic store is not enabled. When the elastic store is enabled, the RSER is clocked by RSYSCLK. Receive Clock Out **RCLKn:** When the LIU is used RCLKn is the recovered output clock from the line. This clock is recovered from the signal at RTIP and RRING. The output is 1.544MHz for T1 and 2.048MHz for E1. This clock is used to clock data through the receive-side framer. RSER data is output on the rising edge of RCLKn. RCLKn is used to output RSER when the elastic store is not enabled. When the elastic store is enabled, the RSER is clocked by RSYSCLK.
TCLKF1 TCLKF2 TCLKF3 TCLKF4 TCLKF5 TCLKF6 TCLKF7 TCLKF8	I	Transmit Clock Input for the Formatter **TCLKFn:** A 1.544MHz or a 2.048MHz primary clock. Used to clock data through the transmit-side formatter. This pin is active in external mode.
TCLKO1 TCLKO2 TCLKO3 TCLKO4 TCLKO5 TCLKO6 TCLKO7 TCLKO8	O 8mA	Transmit Clock Output **TCLKOn:** This signal is used to register the TDATFn output and is typically synchronous with the TCLKFn input. However, in framer and payload loopback applications this signal becomes synchronous with RCLKFn.

NAME	TYPE	FUNCTION
RSER1 RSER2 RSER3 RSER4 RSER5 RSER6 RSER7 RSER8	O 8mA	Receive Serial Data Output **RSERn:** Received NRZ serial data. Updated on rising edges of RCLKFn when the receive-side elastic store is disabled. Updated on the rising edges of RSYSCLKn when the receive-side elastic store is enabled. This output is low when in internal mode.
TDATF1 TDATF2 TDATF3 TDATF4 TDATF5 TDATF6 TDATF7 TDATF8	O 8mA	Transmit Data Formatter Output **TDATFn:** Can be programmed to source NRZ data via a configuration register. This pin is low when the internal LIU is enabled. This is active when the internal LIUn is disabled (GCR2.LIUD bit).
RSYNC1 RSYNC2 RSYNC3 RSYNC4 RSYNC5 RSYNC6 RSYNC7 RSYNC8	IO 8mA	Receive Sync **RSYNCn:** If the receive-side elastic store is enabled, then this signal is used to input a frame or multiframe boundary pulse. If set to output frame boundaries then RSYNC can be programmed to output double-wide pulses on signaling frames in T1 mode. In E1 Mode RSYNC out can be used to indicate CAS and CRC4 multiframe.
RSYSCLK1 RSYSCLK2 RSYSCLK3 RSYSCLK4 RSYSCLK5 RSYSCLK6 RSYSCLK7 RSYSCLK8	I	Receive System Clock **RSYSCLKn:** 1.544MHz, or 2.048MHz receive backplane clock. Only used when the receive side elastic store function is enabled. Should be tied low in applications that do not use the receive side elastic store. This pin is active in external mode only.
RF/RMSYNC1 RF/RMSYNC2 RF/RMSYNC3 RF/RMSYNC4 RF/RMSYNC5 RF/RMSYNC6 RF/RMSYNC7 RF/RMSYNC8	O 8mA	Frame Synchronization **RFSYNCn:** RFSYNC is an extracted 8kHz pulse, one RCLKF or RCLK wide that identifies frame boundaries. Receive Multiframe Synchronization **RMSYNCn:** RMSYNC is an extracted pulse, one RCLKF or RCLK wide (elastic store disabled) or one RSYSCLK wide (elastic store enabled), which identifies multiframe boundaries. When the receive elastic store is enabled, the RMSYNC signal indicates the multiframe sync on the system (backplane) side of the elastic store. In E1 mode, will indicate either the CRC4 or CAS multiframe as determined by a configuration register.
RLOF/RLOS1 RLOF/RLOS2 RLOF/RLOS3 RLOF/RLOS4 RLOF/RLOS5 RLOF/RLOS6 RLOF/RLOS7 RLOF/RLOS8	O 8mA	Receive Loss of Frame **RLOFn:** This pin can toggle high when the synchronizer is searching for the frame and multiframe. Receive Loss of Signal **RLOSn:** This pin can toggle high when the framer detects a loss of signal condition.

NAME	TYPE	FUNCTION
TSER1 TSER2 TSER3 TSER4 TSER5 TSER6 TSER7 TSER8	I	Transmit Serial Data **TSERn:** Sampled on the falling edge of TCLKF when the transmit side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit side elastic store is enabled. This pin is active in external mode only.
RDATF1 RDATF2 RDATF3 RDATF4 RDATF5 RDATF6 RDATF7 RDATF8	I	Receive Data Framer input **RDATFn:** RDATFn can be used for unipolar (NRZ) data if enabled. This is active when the internal LIUn is disabled (GCR2.LIUD bit).
TSYNC/TSSYNC1 TSYNC/TSSYNC2 TSYNC/TSSYNC3 TSYNC/TSSYNC4 TSYNC/TSSYNC5 TSYNC/TSSYNC6 TSYNC/TSSYNC7 TSYNC/TSSYNC8	IO 8mA	Transmit Synchronization In/Out **TSYNCn:** A pulse at this pin establishes either frame or multiframe boundaries for the transmit side. This signal can additionally be programmed to output either a frame or multiframe pulse. If this pin is set to output pulses at frame boundaries, it can additionally be set to output doublewide pulses at signaling frames in T1 mode. The operation of this signal is synchronous with TCLKF. Only used when elastic store is disabled. Transmit System Synchronization In **TSSYNCn:** Only used when the transmit-side elastic store is enabled. A pulse at this pin will establish either frame or multiframe boundaries for the transmit side. The operation of this signal is synchronous with TSYSCLK.
TSYSCLK/ECLK1 TSYSCLK/ECLK2 TSYSCLK/ECLK3 TSYSCLK/ECLK4 TSYSCLK/ECLK5 TSYSCLK/ECLK6 TSYSCLK/ECLK7 TSYSCLK/ECLK8	I	Transmit System Clock **TSYSCLKn:** 1.544MHz or 2.048MHz clock. Only used when the transmit-side elastic store function is enabled. This pin is active in external mode. External Clock **ECLK:** This pin is an external clock input for the receive and transmit. The pins is configured by register FMRTOPISM.
CLOCK PINS		
CLK_SYS_S	Ipd	System Clock Select **CLK_SYS_S:** This pin selects the input CLK_SYS frequency. The pin should be tied high when a 25MHz CLK_SYS is used. The pin should be tied low or left unconnected when a 50MHz or 75MHz CLK_SYS is used.
CLK_SYS	I	System Clock **CLK_SYS:** Clock input used to drive the TDM-over-Packet internal circuitry. Requires a 25MHz or 50MHz or 75MHz(±50ppm or better) clock on this pin. The 25MHz CLK_SYS is used to generate a 50MHz or 75MHz internal system clock for the TDM-over-Packet and SD_CLK. The 50MHz or 75MHz CLK_SYS is used for the SD_CLK output, and the internal system clock for the TDM-over-Packet block.

NAME	TYPE	FUNCTION
CLK_HIGH	I	Clock High Synthesis **CLK_HIGH:** 19.44MHz or 38.88MHz or 77.76MHz clock input is used for E1/T1 clock recovery machines of the TDM-over-Packet and the internal MCLK for the LIU and Framer. The LIU and FRAMER use this clock as the internal MCLK when programmed in default mode. A configuration register sets if the clock input is going to be 10.00MHz or 19.44MHz or 38.88MHz or 77.76MHz. It is recommend that this signal be tied to DVSS when none of the recovered clock outputs (TDM1_ACLK–TDM8_ACLK) are used or when the chip is in single-port high-speed mode. Accuracy is described in the *Clock Recovery* section (Section 7.7.4).
MCLK	I	Master Clock **MCLK:** This is an independent free-running clock whose input can be 2.048MHz ±50ppm or 1.544MHz ±32ppm. An external MCLK is used when not using the TDM-over-Packet engine CLK_HIGH. The user must program this pin to be used as the external MCLK source. When using this MCLK pin set MCLKE bit and set MCLKS bit for correct operation as described in the GCR1 register.
CLK_CMN	I	Common Clock **CLK_CMN:** Common clock has to be a multiple of 8kHz and in the range of 1MHz to 25MHz. The frequency input should not be too close to an integer multiple of the service clock frequency. Based on these criteria, the following frequencies are suggested: For systems with access to a common SONET/SDH network, a frequency of 19.44MHz (2430 x 8kHz). For systems with access to a common ATM network, 9.72MHz (1215 x 8kHz) or 19.44MHz (2430 x 8kHz). For systems using GPS, 8.184MHz (1023 x 8kHz). For systems connected by a single hop of 100Mbps Ethernet where it is possible to lock the physical layer clock, 25MHz (3125 x 8kHz). When common clock is not used tie to ground or VDD(3.3V).
MICROPROCESSOR PINS		
H_D[31:1]	IO 8mA	Host Data Bus **H_D[31:1]:** Host data bus MSB is HD[31] when the host data bus width is 32 bits and HD_D[15] when the host data bus width is 16 bits.
H_D[0]/ SPI_MISO	IO 8mA	Host Data Bus **H_D[0]:** In CPU mode (H_CPU_SPI_N = 1), this pin is used as H_D[0], which is the LSB of the CPU data bus. SPI MISO **SPI_MISO[0]:** In SPI mode (H_CPU_SPI = 0), this pin is used as SPI_MISO output. If the SPI interface is not selected(SPI_SEL_N), this output is tri-state.
H_AD[24:1]	I	Host Address Bus **H_AD[24:1]:** Host address bus, MSB is H_AD[24]. When the host data bus is 32 bits, H_AD[1] should be tied to VSS.
H_CS_N	I	Host Chip Select **H_CS_N:** Host chip select active low.
H_R_W_N/ SPI_CP	I	Host Read/Write **H_R_W_N:** In CPU mode (H_CPU_SPI_N = 1), this input is host read/write. SPI Clock Phase **SPU_CP:** In SPI mode (H_CPU_SPI_N = 0), this input is the SPI clock phase.

NAME	TYPE	FUNCTION
H_WR_BE0_N/ SPI_CLK	I	H_D[7:0] Write Enable, Active Low **H_WR_BE0_N:** In CPU mode (H_CPU_SPI_N = 1) this input is H_D[7:0] write enable, active low. SPI Clock **SPI_CLK:** In SPI mode (H_CPU_SPI_N = 0), this input is SPI clock.
H_WR_BE1_N/ SPI_MOSI	I	H_D[15:8] Write Enable, Active Low **H_WR_BE1_N:** In CPU mode (H_CPU_SPI_N = 1), this input is H_D[15:8] write enable, active low. SPI_MOSI **SPI_MOSI:** In SPI mode (H_CPU_SPI_N = 0), this input is SPI_MOSI.
H_WR_BE2_N/ SPI_SEL_N	I	H_D[23:16] Write Enable, Active Low **H_WR_BE2_N:** In CPU mode (H_CPU_SPI_N = 1), this input is H_D[23:16] write enable, active low. SPI Select **SPI_SEL_N:** In SPI mode (H_CPU_SPI_N = 0), this input is SPI_SEL_N.
H_WR_BE3_N/ SPI_CI	I	H_D[31:24] Write Enable, Active Low **H_WR_BE3_N:** In CPU mode (H_CPU_SPI_N = 1), H_D[31:24] write enable, active low. SPI Clock Invert **SPI_CI:** In SPI mode (H_CPU_SPI_N = 0), this input is clock invert for SPI mode.
H_READY_N	Opu 8mA	Host Ready **H_READY_N:** Host ready, active low. This pin requires the use of an external pullup resistor. The signal is actively driven high ‘1’ before it becomes tri-state.
H_INT[1:0]	O 8mA	Host Interrupt **H_INT[1:0]:** Host Interrupts are active low. H_INT[0] is used for the TDM-over-Packet and H_INT[1] is used for the LIU, FRAMER and BERT. H_INT[0] can also be ORed with H_INT[1]. See register bit GCR1.IPOR.
DAT_32_16_N	Ipu	Data 32/16-Bit Select **DAT_32_16_N:** Selects the host data bus width to be ‘16’ when low ‘0’ and ‘32’ when high ‘1’. This pin is ignored in SPI mode.
H_CPU_SPI_N	Ipu	SPI Mode **H_CPU_SPI_N:** ‘0’ – SPI mode, CPU bus is disabled, ‘1’ – Regular CPU bus
MISCELLANEOUS PINS		
RST_SYS_N	Ipu	System Reset **RST_SYS_N:** System reset, active low.
JTMS	Ipu	JTAG Test Mode Select **JTMS:** This pin is sampled on the rising edge of JTCLK and is used to place the test access port into the various defined IEEE 1149.1 states. This pin has a 10kΩ pullup resistor.
JTCLK	I	JTAG Test Clock **JTCLK:** This signal is used to shift data into JTDI on the rising edge and out of JTDO on the falling edge.
JTDI	Ipu	JTAG Test Data In **JTDI:** Test instructions and data are clocked into this pin on the rising edge of JTCLK. This pin has a 10kΩ pullup resistor.
JTDO	Oz 8mA	JTAG Test Data Out **JTDO:** Test instructions and data are clocked out of this pin on the falling edge of JTCLK. If not used, this pin should be left unconnected.

NAME	TYPE	FUNCTION
JTRST	Ipu	JTAG Test Reset **JTRST:** JTRST is used to asynchronously reset the test access port controller. After power-up, JTRST must be toggled from low to high. This action sets the device into the JTAG DEVICE ID mode. Pulling JTRST low restores normal device operation. JTRST is pulled HIGH internally via a 10kΩ resistor operation. If boundary scan is not used, this pin should be held low.
RESREF	I	Resistor Reference **RESREF:** Requires a 10kΩ precision resistor (1% or better) to ground. This is used to calibrate the termination resistors internal to the part and the transmit impedance.
TEST PINS		
SCEN	Ipd	Scan Enable **SCEN:** Used during factory test. This pin should be a “No Connect.”
STMD	Ipd	Scan Test Mode **STMD:** Used during factory test. This pin should be a “No Connect.”
HIZ_N	I	High-Impedance Test Enable (Active Low) **HIZ_N:** This signal is used to enable testing. When this signal is low while JTRST is low, all the digital output and bidirectional pins are placed in the high-impedance state. For normal operation this signal is high. This is an asynchronous input.
MBIST_EN	I	Used during factory test. Tie to DVSS.
MBIST_DONE	O	Used during factory test. This pin should be a “No Connect.”
MBIST_FAIL	O	Used during factory test. This pin should be a “No Connect.”
TEST_CLK	O	Test Clock **TEST_CLK:** Used during factory test. This pin should be a “No Connect.”
TST_CLD	I	Test CLAD **TST_CLD:** Used during factory test. Tie to DVSS.
TST_TA	O	Test Transmit Probe A **TST_TA:** Used during factory test. This pin should be a “No Connect.”
TST_TB	O	Test Transmit Probe B **TST_TB:** Used during factory test. This pin should be a “No Connect.”
TST_TC	O	Test Transmit Probe C **TST_TC:** Used during factory test. This pin should be a “No Connect.”
TST_RA	O	Test Receiver Probe A **TST_RA:** Used during factory test. This pin should be a “No Connect.”
TST_RB	O	Test Receiver Probe A **TST_RA:** Used during factory test. This pin should be a “No Connect.”
TST_RC	O	Test Receiver Probe A **TST_RA:** Used during factory test. This pin should be a “No Connect.”

NAME	TYPE	FUNCTION
POWER PINS		
DVSS	—	Digital Ground for Framers and TDM-over-Packet (31 pins)
DVDDC	—	1.8V Core Supply Voltage for Framers and TDM-over-Packet (17 pins)
DVDDIO	—	3.3V Supply Voltage for IO (16 pins)
DVSSLIU	—	Digital Ground for LIUs (2 pins)
DVDDLIU	—	3.3V Digital Supply for LIUs (2 pins)
ATVDD1 ATVDD2 ATVDD3 ATVDD4 ATVDD5 ATVDD6 ATVDD7 ATVDD8	—	3.3V Power Supply for the Transmitter. All ATVDD pins need to be 3.3V.
ATVSS1 ATVSS2 ATVSS3 ATVSS4 ATVSS5 ATVSS6 ATVSS7 ATVSS8	—	Analog Ground for Transmitters
ARVDD1 ARVDD2 ARVDD3 ARVDD4 ARVDD5 ARVDD6 ARVDD7 ARVDD8	-	3.3V Analog Receive Power Supply
ARVSS1 ARVSS2 ARVSS3 ARVSS4 ARVSS5 ARVSS6 ARVSS7 ARVSS8	—	Analog Receive Ground
ACVDD2	—	1.8V Analog CLAD Power Supply 2 Used for CLK_HIGH Adaption
ACVDD1	—	1.8V Analog CLAD Power Supply 1
ACVSS2	—	Analog CLAD GND2 Used for CLK_HIGH Adaption
ACVSS1	—	Analog CLAD GND1

Note: *Pins with names ending in an asterisk (*) or "_N" are active low.*

11. JTAG Information

For the latest JTAG model search under www.maxim-ic.com/tools/bsdl/.

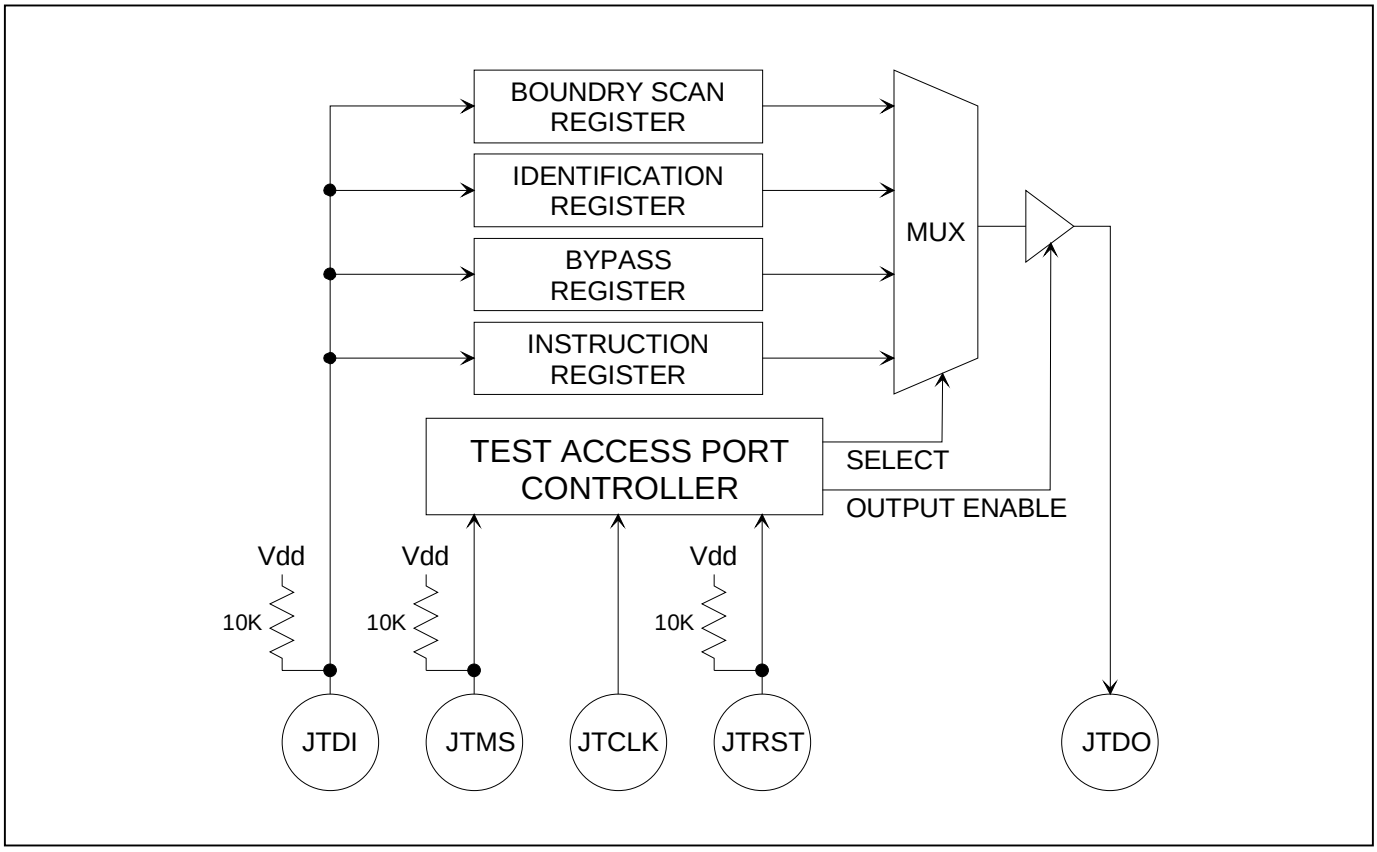
11.1 JTAG Description

The DS34T108 supports the standard instruction codes SAMPLE/PRELOAD, BYPASS, and EXTEST. Optional public instructions included are HIGHZ, CLAMP and IDCODE. See Figure 11-1 for a JTAG block diagram. The DS34T108 contains the following items that meet the requirements set by the IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture:

- Test Access Port (TAP)
- TAP Controller
- Instruction Register
- Bypass Register
- Boundary Scan Register
- Device Identification Register

The Test Access Port has the necessary interface pins, namely JTCLK, JTRST, JTDI, JTDO, and JTMS. Details on these pins can be found in Section 10.2. Details on the Boundary Scan Architecture and the Test Access Port can be found in IEEE 1149.1-1990, IEEE 1149.1a-1993, and IEEE 1149.1b-1994.

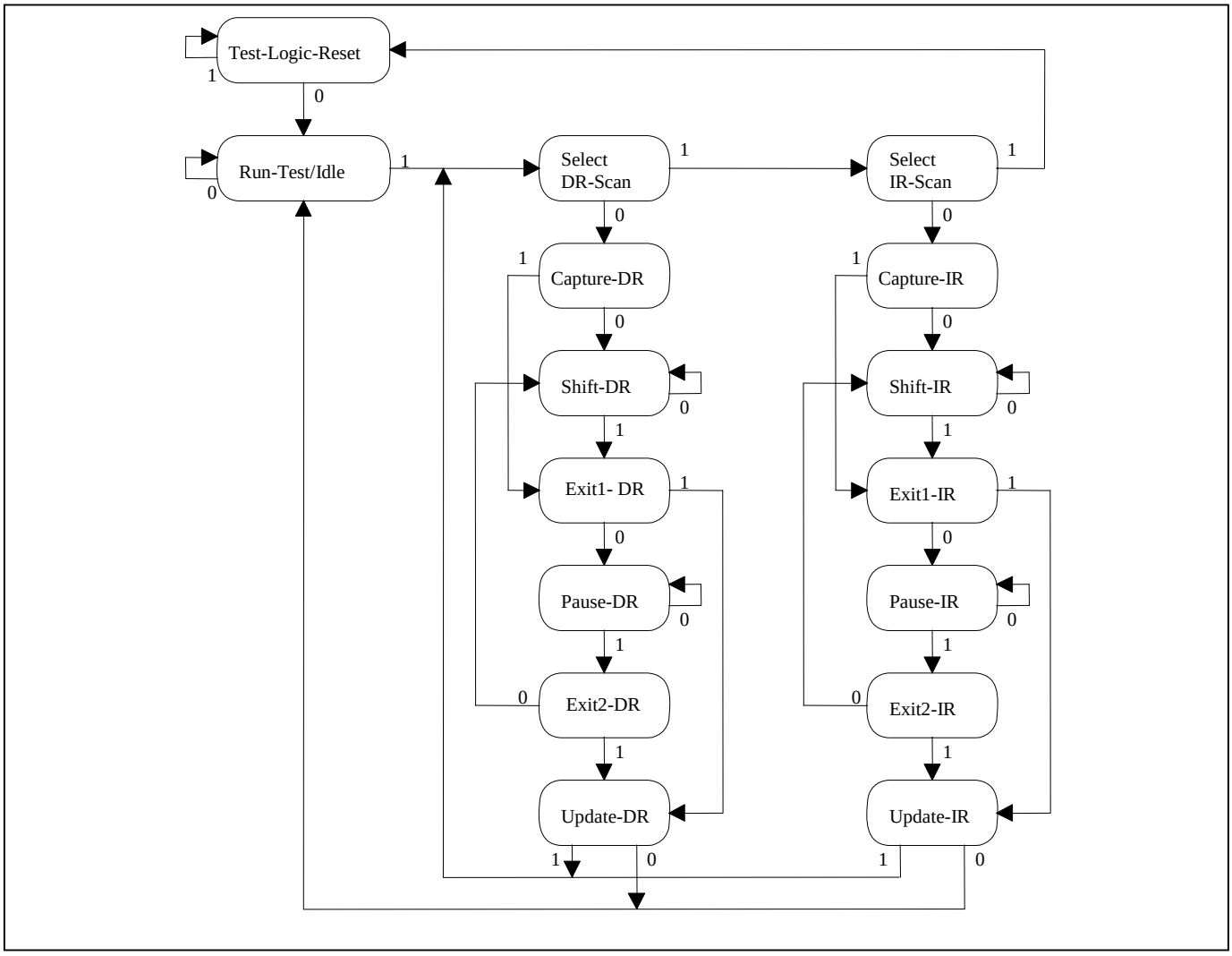
Figure 11-1. JTAG Block Diagram



11.2 JTAG TAP Controller State Machine Description

This section covers the details on the operation of the Test Access Port (TAP) Controller State Machine. See Figure 11-2 for details on each of the states described below. The TAP controller is a finite state machine that responds to the logic level at JTMS on the rising edge of JTCLK.

Figure 11-2. JTAG TAP Controller State Machine



Test-Logic-Reset. Upon device power-up, the TAP controller starts in the Test-Logic-Reset state. The Instruction Register contains the IDCODE instruction. All system logic on the device operates normally.

Run-Test-Idle. Run-Test-Idle is used between scan operations or during specific tests. The Instruction Register and Test Register remain idle.

Select-DR-Scan. All test registers retain their previous state. With JTMS low, a rising edge of JTCLK moves the controller into the Capture-DR state and initiates a scan sequence. JTMS high moves the controller to the Select-IR-SCAN state.

Capture-DR. Data can be parallel loaded into the test data registers selected by the current instruction. If the instruction does not call for a parallel load or the selected register does not allow parallel loads, the test register remains at its current value. On the rising edge of JTCLK, the controller goes to the Shift-DR state if JTMS is low or it to the Exit1-DR state if JTMS is high.

Shift-DR. The test data register selected by the current instruction is connected between JTDI and JTDO and shifts data one stage towards its serial output on each rising edge of JTCLK. If a test register selected by the current instruction is not placed in the serial path, it maintains its previous state.

Exit1-DR. While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state, which terminates the scanning process. A rising edge on JTCLK with JTMS low puts the controller in the Pause-DR state.

Pause-DR. Shifting of the test registers is halted while in this state. All test registers selected by the current instruction retain their previous state. The controller remains in this state while JTMS is low. A rising edge on JTCLK with JTMS high puts the controller in the Exit2-DR state.

Exit2-DR. While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state and terminates the scanning process. A rising edge on JTCLK with JTMS low puts the controller in the Shift-DR state.

Update-DR. A falling edge on JTCLK while in the Update-DR state latches the data from the shift register path of the Test registers into the data output latches. This prevents changes at the parallel output due to changes in the shift register. A rising edge on JTCLK with JTMS low puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

Select-IR-Scan. All Test registers retain their previous state. The Instruction register remains unchanged during this state. With JTMS low, a rising edge on JTCLK moves the controller into the Capture-IR state and initiates a scan sequence for the Instruction register. JTMS high during a rising edge on JTCLK puts the controller back into the Test-Logic-Reset state.

Capture-IR. The Capture-IR state is used to load the shift register in the Instruction register with a fixed value. This value is loaded on the rising edge of JTCLK. If JTMS is high on the rising edge of JTCLK, the controller enters the Exit1-IR state. If JTMS is low on the rising edge of JTCLK, the controller enters the Shift-IR state.

Shift-IR. In this state, the shift register in the Instruction register is connected between JTDI and JTDO and shifts data one stage for every rising edge of JTCLK towards the serial output. The parallel register as well as all test registers remain at their previous states. A rising edge on JTCLK with JTMS high moves the controller to the Exit1-IR state. A rising edge on JTCLK with JTMS low keeps the controller in the Shift-IR state while moving data one stage through the Instruction shift register.

Exit1-IR. A rising edge on JTCLK with JTMS low puts the controller in the Pause-IR state. If JTMS is high on the rising edge of JTCLK, the controller enters the Update-IR state and terminates the scanning process.

Pause-IR. Shifting of the Instruction register is halted temporarily. With JTMS high, a rising edge on JTCLK puts the controller in the Exit2-IR state. The controller remains in the Pause-IR state if JTMS is low during a rising edge on JTCLK.

Exit2-IR. A rising edge on JTCLK with JTMS high put the controller in the Update-IR state. The controller loops back to the Shift-IR state if JTMS is low during a rising edge of JTCLK in this state.

Update-IR. The instruction shifted into the Instruction shift register is latched into the parallel output on the falling edge of JTCLK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on JTCLK with JTMS low puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

11.3 JTAG Instruction Register and Instructions

The instruction register contains a shift register as well as a latched parallel output, and is 3 bits in length. When the TAP controller enters the Shift-IR state, the instruction shift register is connected between JTDI and JTDO. While in the Shift-IR state, a rising edge on JTCLK with JTMS low shifts data one stage towards the serial output at JTDO. A rising edge on JTCLK in the Exit1-IR state or the Exit2-IR state with JTMS high moves the controller to the Update-IR state. The falling edge of that same JTCLK latches the data in the instruction shift register to the instruction parallel output. Instructions supported by the DS34T108 and their respective operational binary codes are shown in Table 11-1.

Table 11-1. JTAG Instruction Codes

INSTRUCTION	SELECTED REGISTER	INSTRUCTION CODES
SAMPLE/PRELOAD	Boundary Scan	010
BYPASS	Bypass	111
EXTEST	Boundary Scan	000
CLAMP	Bypass	011
HIGHZ	Bypass	100
IDCODE	Device Identification	001

Table 11-2. JTAG ID Code

DEVICE	ID CODE (hex)		
	Rev[31:28]	Device ID[27:12]	Manu[11:0]
DS34T108	0	0093	143
DS34T104	0	0092	143
DS34T102	0	0091	143
DS34T101	0	0090	143
DS34S108	0	009B	143
DS34S104	0	009A	143
DS34S102	0	0099	143
DS34S101	0	0098	143

11.3.1 SAMPLE/PRELOAD

SAMPLE/PRELOAD is a mandatory instruction for the IEEE 1149.1 specification. This instruction supports two functions. The digital I/Os of the device can be sampled at the boundary scan register without interfering with the normal operation of the device by using the Capture-DR state. SAMPLE/PRELOAD also allows the DS34T108 to shift data into the boundary scan register via JTDI using the Shift-DR state.

11.3.2 EXTEST

EXTEST allows testing of all interconnections to the device. When the EXTEST instruction is latched in the instruction register, the following actions occur. Once enabled via the Update-IR state, the parallel outputs of all digital output pins are driven. The boundary scan register is connected between JTDI and JTDO. The Capture-DR samples all digital inputs into the boundary scan register.

11.3.3 BYPASS

When the BYPASS instruction is latched into the parallel instruction register, JTDI connects to JTDO through the one-bit bypass test register. This allows data to pass from JTDI to JTDO not affecting the device's normal operation.

11.3.4 IDCODE

When the IDCODE instruction is latched into the parallel Instruction register, the Identification Test register is selected. The device identification code is loaded into the Identification register on the rising edge of JTCLK following entry into the Capture-DR state. Shift-DR can be used to shift the identification code out serially via JTDO. During Test-Logic-Reset, the identification code is forced into the instruction register's parallel output. The device ID code always has a one in the LSB position. The device ID codes are listed in Table 11-2.

11.3.5 HIGHZ

All digital outputs are placed into a high-impedance state. The bypass register is connected between JTDI and JTDO.

11.3.6 CLAMP

All digital outputs pins output data from the boundary scan parallel output while connecting the bypass register between JTDI and JTDO. The outputs do not change during the CLAMP instruction.

11.4 JTAG Test Registers

IEEE 1149.1 requires a minimum of two test registers: the bypass register and the boundary scan register. An optional test register has been included in the device design. This test register is the identification register and is used in conjunction with the IDCODE instruction and the Test-Logic-Reset state of the TAP controller.

11.4.1 Bypass Register

The bypass register is a single one-bit shift register used in conjunction with the BYPASS, CLAMP, and HIGHZ instructions, providing a short path between JTDI and JTDO.

11.4.2 Identification Register

The identification register contains a 32-bit shift register and a 32-bit latched parallel output. This register is selected during the IDCODE instruction and when the TAP controller is in the Test-Logic-Reset state.

11.4.3 Boundary Scan Register

The boundary scan register contains both a shift register path and a latched parallel output for all control cells and digital I/O cells, and is 32 bits in length. The BSDL file found at **www.maxim-ic.com/tools/bsdl** shows the entire cell bit locations and definitions.

12. DC Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Input, Bidirectional or Open Drain
Output Lead with Respect to DVSS……..-0.5V to +5.5V
Supply Voltage Range (VDDIO, DVDDLIU) with Respect to DVSS and DVSSLIU……...-0.5V to +3.6V
Supply Voltage Range (DVDDC) with Respect to DVSS……...-0.5V to +2.0V
Ambient Operating Temperature Range……..-40°C to +85°C
Junction Operating Temperature Range……-40°C to +125°C
Storage Temperature Range……...-55°C to +125°C
Soldering Temperature…….See IPC/JEDEC J-STD-020 specification.

These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect reliability. Ambient Operating Temperature Range is assuming the device is mounted on a JEDEC standard test board in a convection cooled JEDEC test enclosure.

Note: The typical values listed are not production tested.

Table 12-1. Recommended DC Operating Conditions

(T_j = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Logic 1	V_{IH}		2.4		3.465	V
Output Logic 0	V_{IL}		-0.3		+0.8	V
Supply ±5%	DVDDIO, DVDDLIU, ARVDDn, ATVDDn		3.135	3.300	3.465	V
Supply ±5%	DVDDC		1.71	1.8	1.89	V

Table 12-2. DC Electrical Characteristics

(T_j = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
3.3V Supply Current (DVDDIO, DVDDLIU = 3.465V; ARVDDn, ATVDDn = 3.465V) (Note 1)	I_{DDIO}	DS34T108		400	550	mA
		DS34T104		200	300	
		DS34T102		120	175	
		DS34T101		75	115	
1.8V Supply Current (DVDDC = 1.89V)	I_{DDC}	(Note 1)		300	350	mA
Lead Capacitance	C_{IO}			7		pF
Input Leakage	I_{IL}		-10		+10	µA
Input Leakage	I_{ILP}		-100		-10	µA
Output Leakage (when High Impedance)	I_{LO}		-10		+10	µA
Output Voltage (I_{OH} = -4.0mA)	V_{OH}	4mA output	2.4			V
Output Voltage (I_{OL} = +4.0mA)	V_{OL}	4mA output			0.4	V
Output Voltage (I_{OH} = -8.0mA)	V_{OH}	8mA output	2.4			V
Output Voltage (I_{OL} = -8.0mA)	V_{OL}	8mA output			0.4	V
Output Voltage (I_{OL} = +12.0mA)	V_{OL}	12mA output			0.4	V
Output Voltage (I_{OH} = -12.0mA)	V_{OH}	12mA output	2.4			V
Input Voltage Logic 0	V_{IL}				0.8	V
Input Voltage Logic 1	V_{IH}		2.0			V

Note 1: All outputs loaded with rated capacitance; all inputs between DVDDIO and DVSS; inputs with pull-ups connected to DVDDIO.

13. AC Timing Characteristics

Refer to the full data sheet for this information.

14. Pin Assignments

14.1 Board Design for the DS34T108 Family of Products

All devices in the DS34T108 family require the same footprint on the board. It is recommended that users design their board in such a way that it supports the stuffing of higher port-count devices into a lower port-count socket. If lower port-count designs are to be potentially stuffed with higher port-count devices, consideration must be taken during board design to bias the unused inputs, input/outputs, and outputs appropriately. Generally, unused inputs are tied directly to the ground plane, unused outputs are not connected, and unused input/outputs are tied to ground through a 10kΩ resistor. Unused inputs with internal pullups or pulldowns are not connected. Table 14-1 designates how each ball on the package should be connected to implement a common board design. Shading indicates balls for the unused inputs, input/outputs, and outputs of higher port-count devices.

When a user does stuff a socket with a higher port-count device, he/she needs a slightly modified BSDL file, available from the factory upon request.

The user may decide to not implement a common board design. In that event, the balls for the unused inputs, input/outputs, and outputs need not be connected, and the stuffing of higher port-count devices into a lower port-count socket is not recommended.

Table 14-1. Common Board Design Connections

BALL	DS34T108 SOCKET	DS34T104 SOCKET	DS34T102 SOCKET	DS34T101 SOCKET
M2	ACVDD1	ACVDD1	ACVDD1	ACVDD1
K2	ACVDD2	ACVDD2	ACVDD2	ACVDD2
M1	ACVSS1	ACVSS1	ACVSS1	ACVSS1
K1	ACVSS2	ACVSS2	ACVSS2	ACVSS2
B14	ARVDD1	ARVDD1	ARVDD1	ARVDD1
B10	ARVDD2	ARVDD2	ARVDD2	ARVDD2
B2	ARVDD3	ARVDD3	ARVDD3	ARVDD3
F2	ARVDD4	ARVDD4	ARVDD4	ARVDD4
U2	ARVDD5	ARVDD5	ARVDD5	ARVDD5
AA2	ARVDD6	ARVDD6	ARVDD6	ARVDD6
AA11	ARVDD7	ARVDD7	ARVDD7	ARVDD7
AA13	ARVDD8	ARVDD8	ARVDD8	ARVDD8
A14	ARVSS1	ARVSS1	ARVSS1	ARVSS1
A10	ARVSS2	ARVSS2	ARVSS2	ARVSS2
B1	ARVSS3	ARVSS3	ARVSS3	ARVSS3
F1	ARVSS4	ARVSS4	ARVSS4	ARVSS4
U1	ARVSS5	ARVSS5	ARVSS5	ARVSS5
AA1	ARVSS6	ARVSS6	ARVSS6	ARVSS6
AB11	ARVSS7	ARVSS7	ARVSS7	ARVSS7
AB13	ARVSS8	ARVSS8	ARVSS8	ARVSS8
B16	ATVDD1	ATVDD1	ATVDD1	ATVDD1
B8	ATVDD2	ATVDD2	ATVDD2	ATVDD2
D1	ATVDD3	ATVDD3	ATVDD3	ATVDD3
H2	ATVDD4	ATVDD4	ATVDD4	ATVDD4
R2	ATVDD5	ATVDD5	ATVDD5	ATVDD5
W1	ATVDD6	ATVDD6	ATVDD6	ATVDD6

BALL	DS34T108 SOCKET	DS34T104 SOCKET	DS34T102 SOCKET	DS34T101 SOCKET
AA9	ATVDD7	ATVDD7	ATVDD7	ATVDD7
AA15	ATVDD8	ATVDD8	ATVDD8	ATVDD8
A16	ATVSS1	ATVSS1	ATVSS1	ATVSS1
A8	ATVSS2	ATVSS2	ATVSS2	ATVSS2
D2	ATVSS3	ATVSS3	ATVSS3	ATVSS3
H1	ATVSS4	ATVSS4	ATVSS4	ATVSS4
R1	ATVSS5	ATVSS5	ATVSS5	ATVSS5
W2	ATVSS6	ATVSS6	ATVSS6	ATVSS6
AB9	ATVSS7	ATVSS7	ATVSS7	ATVSS7
AB15	ATVSS8	ATVSS8	ATVSS8	ATVSS8
P1	CLK_CMN	CLK_CMN	CLK_CMN	CLK_CMN
L1	CLK_HIGH	CLK_HIGH	CLK_HIGH	CLK_HIGH
V16	CLK_MII_RX	CLK_MII_RX	CLK_MII_RX	CLK_MII_RX
AA18	CLK_MII_TX	CLK_MII_TX	CLK_MII_TX	CLK_MII_TX
Y19	CLK_SSMII_TX	CLK_SSMII_TX	CLK_SSMII_TX	CLK_SSMII_TX
J1	CLK_SYS/SCCLK	CLK_SYS/SCCLK	CLK_SYS/SCCLK	CLK_SYS/SCCLK
J2	CLK_SYS_S	CLK_SYS_S	CLK_SYS_S	CLK_SYS_S
L21	DAT_32_16_N	DAT_32_16_N	DAT_32_16_N	DAT_32_16_N
L2	DVDDC	DVDDC	DVDDC	DVDDC
T5	DVDDC	DVDDC	DVDDC	DVDDC
V5	DVDDC	DVDDC	DVDDC	DVDDC
Y20	DVDDC	DVDDC	DVDDC	DVDDC
Y10	DVDDC	DVDDC	DVDDC	DVDDC
T18	DVDDC	DVDDC	DVDDC	DVDDC
G18	DVDDC	DVDDC	DVDDC	DVDDC
V18	DVDDC	DVDDC	DVDDC	DVDDC
V20	DVDDC	DVDDC	DVDDC	DVDDC
A12	DVDDC	DVDDC	DVDDC	DVDDC
E18	DVDDC	DVDDC	DVDDC	DVDDC
E20	DVDDC	DVDDC	DVDDC	DVDDC
C20	DVDDC	DVDDC	DVDDC	DVDDC
B11	DVDDC	DVDDC	DVDDC	DVDDC
G5	DVDDC	DVDDC	DVDDC	DVDDC
E5	DVDDC	DVDDC	DVDDC	DVDDC
C4	DVDDC	DVDDC	DVDDC	DVDDC
M9	DVDDIO	DVDDIO	DVDDIO	DVDDIO
N9	DVDDIO	DVDDIO	DVDDIO	DVDDIO
P10	DVDDIO	DVDDIO	DVDDIO	DVDDIO
P13	DVDDIO	DVDDIO	DVDDIO	DVDDIO
N14	DVDDIO	DVDDIO	DVDDIO	DVDDIO
P12	DVDDIO	DVDDIO	DVDDIO	DVDDIO
M14	DVDDIO	DVDDIO	DVDDIO	DVDDIO
L14	DVDDIO	DVDDIO	DVDDIO	DVDDIO
P11	DVDDIO	DVDDIO	DVDDIO	DVDDIO
K14	DVDDIO	DVDDIO	DVDDIO	DVDDIO
J12	DVDDIO	DVDDIO	DVDDIO	DVDDIO
J13	DVDDIO	DVDDIO	DVDDIO	DVDDIO

BALL	DS34T108 SOCKET	DS34T104 SOCKET	DS34T102 SOCKET	DS34T101 SOCKET
J11	DVDDIO	DVDDIO	DVDDIO	DVDDIO
J10	DVDDIO	DVDDIO	DVDDIO	DVDDIO
L9	DVDDIO	DVDDIO	DVDDIO	DVDDIO
K9	DVDDIO	DVDDIO	DVDDIO	DVDDIO
C3	DVDDLIU	DVDDLIU	DVDDLIU	DVDDLIU
V3	DVDDLIU	DVDDLIU	DVDDLIU	DVDDLIU
M10	DVSS	DVSS	DVSS	DVSS
L13	DVSS	DVSS	DVSS	DVSS
H15	DVSS	DVSS	DVSS	DVSS
U17	DVSS	DVSS	DVSS	DVSS
L11	DVSS	DVSS	DVSS	DVSS
M11	DVSS	DVSS	DVSS	DVSS
K12	DVSS	DVSS	DVSS	DVSS
K11	DVSS	DVSS	DVSS	DVSS
K10	DVSS	DVSS	DVSS	DVSS
M12	DVSS	DVSS	DVSS	DVSS
N11	DVSS	DVSS	DVSS	DVSS
D4	DVSS	DVSS	DVSS	DVSS
H8	DVSS	DVSS	DVSS	DVSS
K13	DVSS	DVSS	DVSS	DVSS
M13	DVSS	DVSS	DVSS	DVSS
B12	DVSS	DVSS	DVSS	DVSS
N2	DVSS	DVSS	DVSS	DVSS
F6	DVSS	DVSS	DVSS	DVSS
L10	DVSS	DVSS	DVSS	DVSS
U6	DVSS	DVSS	DVSS	DVSS
W4	DVSS	DVSS	DVSS	DVSS
R8	DVSS	DVSS	DVSS	DVSS
N12	DVSS	DVSS	DVSS	DVSS
F17	DVSS	DVSS	DVSS	DVSS
L12	DVSS	DVSS	DVSS	DVSS
N10	DVSS	DVSS	DVSS	DVSS
R15	DVSS	DVSS	DVSS	DVSS
W19	DVSS	DVSS	DVSS	DVSS
N13	DVSS	DVSS	DVSS	DVSS
Y12	DVSS	DVSS	DVSS	DVSS
D19	DVSS	DVSS	DVSS	DVSS
Y3	DVSSLIU	DVSSLIU	DVSSLIU	DVSSLIU
E3	DVSSLIU	DVSSLIU	DVSSLIU	DVSSLIU
L18	H_AD[1]	H_AD[1]	H_AD[1]	H_AD[1]
N22	H_AD[10]	H_AD[10]	H_AD[10]	H_AD[10]
L15	H_AD[11]	H_AD[11]	H_AD[11]	H_AD[11]
P21	H_AD[12]	H_AD[12]	H_AD[12]	H_AD[12]
N16	H_AD[13]	H_AD[13]	H_AD[13]	H_AD[13]
N20	H_AD[14]	H_AD[14]	H_AD[14]	H_AD[14]
P22	H_AD[15]	H_AD[15]	H_AD[15]	H_AD[15]
N19	H_AD[16]	H_AD[16]	H_AD[16]	H_AD[16]

BALL	DS34T108 SOCKET	DS34T104 SOCKET	DS34T102 SOCKET	DS34T101 SOCKET
R21	H_AD[17]	H_AD[17]	H_AD[17]	H_AD[17]
M19	H_AD[18]	H_AD[18]	H_AD[18]	H_AD[18]
N21	H_AD[19]	H_AD[19]	H_AD[19]	H_AD[19]
M21	H_AD[2]	H_AD[2]	H_AD[2]	H_AD[2]
M17	H_AD[20]	H_AD[20]	H_AD[20]	H_AD[20]
P20	H_AD[21]	H_AD[21]	H_AD[21]	H_AD[21]
R22	H_AD[22]	H_AD[22]	H_AD[22]	H_AD[22]
N17	H_AD[23]	H_AD[23]	H_AD[23]	H_AD[23]
T21	H_AD[24]	H_AD[24]	H_AD[24]	H_AD[24]
K16	H_AD[3]	H_AD[3]	H_AD[3]	H_AD[3]
M22	H_AD[4]	H_AD[4]	H_AD[4]	H_AD[4]
T20	H_AD[5]	H_AD[5]	H_AD[5]	H_AD[5]
M18	H_AD[6]	H_AD[6]	H_AD[6]	H_AD[6]
M16	H_AD[7]	H_AD[7]	H_AD[7]	H_AD[7]
M20	H_AD[8]	H_AD[8]	H_AD[8]	H_AD[8]
L16	H_AD[9]	H_AD[9]	H_AD[9]	H_AD[9]
K19	H_CPU_SPI_N	H_CPU_SPI_N	H_CPU_SPI_N	H_CPU_SPI_N
L17	H_CS_N	H_CS_N	H_CS_N	H_CS_N
T22	H_D[0]/SPI_MISO	H_D[0]/SPI_MISO	H_D[0]/SPI_MISO	H_D[0]/SPI_MISO
U21	H_D[1]	H_D[1]	H_D[1]	H_D[1]
V22	H_D[10]	H_D[10]	H_D[10]	H_D[10]
P18	H_D[11]	H_D[11]	H_D[11]	H_D[11]
W22	H_D[12]	H_D[12]	H_D[12]	H_D[12]
Y21	H_D[13]	H_D[13]	H_D[13]	H_D[13]
P19	H_D[14]	H_D[14]	H_D[14]	H_D[14]
Y22	H_D[15]	H_D[15]	H_D[15]	H_D[15]
AA21	H_D[16]	H_D[16]	H_D[16]	H_D[16]
AA22	H_D[17]	H_D[17]	H_D[17]	H_D[17]
AB21	H_D[18]	H_D[18]	H_D[18]	H_D[18]
U20	H_D[19]	H_D[19]	H_D[19]	H_D[19]
N18	H_D[2]	H_D[2]	H_D[2]	H_D[2]
R19	H_D[20]	H_D[20]	H_D[20]	H_D[20]
AB22	H_D[21]	H_D[21]	H_D[21]	H_D[21]
P17	H_D[22]	H_D[22]	H_D[22]	H_D[22]
V21	H_D[23]	H_D[23]	H_D[23]	H_D[23]
R17	H_D[24]	H_D[24]	H_D[24]	H_D[24]
V19	H_D[25]	H_D[25]	H_D[25]	H_D[25]
T19	H_D[26]	H_D[26]	H_D[26]	H_D[26]
W21	H_D[27]	H_D[27]	H_D[27]	H_D[27]
U16	H_D[28]	H_D[28]	H_D[28]	H_D[28]
R18	H_D[29]	H_D[29]	H_D[29]	H_D[29]
R20	H_D[3]	H_D[3]	H_D[3]	H_D[3]
W20	H_D[30]	H_D[30]	H_D[30]	H_D[30]
U19	H_D[31]	H_D[31]	H_D[31]	H_D[31]
T17	H_D[4]	H_D[4]	H_D[4]	H_D[4]
P16	H_D[5]	H_D[5]	H_D[5]	H_D[5]
U18	H_D[6]	H_D[6]	H_D[6]	H_D[6]

BALL	DS34T108 SOCKET	DS34T104 SOCKET	DS34T102 SOCKET	DS34T101 SOCKET
R16	H_D[7]	H_D[7]	H_D[7]	H_D[7]
U22	H_D[8]	H_D[8]	H_D[8]	H_D[8]
T16	H_D[9]	H_D[9]	H_D[9]	H_D[9]
J17	H_INT[0]	H_INT[0]	H_INT[0]	H_INT[0]
L22	H_INT[1]	H_INT[1]	H_INT[1]	H_INT[1]
K17	H_R_W_N/SPI_CP	H_R_W_N/SPI_CP	H_R_W_N/SPI_CP	H_R_W_N/SPI_CP
K18	H_READY_N	H_READY_N	H_READY_N	H_READY_N
L19	H_WR_BE0_N/SPI_CLK	H_WR_BE0_N/SPI_CLK	H_WR_BE0_N/SPI_CLK	H_WR_BE0_N/SPI_CLK
J16	H_WR_BE1_N/SPI_MOSI	H_WR_BE1_N/SPI_MOSI	H_WR_BE1_N/SPI_MOSI	H_WR_BE1_N/SPI_MOSI
J18	H_WR_BE2_N/SPI_SEL_N	H_WR_BE2_N/SPI_SEL_N	H_WR_BE2_N/SPI_SEL_N	H_WR_BE2_N/SPI_SEL_N
L20	H_WR_BE3_N/SPI_CI	H_WR_BE3_N/SPI_CI	H_WR_BE3_N/SPI_CI	H_WR_BE3_N/SPI_CI
T3	HiZ_N	HiZ_N	HiZ_N	HiZ_N
L3	JTCLK	JTCLK	JTCLK	JTCLK
M3	JTDI	JTDI	JTDI	JTDI
N3	JTDO	JTDO	JTDO	JTDO
K3	JTMS	JTMS	JTMS	JTMS
P3	JTRST_N	JTRST_N	JTRST_N	JTRST_N
M15	MBIST_DONE	MBIST_DONE	MBIST_DONE	MBIST_DONE
P15	MBIST_EN	MBIST_EN	MBIST_EN	MBIST_EN
N15	MBIST_FAIL	MBIST_FAIL	MBIST_FAIL	MBIST_FAIL
N1	MCLK	MCLK	MCLK	MCLK
AB17	MDC	MDC	MDC	MDC
AA20	MDIO	MDIO	MDIO	MDIO
AA17	MII_COL	MII_COL	MII_COL	MII_COL
Y18	MII_CRS	MII_CRS	MII_CRS	MII_CRS
Y17	MII_RX_DV	MII_RX_DV	MII_RX_DV	MII_RX_DV
V17	MII_RX_ERR	MII_RX_ERR	MII_RX_ERR	MII_RX_ERR
AA16	MII_RXD[0]	MII_RXD[0]	MII_RXD[0]	MII_RXD[0]
W16	MII_RXD[1]	MII_RXD[1]	MII_RXD[1]	MII_RXD[1]
AB16	MII_RXD[2]	MII_RXD[2]	MII_RXD[2]	MII_RXD[2]
Y16	MII_RXD[3]	MII_RXD[3]	MII_RXD[3]	MII_RXD[3]
W17	MII_TX_EN	MII_TX_EN	MII_TX_EN	MII_TX_EN
AB20	MII_TX_ERR	MII_TX_ERR	MII_TX_ERR	MII_TX_ERR
AB18	MII_TXD[0]	MII_TXD[0]	MII_TXD[0]	MII_TXD[0]
W18	MII_TXD[1]	MII_TXD[1]	MII_TXD[1]	MII_TXD[1]
AA19	MII_TXD[2]	MII_TXD[2]	MII_TXD[2]	MII_TXD[2]
AB19	MII_TXD[3]	MII_TXD[3]	MII_TXD[3]	MII_TXD[3]
C10	N.C.	N.C.	N.C.	N.C.
L4	RCLKF1/RCLK1	RCLKF1/RCLK1	RCLKF1/RCLK1	RCLKF1/RCLK1
C9	RCLKF2/RCLK2	RCLKF2/RCLK2	RCLKF2/RCLK2	10K to GND
K5	RCLKF3/RCLK3	RCLKF3/RCLK3	10K to GND	10K to GND
D7	RCLKF4/RCLK4	RCLKF4/RCLK4	10K to GND	10K to GND
P6	RCLKF5/RCLK5	10K to GND	10K to GND	10K to GND
Y6	RCLKF6/RCLK6	10K to GND	10K to GND	10K to GND
P5	RCLKF7/RCLK7	10K to GND	10K to GND	10K to GND
AB3	RCLKF8/RCLK8	10K to GND	10K to GND	10K to GND

BALL	DS34T108 SOCKET	DS34T104 SOCKET	DS34T102 SOCKET	DS34T101 SOCKET
A6	RDATF1	RDATF1	RDATF1	RDATF1
L7	RDATF2	RDATF2	RDATF2	GND
C5	RDATF3	RDATF3	GND	GND
F4	RDATF4	RDATF4	GND	GND
P4	RDATF5	GND	GND	GND
Y4	RDATF6	GND	GND	GND
AA5	RDATF7	GND	GND	GND
AA3	RDATF8	GND	GND	GND
A11	RESREF	RESREF	RESREF	RESREF
K8	RF/RMSYNC1	RF/RMSYNC1	RF/RMSYNC1	RF/RMSYNC1
E7	RF/RMSYNC2	RF/RMSYNC2	RF/RMSYNC2	N.C.
G4	RF/RMSYNC3	RF/RMSYNC3	N.C.	N.C.
E4	RF/RMSYNC4	RF/RMSYNC4	N.C.	N.C.
M6	RF/RMSYNC5	N.C.	N.C.	N.C.
W8	RF/RMSYNC6	N.C.	N.C.	N.C.
T4	RF/RMSYNC7	N.C.	N.C.	N.C.
AB5	RF/RMSYNC8	N.C.	N.C.	N.C.
M8	RLOF/RLOS1	RLOF/RLOS1	RLOF/RLOS1	RLOF/RLOS1
A4	RLOF/RLOS2	RLOF/RLOS2	RLOF/RLOS2	N.C.
H4	RLOF/RLOS3	RLOF/RLOS3	N.C.	N.C.
D5	RLOF/RLOS4	RLOF/RLOS4	N.C.	N.C.
U4	RLOF/RLOS5	N.C.	N.C.	N.C.
U3	RLOF/RLOS6	N.C.	N.C.	N.C.
N7	RLOF/RLOS7	N.C.	N.C.	N.C.
V7	RLOF/RLOS8	N.C.	N.C.	N.C.
B13	RRING1	RRING1	RRING1	RRING1
B9	RRING2	RRING2	RRING2	N.C.
A2	RRING3	RRING3	N.C.	N.C.
E2	RRING4	RRING4	N.C.	N.C.
V2	RRING5	N.C.	N.C.	N.C.
AB2	RRING6	N.C.	N.C.	N.C.
AA10	RRING7	N.C.	N.C.	N.C.
AA12	RRING8	N.C.	N.C.	N.C.
J5	RSER1	RSER1	RSER1	RSER1
D6	RSER2	RSER2	RSER2	N.C.
H7	RSER3	RSER3	N.C.	N.C.
D3	RSER4	RSER4	N.C.	N.C.
N6	RSER5	N.C.	N.C.	N.C.
W6	RSER6	N.C.	N.C.	N.C.
T8	RSER7	N.C.	N.C.	N.C.
AB4	RSER8	N.C.	N.C.	N.C.
P2	RST_SYS_N	RST_SYS_N	RST_SYS_N	RST_SYS_N
A5	RSYNC1	RSYNC1	RSYNC1	RSYNC1
L6	RSYNC2	RSYNC2	RSYNC2	10K to GND
A3	RSYNC3	RSYNC3	10K to GND	10K to GND

BALL	DS34T108 SOCKET	DS34T104 SOCKET	DS34T102 SOCKET	DS34T101 SOCKET
H6	RSYNC4	RSYNC4	10K to GND	10K to GND
W3	RSYNC5	10K to GND	10K to GND	10K to GND
R4	RSYNC6	10K to GND	10K to GND	10K to GND
AA6	RSYNC7	10K to GND	10K to GND	10K to GND
M5	RSYNC8	10K to GND	10K to GND	10K to GND
C6	RSYSCLK1	RSYSCLK1	RSYSCLK1	RSYSCLK1
K7	RSYSCLK2	RSYSCLK2	RSYSCLK2	GND
F8	RSYSCLK3	RSYSCLK3	GND	GND
H5	RSYSCLK4	RSYSCLK4	GND	GND
W5	RSYSCLK5	GND	GND	GND
U5	RSYSCLK6	GND	GND	GND
Y8	RSYSCLK7	GND	GND	GND
N8	RSYSCLK8	GND	GND	GND
A13	RTIP1	RTIP1	RTIP1	RTIP1
A9	RTIP2	RTIP2	RTIP2	N.C.
A1	RTIP3	RTIP3	N.C.	N.C.
E1	RTIP4	RTIP4	N.C.	N.C.
V1	RTIP5	N.C.	N.C.	N.C.
AB1	RTIP6	N.C.	N.C.	N.C.
AB10	RTIP7	N.C.	N.C.	N.C.
AB12	RTIP8	N.C.	N.C.	N.C.
R3	RXTSEL	RXTSEL	RXTSEL	RXTSEL
J15	SCEN	SCEN	SCEN	SCEN
A17	SD_A[0]	SD_A[0]	SD_A[0]	SD_A[0]
F18	SD_A[1]	SD_A[1]	SD_A[1]	SD_A[1]
B19	SD_A[10]	SD_A[10]	SD_A[10]	SD_A[10]
D17	SD_A[11]	SD_A[11]	SD_A[11]	SD_A[11]
F16	SD_A[2]	SD_A[2]	SD_A[2]	SD_A[2]
B18	SD_A[3]	SD_A[3]	SD_A[3]	SD_A[3]
E17	SD_A[4]	SD_A[4]	SD_A[4]	SD_A[4]
A19	SD_A[5]	SD_A[5]	SD_A[5]	SD_A[5]
H17	SD_A[6]	SD_A[6]	SD_A[6]	SD_A[6]
F19	SD_A[7]	SD_A[7]	SD_A[7]	SD_A[7]
F20	SD_A[8]	SD_A[8]	SD_A[8]	SD_A[8]
D18	SD_A[9]	SD_A[9]	SD_A[9]	SD_A[9]
G17	SD_BA[0]	SD_BA[0]	SD_BA[0]	SD_BA[0]
C19	SD_BA[1]	SD_BA[1]	SD_BA[1]	SD_BA[1]
E16	SD_CAS_N	SD_CAS_N	SD_CAS_N	SD_CAS_N
H16	SD_CLK	SD_CLK	SD_CLK	SD_CLK
B17	SD_CS_N	SD_CS_N	SD_CS_N	SD_CS_N
C18	SD_D[0]	SD_D[0]	SD_D[0]	SD_D[0]
F21	SD_D[1]	SD_D[1]	SD_D[1]	SD_D[1]
B22	SD_D[10]	SD_D[10]	SD_D[10]	SD_D[10]
H20	SD_D[11]	SD_D[11]	SD_D[11]	SD_D[11]
C21	SD_D[12]	SD_D[12]	SD_D[12]	SD_D[12]
H18	SD_D[13]	SD_D[13]	SD_D[13]	SD_D[13]

BALL	DS34T108 SOCKET	DS34T104 SOCKET	DS34T102 SOCKET	DS34T101 SOCKET
C22	SD_D[14]	SD_D[14]	SD_D[14]	SD_D[14]
D21	SD_D[15]	SD_D[15]	SD_D[15]	SD_D[15]
G20	SD_D[16]	SD_D[16]	SD_D[16]	SD_D[16]
D22	SD_D[17]	SD_D[17]	SD_D[17]	SD_D[17]
J20	SD_D[18]	SD_D[18]	SD_D[18]	SD_D[18]
G21	SD_D[19]	SD_D[19]	SD_D[19]	SD_D[19]
G19	SD_D[2]	SD_D[2]	SD_D[2]	SD_D[2]
J21	SD_D[20]	SD_D[20]	SD_D[20]	SD_D[20]
E22	SD_D[21]	SD_D[21]	SD_D[21]	SD_D[21]
J19	SD_D[22]	SD_D[22]	SD_D[22]	SD_D[22]
H21	SD_D[23]	SD_D[23]	SD_D[23]	SD_D[23]
F22	SD_D[24]	SD_D[24]	SD_D[24]	SD_D[24]
K21	SD_D[25]	SD_D[25]	SD_D[25]	SD_D[25]
G22	SD_D[26]	SD_D[26]	SD_D[26]	SD_D[26]
K20	SD_D[27]	SD_D[27]	SD_D[27]	SD_D[27]
H22	SD_D[28]	SD_D[28]	SD_D[28]	SD_D[28]
G16	SD_D[29]	SD_D[29]	SD_D[29]	SD_D[29]
A21	SD_D[3]	SD_D[3]	SD_D[3]	SD_D[3]
K22	SD_D[30]	SD_D[30]	SD_D[30]	SD_D[30]
J22	SD_D[31]	SD_D[31]	SD_D[31]	SD_D[31]
C16	SD_D[4]	SD_D[4]	SD_D[4]	SD_D[4]
A22	SD_D[5]	SD_D[5]	SD_D[5]	SD_D[5]
A18	SD_D[6]	SD_D[6]	SD_D[6]	SD_D[6]
B21	SD_D[7]	SD_D[7]	SD_D[7]	SD_D[7]
E21	SD_D[8]	SD_D[8]	SD_D[8]	SD_D[8]
H19	SD_D[9]	SD_D[9]	SD_D[9]	SD_D[9]
A20	SD_DQM[0]	SD_DQM[0]	SD_DQM[0]	SD_DQM[0]
E19	SD_DQM[1]	SD_DQM[1]	SD_DQM[1]	SD_DQM[1]
B20	SD_DQM[2]	SD_DQM[2]	SD_DQM[2]	SD_DQM[2]
D20	SD_DQM[3]	SD_DQM[3]	SD_DQM[3]	SD_DQM[3]
D16	SD_RAS_N	SD_RAS_N	SD_RAS_N	SD_RAS_N
C17	SD_WE_N	SD_WE_N	SD_WE_N	SD_WE_N
K15	STMD	STMD	STMD	STMD
B6	TCLKF1	TCLKF1	TCLKF1	TCLKF1
K4	TCLKF2	TCLKF2	TCLKF2	GND
D8	TCLKF3	TCLKF3	GND	GND
J6	TCLKF4	TCLKF4	GND	GND
T6	TCLKF5	GND	GND	GND
T7	TCLKF6	GND	GND	GND
U8	TCLKF7	GND	GND	GND
M4	TCLKF8	GND	GND	GND
L8	TCLKO1	TCLKO1	TCLKO1	TCLKO1
B5	TCLKO2	TCLKO2	TCLKO2	N.C.
J7	TCLKO3	TCLKO3	N.C.	N.C.
E6	TCLKO4	TCLKO4	N.C.	N.C.
N4	TCLKO5	N.C.	N.C.	N.C.

BALL	DS34T108 SOCKET	DS34T104 SOCKET	DS34T102 SOCKET	DS34T101 SOCKET
U7	TCLKO6	N.C.	N.C.	N.C.
P7	TCLKO7	N.C.	N.C.	N.C.
AA7	TCLKO8	N.C.	N.C.	N.C.
C7	TDATF1	TDATF1	TDATF1	TDATF1
J8	TDATF2	TDATF2	TDATF2	N.C.
B4	TDATF3	TDATF3	N.C.	N.C.
K6	TDATF4	TDATF4	N.C.	N.C.
R6	TDATF5	N.C.	N.C.	N.C.
N5	TDATF6	N.C.	N.C.	N.C.
Y7	TDATF7	N.C.	N.C.	N.C.
P8	TDATF8	N.C.	N.C.	N.C.
E10	TDM1_ACLK	TDM1_ACLK	TDM1_ACLK	TDM1_ACLK
D12	TDM1_RCLK	TDM1_RCLK	TDM1_RCLK	TDM1_RCLK
C11	TDM1_RSIG_RTS	TDM1_RSIG_RTS	TDM1_RSIG_RTS	TDM1_RSIG_RTS
D10	TDM1_RX	TDM1_RX	TDM1_RX	TDM1_RX
D11	TDM1_RX_SYNC	TDM1_RX_SYNC	TDM1_RX_SYNC	TDM1_RX_SYNC
F12	TDM1_TCLK	TDM1_TCLK	TDM1_TCLK	TDM1_TCLK
E11	TDM1_TSIG_CTS	TDM1_TSIG_CTS	TDM1_TSIG_CTS	TDM1_TSIG_CTS
C12	TDM1_TX	TDM1_TX	TDM1_TX	TDM1_TX
F13	TDM1_TX_MF_CD	TDM1_TX_MF_CD	TDM1_TX_MF_CD	TDM1_TX_MF_CD
E13	TDM1_TX_SYNC	TDM1_TX_SYNC	TDM1_TX_SYNC	TDM1_TX_SYNC
E9	TDM2_ACLK	TDM2_ACLK	TDM2_ACLK	N.C.
E12	TDM2_RCLK	TDM2_RCLK	TDM2_RCLK	N.C.
C14	TDM2_RSIG_RTS	TDM2_RSIG_RTS	TDM2_RSIG_RTS	N.C.
D13	TDM2_RX	TDM2_RX	TDM2_RX	N.C.
C13	TDM2_RX_SYNC	TDM2_RX_SYNC	TDM2_RX_SYNC	N.C.
G10	TDM2_TCLK	TDM2_TCLK	TDM2_TCLK	N.C.
F11	TDM2_TSIG_CTS	TDM2_TSIG_CTS	TDM2_TSIG_CTS	N.C.
G11	TDM2_TX	TDM2_TX	TDM2_TX	N.C.
F10	TDM2_TX_MF_CD	TDM2_TX_MF_CD	TDM2_TX_MF_CD	N.C.
E14	TDM2_TX_SYNC	TDM2_TX_SYNC	TDM2_TX_SYNC	N.C.
G14	TDM3_ACLK	TDM3_ACLK	N.C.	N.C.
C15	TDM3_RCLK	TDM3_RCLK	N.C.	N.C.
G13	TDM3_RSIG_RTS	TDM3_RSIG_RTS	N.C.	N.C.
D15	TDM3_RX	TDM3_RX	N.C.	N.C.
D14	TDM3_RX_SYNC	TDM3_RX_SYNC	N.C.	N.C.
G9	TDM3_TCLK	TDM3_TCLK	N.C.	N.C.
G12	TDM3_TSIG_CTS	TDM3_TSIG_CTS	N.C.	N.C.
E15	TDM3_TX	TDM3_TX	N.C.	N.C.
F9	TDM3_TX_MF_CD	TDM3_TX_MF_CD	N.C.	N.C.
F14	TDM3_TX_SYNC	TDM3_TX_SYNC	N.C.	N.C.
H12	TDM4_ACLK	TDM4_ACLK	N.C.	N.C.
J14	TDM4_RCLK	TDM4_RCLK	N.C.	N.C.
F15	TDM4_RSIG_RTS	TDM4_RSIG_RTS	N.C.	N.C.
H9	TDM4_RX	TDM4_RX	N.C.	N.C.

BALL	DS34T108 SOCKET	DS34T104 SOCKET	DS34T102 SOCKET	DS34T101 SOCKET
H14	TDM4_RX_SYNC	TDM4_RX_SYNC	N.C.	N.C.
H11	TDM4_TCLK	TDM4_TCLK	N.C.	N.C.
G15	TDM4_TSIG_CTS	TDM4_TSIG_CTS	N.C.	N.C.
J9	TDM4_TX	TDM4_TX	N.C.	N.C.
H13	TDM4_TX_MF_CD	TDM4_TX_MF_CD	N.C.	N.C.
H10	TDM4_TX_SYNC	TDM4_TX_SYNC	N.C.	N.C.
V11	TDM5_ACLK	N.C.	N.C.	N.C.
V9	TDM5_RCLK	N.C.	N.C.	N.C.
T9	TDM5_RSIG_RTS	N.C.	N.C.	N.C.
R11	TDM5_RX	N.C.	N.C.	N.C.
U14	TDM5_RX_SYNC	N.C.	N.C.	N.C.
T13	TDM5_TCLK	N.C.	N.C.	N.C.
P14	TDM5_TSIG_CTS	N.C.	N.C.	N.C.
R12	TDM5_TX	N.C.	N.C.	N.C.
R10	TDM5_TX_MF_CD	N.C.	N.C.	N.C.
R14	TDM5_TX_SYNC	N.C.	N.C.	N.C.
W14	TDM6_ACLK	N.C.	N.C.	N.C.
T12	TDM6_RCLK	N.C.	N.C.	N.C.
R9	TDM6_RSIG_RTS	N.C.	N.C.	N.C.
V12	TDM6_RX	N.C.	N.C.	N.C.
T15	TDM6_RX_SYNC	N.C.	N.C.	N.C.
V15	TDM6_TCLK	N.C.	N.C.	N.C.
V13	TDM6_TSIG_CTS	N.C.	N.C.	N.C.
W15	TDM6_TX	N.C.	N.C.	N.C.
U15	TDM6_TX_MF_CD	N.C.	N.C.	N.C.
T10	TDM6_TX_SYNC	N.C.	N.C.	N.C.
V14	TDM7_ACLK	N.C.	N.C.	N.C.
U13	TDM7_RCLK	N.C.	N.C.	N.C.
T14	TDM7_RSIG_RTS	N.C.	N.C.	N.C.
U12	TDM7_RX	N.C.	N.C.	N.C.
R13	TDM7_RX_SYNC	N.C.	N.C.	N.C.
Y11	TDM7_TCLK	N.C.	N.C.	N.C.
W9	TDM7_TSIG_CTS	N.C.	N.C.	N.C.
W12	TDM7_TX	N.C.	N.C.	N.C.
Y15	TDM7_TX_MF_CD	N.C.	N.C.	N.C.
U11	TDM7_TX_SYNC	N.C.	N.C.	N.C.
Y13	TDM8_ACLK	N.C.	N.C.	N.C.
U9	TDM8_RCLK	N.C.	N.C.	N.C.
Y9	TDM8_RSIG_RTS	N.C.	N.C.	N.C.
V10	TDM8_RX	N.C.	N.C.	N.C.
T11	TDM8_RX_SYNC	N.C.	N.C.	N.C.
Y14	TDM8_TCLK	N.C.	N.C.	N.C.
W11	TDM8_TSIG_CTS	N.C.	N.C.	N.C.
W10	TDM8_TX	N.C.	N.C.	N.C.
W13	TDM8_TX_MF_CD	N.C.	N.C.	N.C.

BALL	DS34T108 SOCKET	DS34T104 SOCKET	DS34T102 SOCKET	DS34T101 SOCKET
U10	TDM8_TX_SYNC	N.C.	N.C.	N.C.
J3	TEST_CLK	TEST_CLK	TEST_CLK	TEST_CLK
B15	TRING1	TRING1	TRING1	TRING1
B7	TRING2	TRING2	TRING2	N.C.
C2	TRING3	TRING3	N.C.	N.C.
G2	TRING4	TRING4	N.C.	N.C.
T2	TRING5	N.C.	N.C.	N.C.
Y2	TRING6	N.C.	N.C.	N.C.
AA8	TRING7	N.C.	N.C.	N.C.
AA14	TRING8	N.C.	N.C.	N.C.
D9	TSER1	TSER1	TSER1	TSER1
J4	TSER2	TSER2	TSER2	GND
B3	TSER3	TSER3	GND	GND
F3	TSER4	TSER4	GND	GND
V6	TSER5	GND	GND	GND
R7	TSER6	GND	GND	GND
V8	TSER7	GND	GND	GND
P9	TSER8	GND	GND	GND
G3	TST_CLD	TST_CLD	TST_CLD	TST_CLD
L5	TSYNC/TSSYNC1	TSYNC/TSSYNC1	TSYNC/TSSYNC1	TSYNC/TSSYNC1
E8	TSYNC/TSSYNC2	TSYNC/TSSYNC2	TSYNC/TSSYNC2	10K to GND
G7	TSYNC/TSSYNC3	TSYNC/TSSYNC3	10K to GND	10K to GND
F5	TSYNC/TSSYNC4	TSYNC/TSSYNC4	10K to GND	10K to GND
M7	TSYNC/TSSYNC5	10K to GND	10K to GND	10K to GND
Y5	TSYNC/TSSYNC6	10K to GND	10K to GND	10K to GND
R5	TSYNC/TSSYNC7	10K to GND	10K to GND	10K to GND
AB6	TSYNC/TSSYNC8	10K to GND	10K to GND	10K to GND
C8	TSYSCLK1/ECLK1	TSYSCLK1/ECLK1	TSYSCLK1/ECLK1	TSYSCLK1/ECLK1
G8	TSYSCLK2/ECLK2	TSYSCLK2/ECLK2	TSYSCLK2/ECLK2	GND
F7	TSYSCLK3/ECLK3	TSYSCLK3/ECLK3	GND	GND
G6	TSYSCLK4/ECLK4	TSYSCLK4/ECLK4	GND	GND
V4	TSYSCLK5/ECLK5	GND	GND	GND
AA4	TSYSCLK6/ECLK6	GND	GND	GND
W7	TSYSCLK7/ECLK7	GND	GND	GND
AB7	TSYSCLK8/ECLK8	GND	GND	GND
A15	TTIP1	TTIP1	TTIP1	TTIP1
A7	TTIP2	TTIP2	TTIP2	N.C.
C1	TTIP3	TTIP3	N.C.	N.C.
G1	TTIP4	TTIP4	N.C.	N.C.
T1	TTIP5	N.C.	N.C.	N.C.
Y1	TTIP6	N.C.	N.C.	N.C.
AB8	TTIP7	N.C.	N.C.	N.C.
AB14	TTIP8	N.C.	N.C.	N.C.
H3	TXENABLE	TXENABLE	TXENABLE	TXENABLE

14.2 DS34T108 Pin Assignment

Figure 14-1. DS34T108 Pin Assignment (HSBGA Package)

	1	2	3	4	5	6	7	8	9	10	11
A	RTIP3	RRING3	RSYNC3	RLOF/RLOS2	RSYNC1	RDATF1	TTIP2	ATVSS2	RTIP2	ARVSS2	RESREF
B	ARVSS3	ARVDD3	TSER3	TDATF3	TCLKO2	TCLKF1	TRING2	ATVDD2	RRING2	ARVDD2	DVDDC
C	TTIP3	TRING3	DVDDLIU	DVDDC	RDATF3	RSYSCLK1	TDATF1	TSYSCLK1/ECLK1	RCLKF2/RCLK2	NC	TDM1_RSIG_RTS
D	ATVDD3	ATVSS3	RSER4	DVSS	RLOF/RLOS4	RSER2	RCLKF4/RCLK4	TCLKF3	TSER1	TDM1_RX	TDM1_RX_SYNC
E	RTIP4	RRING4	DVSSLIU	RF/RMSYNC4	DVDDC	TCLKO4	RF/RMSYNC2	TSYNC/TSSYNC2	TDM2_ACLK	TDM1_ACLK	TDM1_TSIG_CTS
F	ARVSS4	ARVDD4	TSER4	RDATF4	TSYNC/TSSYNC4	DVSS	TSYSCLK3/ECLK3	RSYSCLK3	TDM3_TX_MF_CD	TDM2_TX_MF_CD	TDM2_TSIG_CTS
G	TTIP4	TRING4	TST_CLD	RF/RMSYNC3	DVDDC	TSYSCLK4/ECLK4	TSYNC/TSSYNC3	TSYSCLK2/ECLK2	TDM3_TCLK	TDM2_TCLK	TDM2_TX
H	ATVSS4	ATVDD4	TXENABLE	RLOF/RLOS3	RSYSCLK4	RSYNC4	RSER3	DVSS	TDM4_RX	TDM4_TX_SYNC	TDM4_TCLK
J	CLK_SYS/SCCLK	CLK_SYS_S	TEST_CLK	TSER2	RSER1	TCLKF4	TCLKO3	TDATF2	TDM4_TX	DVDDIO	DVDDIO
K	ACVSS2	ACVDD2	JTMS	TCLKF2	RCLKF3/RCLK3	TDATF4	RSYSCLK2	RF/RMSYNC1	DVDDIO	DVSS	DVSS
L	CLK_HIGH	DVDDC	JTCLK	RCLKF1/RCLK1	TSYNC/TSSYNC1	RSYNC2	RDATF2	TCLKO1	DVDDIO	DVSS	DVSS
M	ACVSS1	ACVDD1	JTDI	TCLKF8	RSYNC8	RF/RMSYNC5	TSYNC/TSSYNC5	RLOF/RLOS1	DVDDIO	DVSS	DVSS
N	MCLK	DVSS	JTDO	TCLKO5	TDATF6	RSER5	RLOF/RLOS7	RSYSCLK8	DVDDIO	DVSS	DVSS
P	CLK_CMN	RST_SYS_N	JTRST_N	RDATF5	RCLKF7/RCLK7	RCLKF5/RCLK5	TCLKO7	TDATF8	TSER8	DVDDIO	DVDDIO
R	ATVSS5	ATVDD5	RXTSEL	RSYNC6	TSYNC/TSSYNC7	TDATF5	TSER6	DVSS	TDM6_RSIG_RTS	TDM5_TX_MF_CD	TDM5_RX
T	TTIP5	TRING5	HIZ_N	RF/RMSYNC7	DVDDC	TCLKF5	TCLKF6	RSER7	TDM5_RSIG_RTS	TDM6_TX_SYNC	TDM8_RX_SYNC
U	ARVSS5	ARVDD5	RLOF/RLOS6	RLOF/RLOS5	RSYSCLK6	DVSS	TCLKO6	TCLKF7	TDM8_RCLK	TDM8_TX_SYNC	TDM7_TX_SYNC
V	RTIP5	RRING5	DVDDLIU	TSYSCLK5/ECLK5	DVDDC	TSER5	RLOF/RLOS8	TSER7	TDM5_RCLK	TDM8_RX	TDM5_ACLK
W	ATVDD6	ATVSS6	RSYNC5	DVSS	RSYSCLK5	RSER6	TSYSCLK7/ECLK7	RF/RMSYNC6	TDM7_TSIG_CTS	TDM8_TX	TDM8_TSIG_CTS
Y	TTIP6	TRING6	DVSSLIU	RDATF6	TSYNC/TSSYNC6	RCLKF6/RCLK6	TDATF7	RSYSCLK7	TDM8_RSIG_RTS	DVDDC	TDM7_TCLK
AA	ARVSS6	ARVDD6	RDATF8	TSYSCLK6/ECLK6	RDATF7	RSYNC7	TCLKO8	TRING7	ATVDD7	RRING7	ARVDD7
AB	RTIP6	RRING6	RCLKF8/RCLK8	RSER8	RF/RMSYNC8	TSYNC/TSSYNC8	TSYSCLK8/ECLK8	TTIP7	ATVSS7	RTIP7	ARVSS7
	1	2	3	4	5	6	7	8	9	10	11

12	13	14	15	16	17	18	19	20	21	22	
DVDDC	RTIP1	ARVSS1	TTIP1	ATVSS1	SD_A[0]	SD_D[6]	SD_A[5]	SD_DQM[0]	SD_D[3]	SD_D[5]	A
DVSS	RRING1	ARVDD1	TRING1	ATVDD1	SD_CS_N	SD_A[3]	SD_A[10]	SD_DQM[2]	SD_D[7]	SD_D[10]	B
TDM1_TX	TDM2_RX_SYNC	TDM2_RSIG_RTS	TDM3_RCLK	SD_D[4]	SD_WE_N	SD_D[0]	SD_BA[1]	DVDDC	SD_D[12]	SD_D[14]	C
TDM1_RCLK	TDM2_RX	TDM3_RX_SYNC	TDM3_RX	SD_RAS_N	SD_A[11]	SD_A[9]	DVSS	SD_DQM[3]	SD_D[15]	SD_D[17]	D
TDM2_RCLK	TDM1_TX_SYNC	TDM2_TX_SYNC	TDM3_TX	SD_CAS_N	SD_A[4]	DVDDC	SD_DQM[1]	DVDDC	SD_D[8]	SD_D[21]	E
TDM1_TCLK	TDM1_TX_MF_CD	TDM3_TX_SYNC	TDM4_RSIG_RTS	SD_A[2]	DVSS	SD_A[1]	SD_A[7]	SD_A[8]	SD_D[1]	SD_D[24]	F
TDM3_TSIG_CTS	TDM3_RSIG_RTS	TDM3_ACLK	TDM4_TSIG_CTS	SD_D[29]	SD_BA[0]	DVDDC	SD_D[2]	SD_D[16]	SD_D[19]	SD_D[26]	G
TDM4_ACLK	TDM4_TX_MF_CD	TDM4_RX_SYNC	DVSS	SD_CLK	SD_A[6]	SD_D[13]	SD_D[9]	SD_D[11]	SD_D[23]	SD_D[28]	H
DVDDIO	DVDDIO	TDM4_RCLK	SCEN	H_WR_BE1_N/SPI_MOSI	H_INT[0]	H_WR_BE2_N/SPI_SEL_N	SD_D[22]	SD_D[18]	SD_D[20]	SD_D[31]	J
DVSS	DVSS	DVDDIO	STMD	H_AD[3]	H_R_W_N/SPI_CP	H_READY_N	H_CPU_SPI_N	SD_D[27]	SD_D[25]	SD_D[30]	K
DVSS	DVSS	DVDDIO	H_AD[11]	H_AD[9]	H_CS_N	H_AD[1]	H_WR_BE0_N/SPI_CLK	H_WR_BE3_N/SPI_CI	DAT_32_16_N	H_INT[1]	L
DVSS	DVSS	DVDDIO	MBIST_DONE	H_AD[7]	H_AD[20]	H_AD[6]	H_AD[18]	H_AD[8]	H_AD[2]	H_AD[4]	M
DVSS	DVSS	DVDDIO	MBIST_FAIL	H_AD[13]	H_AD[23]	H_D[2]	H_AD[16]	H_AD[14]	H_AD[19]	H_AD[10]	N
DVDDIO	DVDDIO	TDM5_TSIG_CTS	MBIST_EN	H_D[5]	H_D[22]	H_D[11]	H_D[14]	H_AD[21]	H_AD[12]	H_AD[15]	P
TDM5_TX	TDM7_RX_SYNC	TDM5_TX_SYNC	DVSS	H_D[7]	H_D[24]	H_D[29]	H_D[20]	H_D[3]	H_AD[17]	H_AD[22]	R
TDM6_RCLK	TDM5_TCLK	TDM7_RSIG_RTS	TDM6_RX_SYNC	H_D[9]	H_D[4]	DVDDC	H_D[26]	H_AD[5]	H_AD[24]	H_D[0]/SPI_MISO	T
TDM7_RX	TDM7_RCLK	TDM5_RX_SYNC	TDM6_TX_MF_CD	H_D[28]	DVSS	H_D[6]	H_D[31]	H_D[19]	H_D[1]	H_D[8]	U
TDM6_RX	TDM6_TSIG_CTS	TDM7_ACLK	TDM6_TCLK	CLK_MII_RX	MII_RX_ERR	DVDDC	H_D[25]	DVDDC	H_D[23]	H_D[10]	V
TDM7_TX	TDM8_TX_MF_CD	TDM6_ACLK	TDM6_TX	MII_RXD[1]	MII_TX_EN	MII_TXD[1]	DVSS	H_D[30]	H_D[27]	H_D[12]	W
DVSS	TDM8_ACLK	TDM8_TCLK	TDM7_TX_MF_CD	MII_RXD[3]	MII_RX_DV	MII_CRS	CLK_SSMII_TX	DVDDC	H_D[13]	H_D[15]	Y
RRING8	ARVDD8	TRING8	ATVDD8	MII_RXD[0]	MII_COL	CLK_MII_TX	MII_TXD[2]	MDIO	H_D[16]	H_D[17]	AA
RTIP8	ARVSS8	TTIP8	ATVSS8	MII_RXD[2]	MDC	MII_TXD[0]	MII_TXD[3]	MII_TX_ERR	H_D[18]	H_D[21]	AB
12	13	14	15	16	17	18	19	20	21	22	

14.3 DS34T104 Pin Assignment

Figure 14-2. DS34T104 Pin Assignment (TEBGA Package)

	1	2	3	4	5	6	7	8	9	10	11
A	RTIP3	RRING3	RSYNC3	RLOF/RLOS2	RSYNC1	RDATF1	TTIP2	ATVSS2	RTIP2	ARVSS2	RESREF
B	ARVSS3	ARVDD3	TSER3	TDATF3	TCLKO2	TCLKF1	TRING2	ATVDD2	RRING2	ARVDD2	DVDDC
C	TTIP3	TRING3	DVDDLIU	DVDDC	RDATF3	RSYSCLK1	TDATF1	TSYSCLK1/ECLK1	RCLKF2/RCLK2	NC	TDM1_RSIG_RTS
D	ATVDD3	ATVSS3	RSER4	DVSS	RLOF/RLOS4	RSER2	RCLKF4/RCLK4	TCLKF3	TSER1	TDM1_RX	TDM1_RX_SYNC
E	RTIP4	RRING4	DVSSLIU	RF/RMSYNC4	DVDDC	TCLKO4	RF/RMSYNC2	TSYNC/TSSYNC2	TDM2_ACLK	TDM1_ACLK	TDM1_TSIG_CTS
F	ARVSS4	ARVDD4	TSER4	RDATF4	TSYNC/TSSYNC4	DVSS	TSYSCLK3/ECLK3	RSYSCLK3	TDM3_TX_MF_CD	TDM2_TX_MF_CD	TDM2_TSIG_CTS
G	TTIP4	TRING4	TST_CLD	RF/RMSYNC3	DVDDC	TSYSCLK4/ECLK4	TSYNC/TSSYNC3	TSYSCLK2/ECLK2	TDM3_TCLK	TDM2_TCLK	TDM2_TX
H	ATVSS4	ATVDD4	TXENABLE	RLOF/RLOS3	RSYSCLK4	RSYNC4	RSER3	DVSS	TDM4_RX	TDM4_TX_SYNC	TDM4_TCLK
J	CLK_SYS/SCCLK	CLK_SYS_S	TEST_CLK	TSER2	RSER1	TCLKF4	TCLKO3	TDATF2	TDM4_TX	DVDDIO	DVDDIO
K	ACVSS2	ACVDD2	JTMS	TCLKF2	RCLKF3/RCLK3	TDATF4	RSYSCLK2	RF/RMSYNC1	DVDDIO	DVSS	DVSS
L	CLK_HIGH	DVDDC	JTCLK	RCLKF1/RCLK1	TSYNC/TSSYNC1	RSYNC2	RDATF2	TCLKO1	DVDDIO	DVSS	DVSS
M	ACVSS1	ACVDD1	JTDI	NC	NC	TST_RB	TST_TC	RLOF/RLOS1	DVDDIO	DVSS	DVSS
N	MCLK	DVSS	JTDO	NC	TST_TA	TST_RA	NC	NC	DVDDIO	DVSS	DVSS
P	CLK_CMN	RST_SYS_N	JTRST_N	TST_TB	NC	NC	NC	NC	NC	DVDDIO	DVDDIO
R	ATVSS5	ATVDD5	RXTSEL	NC	NC	TST_RC	NC	DVSS	NC	NC	NC
T	NC	NC	HiZ_N	NC	DVDDC	NC	NC	NC	NC	NC	NC
U	ARVSS5	ARVDD5	NC	NC	NC	DVSS	NC	NC	NC	NC	NC
V	NC	NC	DVDDLIU	NC	DVDDC	NC	NC	NC	NC	NC	NC
W	ATVDD6	ATVSS6	NC	DVSS	NC	NC	NC	NC	NC	NC	NC
Y	NC	NC	DVSSLIU	NC	NC	NC	NC	NC	NC	DVDDC	NC
AA	ARVSS6	ARVDD6	NC	NC	NC	NC	NC	NC	ATVDD7	NC	ARVDD7
AB	NC	NC	NC	NC	NC	NC	NC	NC	ATVSS7	NC	ARVSS7
	1	2	3	4	5	6	7	8	9	10	11

12	13	14	15	16	17	18	19	20	21	22	
DVDDC	RTIP1	ARVSS1	TTIP1	ATVSS1	SD_A[0]	SD_D[6]	SD_A[5]	SD_DQM[0]	SD_D[3]	SD_D[5]	A
DVSS	RRING1	ARVDD1	TRING1	ATVDD1	SD_CS_N	SD_A[3]	SD_A[10]	SD_DQM[2]	SD_D[7]	SD_D[10]	B
TDM1_TX	TDM2_RX_SYNC	TDM2_RSIG_RTS	TDM3_RCLK	SD_D[4]	SD_WE_N	SD_D[0]	SD_BA[1]	DVDDC	SD_D[12]	SD_D[14]	C
TDM1_RCLK	TDM2_RX	TDM3_RX_SYNC	TDM3_RX	SD_RAS_N	SD_A[11]	SD_A[9]	DVSS	SD_DQM[3]	SD_D[15]	SD_D[17]	D
TDM2_RCLK	TDM1_TX_SYNC	TDM2_TX_SYNC	TDM3_TX	SD_CAS_N	SD_A[4]	DVDDC	SD_DQM[1]	DVDDC	SD_D[8]	SD_D[21]	E
TDM1_TCLK	TDM1_TX_MF_CD	TDM3_TX_SYNC	TDM4_RSIG_RTS	SD_A[2]	DVSS	SD_A[1]	SD_A[7]	SD_A[8]	SD_D[1]	SD_D[24]	F
TDM3_TSIG_CTS	TDM3_RSIG_RTS	TDM3_ACLK	TDM4_TSIG_CTS	SD_D[29]	SD_BA[0]	DVDDC	SD_D[2]	SD_D[16]	SD_D[19]	SD_D[26]	G
TDM4_ACLK	TDM4_TX_MF_CD	TDM4_RX_SYNC	DVSS	SD_CLK	SD_A[6]	SD_D[13]	SD_D[9]	SD_D[11]	SD_D[23]	SD_D[28]	H
DVDDIO	DVDDIO	TDM4_RCLK	SCEN	H_WR_BE1_N/SPI_MOSI	H_INT[0]	H_WR_BE2_N/SPI_SEL_N	SD_D[22]	SD_D[18]	SD_D[20]	SD_D[31]	J
DVSS	DVSS	DVDDIO	STMD	H_AD[3]	H_R_W_N/SPI_CP	H_READY_N	H_CPU_SPI_N	SD_D[27]	SD_D[25]	SD_D[30]	K
DVSS	DVSS	DVDDIO	H_AD[11]	H_AD[9]	H_CS_N	H_AD[1]	H_WR_BE0_N/SPI_CLK	H_WR_BE3_N/SPI_CI	DAT_32_16_N	H_INT[1]	L
DVSS	DVSS	DVDDIO	MBIST_DONE	H_AD[7]	H_AD[20]	H_AD[6]	H_AD[18]	H_AD[8]	H_AD[2]	H_AD[4]	M
DVSS	DVSS	DVDDIO	MBIST_FAIL	H_AD[13]	H_AD[23]	H_D[2]	H_AD[16]	H_AD[14]	H_AD[19]	H_AD[10]	N
DVDDIO	DVDDIO	NC	MBIST_EN	H_D[5]	H_D[22]	H_D[11]	H_D[14]	H_AD[21]	H_AD[12]	H_AD[15]	P
NC	NC	NC	DVSS	H_D[7]	H_D[24]	H_D[29]	H_D[20]	H_D[3]	H_AD[17]	H_AD[22]	R
NC	NC	NC	NC	H_D[9]	H_D[4]	DVDDC	H_D[26]	H_AD[5]	H_AD[24]	H_D[0]/SPI_MISO	T
NC	NC	NC	NC	H_D[28]	DVSS	H_D[6]	H_D[31]	H_D[19]	H_D[1]	H_D[8]	U
NC	NC	NC	NC	CLK_MII_RX	MII_RX_ERR	DVDDC	H_D[25]	DVDDC	H_D[23]	H_D[10]	V
NC	NC	NC	NC	MII_RXD[1]	MII_TX_EN	MII_TXD[1]	DVSS	H_D[30]	H_D[27]	H_D[12]	W
DVSS	NC	NC	NC	MII_RXD[3]	MII_RX_DV	MII_CRS	CLK_SSMII_TX	DVDDC	H_D[13]	H_D[15]	Y
NC	ARVDD8	NC	ATVDD8	MII_RXD[0]	MII_COL	CLK_MII_TX	MII_TXD[2]	MDIO	H_D[16]	H_D[17]	AA
NC	ARVSS8	NC	ATVSS8	MII_RXD[2]	MDC	MII_TXD[0]	MII_TXD[3]	MII_TX_ERR	H_D[18]	H_D[21]	AB
12	13	14	15	16	17	18	19	20	21	22	

14.4 DS34T102 Pin Assignment

Figure 14-3. DS34T102 Pin Assignment (TEBGA Package)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC	NC	RLOF/RLOS2	RSYNC1	RDATF1	TTIP2	ATVSS2	RTIP2	ARVSS2	RESREF
B	ARVSS3	ARVDD3	NC	NC	TCLKO2	TCLKF1	TRING2	ATVDD2	RRING2	ARVDD2	DVDDC
C	NC	NC	DVDDLIU	DVDDC	NC	RSYSCLK1	TDATF1	TSYSCLK1/ECLK1	RCLKF2/RCLK2	NC	TDM1_RSIG_RTS
D	ATVDD3	ATVSS3	NC	DVSS	NC	RSER2	NC	NC	TSER1	TDM1_RX	TDM1_RX_SYNC
E	NC	NC	DVSSLIU	NC	DVDDC	NC	RF/RMSYNC2	TSYNC/TSSYNC2	TDM2_ACLK	TDM1_ACLK	TDM1_TSIG_CTS
F	ARVSS4	ARVDD4	NC	NC	NC	DVSS	NC	NC	NC	TDM2_TX_MF_CD	TDM2_TSIG_CTS
G	NC	NC	TST_CLD	NC	DVDDC	NC	NC	TSYSCLK2/ECLK2	NC	TDM2_TCLK	TDM2_TX
H	ATVSS4	ATVDD4	TXENABLE	NC	NC	NC	NC	DVSS	NC	NC	NC
J	CLK_SYS/SCCLK	CLK_SYS_S	TEST_CLK	TSER2	RSER1	NC	NC	TDATF2	NC	DVDDIO	DVDDIO
K	ACVSS2	ACVDD2	JTMS	TCLKF2	NC	NC	RSYSCLK2	RF/RMSYNC1	DVDDIO	DVSS	DVSS
L	CLK_HIGH	DVDDC	JTCLK	RCLKF1/RCLK1	TSYNC/TSSYNC1	RSYNC2	RDATF2	TCLKO1	DVDDIO	DVSS	DVSS
M	ACVSS1	ACVDD1	JTDI	NC	NC	NC	NC	RLOF/RLOS1	DVDDIO	DVSS	DVSS
N	MCLK	DVSS	JTDO	NC	NC	NC	NC	NC	DVDDIO	DVSS	DVSS
P	CLK_CMN	RST_SYS_N	JTRST_N	NC	NC	NC	NC	NC	NC	DVDDIO	DVDDIO
R	ATVSS5	ATVDD5	RXTSEL	NC	NC	NC	NC	DVSS	NC	NC	NC
T	NC	NC	HiZ_N	NC	DVDDC	NC	NC	NC	NC	NC	NC
U	ARVSS5	ARVDD5	NC	NC	NC	DVSS	NC	NC	NC	NC	NC
V	NC	NC	DVDDLIU	NC	DVDDC	NC	NC	NC	NC	NC	NC
W	ATVDD6	ATVSS6	NC	DVSS	NC	NC	NC	NC	NC	NC	NC
Y	NC	NC	DVSSLIU	NC	NC	NC	NC	NC	NC	DVDDC	NC
AA	ARVSS6	ARVDD6	NC	NC	NC	NC	NC	NC	ATVDD7	NC	ARVDD7
AB	NC	NC	NC	NC	NC	NC	NC	NC	ATVSS7	NC	ARVSS7
	1	2	3	4	5	6	7	8	9	10	11

12	13	14	15	16	17	18	19	20	21	22	
DVDDC	RTIP1	ARVSS1	TTIP1	ATVSS1	SD_A[0]	SD_D[6]	SD_A[5]	SD_DQM[0]	SD_D[3]	SD_D[5]	A
DVSS	RRING1	ARVDD1	TRING1	ATVDD1	SD_CS_N	SD_A[3]	SD_A[10]	SD_DQM[2]	SD_D[7]	SD_D[10]	B
TDM1_TX	TDM2_RX_SYNC	TDM2_RSIG_RTS	NC	SD_D[4]	SD_WE_N	SD_D[0]	SD_BA[1]	DVDDC	SD_D[12]	SD_D[14]	C
TDM1_RCLK	TDM2_RX	NC	NC	SD_RAS_N	SD_A[11]	SD_A[9]	DVSS	SD_DQM[3]	SD_D[15]	SD_D[17]	D
TDM2_RCLK	TDM1_TX_SYNC	TDM2_TX_SYNC	NC	SD_CAS_N	SD_A[4]	DVDDC	SD_DQM[1]	DVDDC	SD_D[8]	SD_D[21]	E
TDM1_TCLK	TDM1_TX_MF_CD	NC	NC	SD_A[2]	DVSS	SD_A[1]	SD_A[7]	SD_A[8]	SD_D[1]	SD_D[24]	F
NC	NC	NC	NC	SD_D[29]	SD_BA[0]	DVDDC	SD_D[2]	SD_D[16]	SD_D[19]	SD_D[26]	G
NC	NC	NC	DVSS	SD_CLK	SD_A[6]	SD_D[13]	SD_D[9]	SD_D[11]	SD_D[23]	SD_D[28]	H
DVDDIO	DVDDIO	NC	SCEN	H_WR_BE1_N/SPI_MOSI	H_INT[0]	H_WR_BE2_N/SPI_SEL_N	SD_D[22]	SD_D[18]	SD_D[20]	SD_D[31]	J
DVSS	DVSS	DVDDIO	STMD	H_AD[3]	H_R_W_N/SPI_CP	H_READY_N	H_CPU_SPI_N	SD_D[27]	SD_D[25]	SD_D[30]	K
DVSS	DVSS	DVDDIO	H_AD[11]	H_AD[9]	H_CS_N	H_AD[1]	H_WR_BE0_N/SPI_CLK	H_WR_BE3_N/SPI_CI	DAT_32_16_N	H_INT[1]	L
DVSS	DVSS	DVDDIO	MBIST_DONE	H_AD[7]	H_AD[20]	H_AD[6]	H_AD[18]	H_AD[8]	H_AD[2]	H_AD[4]	M
DVSS	DVSS	DVDDIO	MBIST_FAIL	H_AD[13]	H_AD[23]	H_D[2]	H_AD[16]	H_AD[14]	H_AD[19]	H_AD[10]	N
DVDDIO	DVDDIO	NC	MBIST_EN	H_D[5]	H_D[22]	H_D[11]	H_D[14]	H_AD[21]	H_AD[12]	H_AD[15]	P
NC	NC	NC	DVSS	H_D[7]	H_D[24]	H_D[29]	H_D[20]	H_D[3]	H_AD[17]	H_AD[22]	R
NC	NC	NC	NC	H_D[9]	H_D[4]	DVDDC	H_D[26]	H_AD[5]	H_AD[24]	H_D[0]/SPI_MISO	T
NC	NC	NC	NC	H_D[28]	DVSS	H_D[6]	H_D[31]	H_D[19]	H_D[1]	H_D[8]	U
NC	NC	NC	NC	CLK_MII_RX	MII_RX_ERR	DVDDC	H_D[25]	DVDDC	H_D[23]	H_D[10]	V
NC	NC	NC	NC	MII_RXD[1]	MII_TX_EN	MII_TXD[1]	DVSS	H_D[30]	H_D[27]	H_D[12]	W
DVSS	NC	NC	NC	MII_RXD[3]	MII_RX_DV	MII_CRS	CLK_SSMII_TX	DVDDC	H_D[13]	H_D[15]	Y
NC	ARVDD8	NC	ATVDD8	MII_RXD[0]	MII_COL	CLK_MII_TX	MII_TXD[2]	MDIO	H_D[16]	H_D[17]	AA
NC	ARVSS8	NC	ATVSS8	MII_RXD[2]	MDC	MII_TXD[0]	MII_TXD[3]	MII_TX_ERR	H_D[18]	H_D[21]	AB
12	13	14	15	16	17	18	19	20	21	22	

14.5 DS34T101 Pin Assignment

Figure 14-4. DS34T101 Pin Assignment (TEBGA Package)

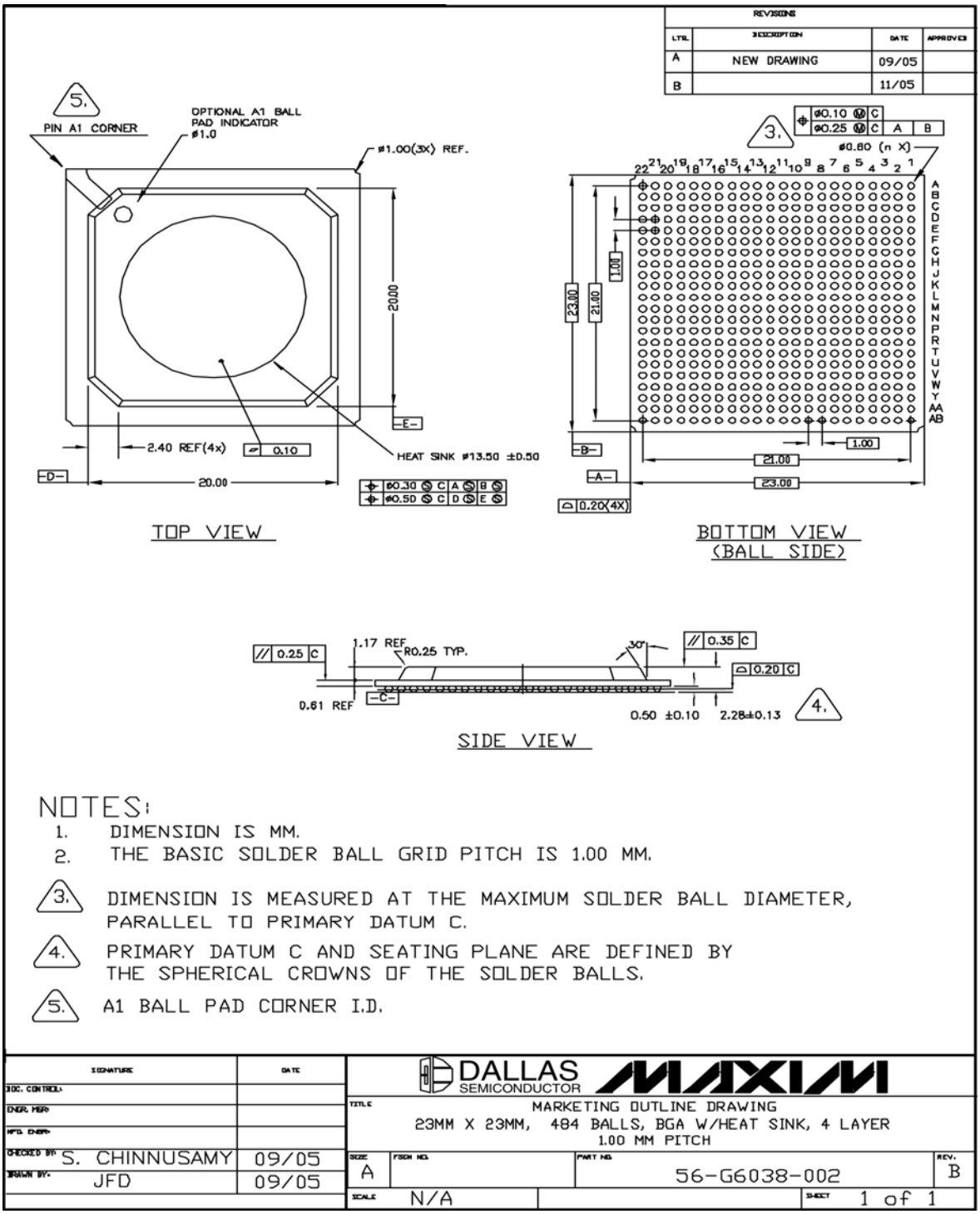
	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC	NC	NC	RSYNC1	RDATF1	NC	ATVSS2	NC	ARVSS2	RESREF
B	ARVSS3	ARVDD3	NC	NC	NC	TCLKF1	NC	ATVDD2	NC	ARVDD2	DVDDC
C	NC	NC	DVDDLIU	DVDDC	NC	RSYSCLK1	TDATF1	TSYSCLK1/ECLK1	NC	NC	TDM1_RSIG_RTS
D	ATVDD3	ATVSS3	NC	DVSS	NC	NC	NC	NC	TSER1	TDM1_RX	TDM1_RX_SYNC
E	NC	NC	DVSSLIU	NC	DVDDC	NC	NC	NC	NC	TDM1_ACLK	TDM1_TSIG_CTS
F	ARVSS4	ARVDD4	NC	NC	NC	DVSS	NC	NC	NC	NC	NC
G	NC	NC	TST_CLD	NC	DVDDC	NC	NC	NC	NC	NC	NC
H	ATVSS4	ATVDD4	TXENABLE	NC	NC	NC	NC	DVSS	NC	NC	NC
J	CLK_SYS/SCCLK	CLK_SYS_S	TEST_CLK	NC	RSER1	NC	NC	NC	NC	DVDDIO	DVDDIO
K	ACVSS2	ACVDD2	JTMS	NC	NC	NC	NC	RF/RMSYNC1	DVDDIO	DVSS	DVSS
L	CLK_HIGH	DVDDC	JTCLK	RCLKF1/RCLK1	TSYNC/TSSYNC1	NC	NC	TCLKO1	DVDDIO	DVSS	DVSS
M	ACVSS1	ACVDD1	JTDI	NC	NC	NC	NC	RLOF/RLOS1	DVDDIO	DVSS	DVSS
N	MCLK	DVSS	JTDO	NC	NC	NC	NC	NC	DVDDIO	DVSS	DVSS
P	CLK_CMN	RST_SYS_N	JTRST_N	NC	NC	NC	NC	NC	NC	DVDDIO	DVDDIO
R	ATVSS5	ATVDD5	RXTSEL	NC	NC	NC	NC	DVSS	NC	NC	NC
T	NC	NC	HIZ_N	NC	DVDDC	NC	NC	NC	NC	NC	NC
U	ARVSS5	ARVDD5	NC	NC	NC	DVSS	NC	NC	NC	NC	NC
V	NC	NC	DVDDLIU	NC	DVDDC	NC	NC	NC	NC	NC	NC
W	ATVDD6	ATVSS6	NC	DVSS	NC	NC	NC	NC	NC	NC	NC
Y	NC	NC	DVSSLIU	NC	NC	NC	NC	NC	NC	DVDDC	NC
AA	ARVSS6	ARVDD6	NC	NC	NC	NC	NC	NC	ATVDD7	NC	ARVDD7
AB	NC	NC	NC	NC	NC	NC	NC	NC	ATVSS7	NC	ARVSS7
	1	2	3	4	5	6	7	8	9	10	11

12	13	14	15	16	17	18	19	20	21	22	
DVDDC	RTIP1	ARVSS1	TTIP1	ATVSS1	SD_A[0]	SD_D[6]	SD_A[5]	SD_DQM[0]	SD_D[3]	SD_D[5]	A
DVSS	RRING1	ARVDD1	TRING1	ATVDD1	SD_CS_N	SD_A[3]	SD_A[10]	SD_DQM[2]	SD_D[7]	SD_D[10]	B
TDM1_TX	NC	NC	NC	SD_D[4]	SD_WE_N	SD_D[0]	SD_BA[1]	DVDDC	SD_D[12]	SD_D[14]	C
TDM1_RCLK	NC	NC	NC	SD_RAS_N	SD_A[11]	SD_A[9]	DVSS	SD_DQM[3]	SD_D[15]	SD_D[17]	D
NC	TDM1_TX_SYNC	NC	NC	SD_CAS_N	SD_A[4]	DVDDC	SD_DQM[1]	DVDDC	SD_D[8]	SD_D[21]	E
TDM1_TCLK	TDM1_TX_MF_CD	NC	NC	SD_A[2]	DVSS	SD_A[1]	SD_A[7]	SD_A[8]	SD_D[1]	SD_D[24]	F
NC	NC	NC	NC	SD_D[29]	SD_BA[0]	DVDDC	SD_D[2]	SD_D[16]	SD_D[19]	SD_D[26]	G
NC	NC	NC	DVSS	SD_CLK	SD_A[6]	SD_D[13]	SD_D[9]	SD_D[11]	SD_D[23]	SD_D[28]	H
DVDDIO	DVDDIO	NC	SCEN	H_WR_BE1_N/SPI_MOSI	H_INT[0]	H_WR_BE2_N/SPI_SEL_N	SD_D[22]	SD_D[18]	SD_D[20]	SD_D[31]	J
DVSS	DVSS	DVDDIO	STMD	H_AD[3]	H_R_W_N/SPI_CP	H_READY_N	H_CPU_SPI_N	SD_D[27]	SD_D[25]	SD_D[30]	K
DVSS	DVSS	DVDDIO	H_AD[11]	H_AD[9]	H_CS_N	H_AD[1]	H_WR_BE0_N/SPI_CLK	H_WR_BE3_N/SPI_CI	DAT_32_16_N	H_INT[1]	L
DVSS	DVSS	DVDDIO	MBIST_DONE	H_AD[7]	H_AD[20]	H_AD[6]	H_AD[18]	H_AD[8]	H_AD[2]	H_AD[4]	M
DVSS	DVSS	DVDDIO	MBIST_FAIL	H_AD[13]	H_AD[23]	H_D[2]	H_AD[16]	H_AD[14]	H_AD[19]	H_AD[10]	N
DVDDIO	DVDDIO	NC	MBIST_EN	H_D[5]	H_D[22]	H_D[11]	H_D[14]	H_AD[21]	H_AD[12]	H_AD[15]	P
NC	NC	NC	DVSS	H_D[7]	H_D[24]	H_D[29]	H_D[20]	H_D[3]	H_AD[17]	H_AD[22]	R
NC	NC	NC	NC	H_D[9]	H_D[4]	DVDDC	H_D[26]	H_AD[5]	H_AD[24]	H_D[0]/SPI_MISO	T
NC	NC	NC	NC	H_D[28]	DVSS	H_D[6]	H_D[31]	H_D[19]	H_D[1]	H_D[8]	U
NC	NC	NC	NC	CLK_MII_RX	MII_RX_ERR	DVDDC	H_D[25]	DVDDC	H_D[23]	H_D[10]	V
NC	NC	NC	NC	MII_RXD[1]	MII_TX_EN	MII_TXD[1]	DVSS	H_D[30]	H_D[27]	H_D[12]	W
DVSS	NC	NC	NC	MII_RXD[3]	MII_RX_DV	MII_CRS	CLK_SSMII_TX	DVDDC	H_D[13]	H_D[15]	Y
NC	ARVDD8	NC	ATVDD8	MII_RXD[0]	MII_COL	CLK_MII_TX	MII_TXD[2]	MDIO	H_D[16]	H_D[17]	AA
NC	ARVSS8	NC	ATVSS8	MII_RXD[2]	MDC	MII_TXD[0]	MII_TXD[3]	MII_TX_ERR	H_D[18]	H_D[21]	AB
12	13	14	15	16	17	18	19	20	21	22	

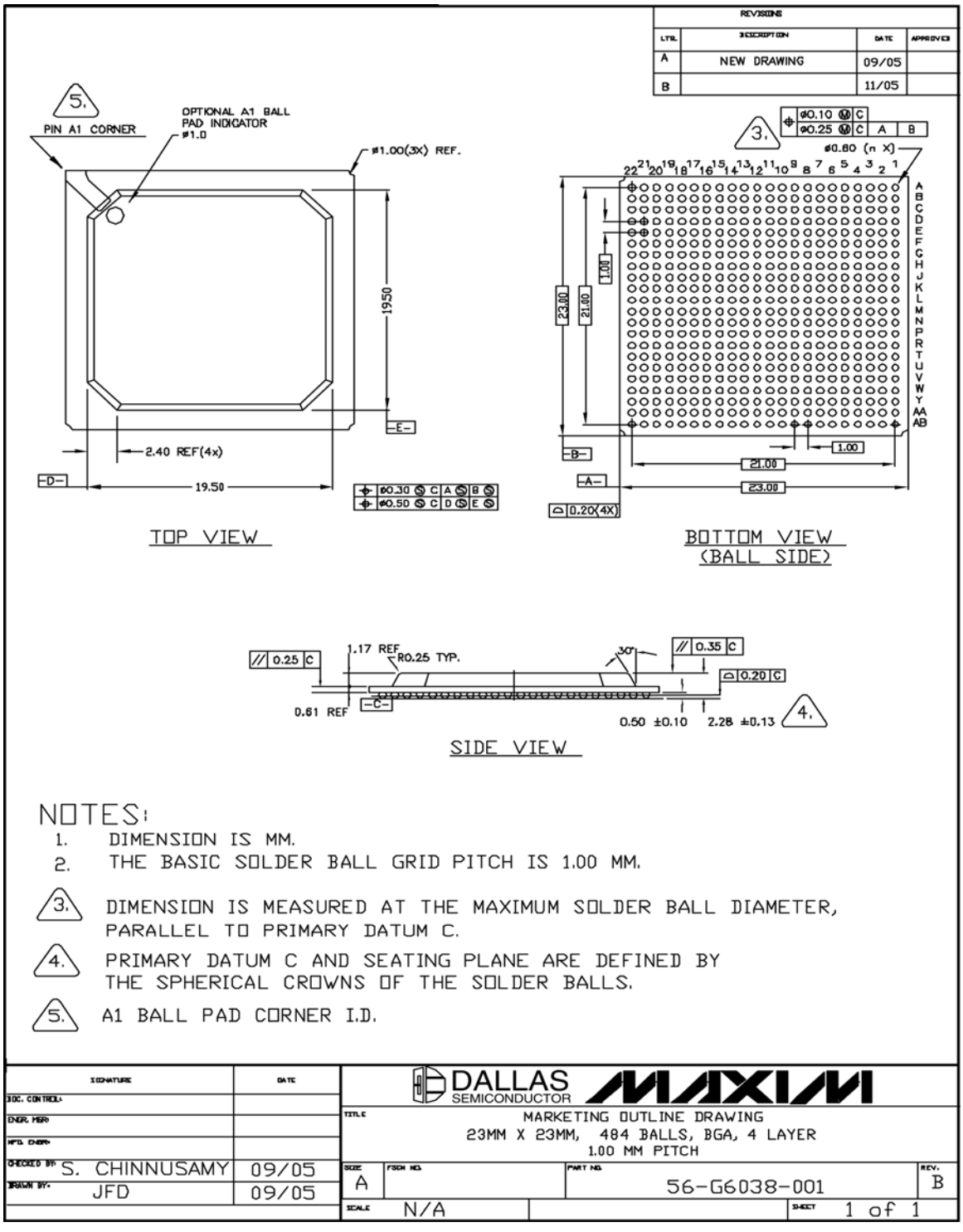
15. Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. The package number provided for each package is a link to the latest package outline information. The 484-ball HSBGA and the 484-ball TEBGA have the same footprint. The difference between the packages is that the HSBGA has an internal heat spreader.)

15.1 484-Ball HSBGA (56-G6038-002)



15.2 484-Ball TEBGA (56-G6038-001)



16. Thermal Information

PARAMETER	VALUE	
	HSBGA	TEBGA
Target Ambient Temperature Range	-40°C to +85°C	-40°C to +85°C
Die Junction Temperature Range	-40°C to +125°C	-40°C to +125°C
Theta-JC (Junction to Top of Case)	2.2°C/W	5.4°C/W
Theta-JB (Junction to Bottom Pins)	5.2°C/W	11.2°C/W
Theta-JA, Still Air (Note 1)	12.5°C/W	19.7°C/W

Note 1: Theta-JA values are estimates using JEDEC-standard PCB and enclosure dimensions.

17. Document Revision History

REVISION	DESCRIPTION
072707	New product release.