DATA SHEET

512MB Registered SDRAM DIMM

EBS51RC4ACFC (64M words × 72 bits, 1 bank)

Description

The EBS51RC4ACFC is 64M words × 72 bits, 1 bank Synchronous Dynamic RAM Registered Module, mounted 18 pieces of 256M bits SDRAM sealed in TSOP package. This module provides high density and large quantities of memory in a small space without utilizing the surface mounting technology. Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Fully compatible with 8 bytes DIMM: JEDEC standard outline
- 168-pin socket type dual in line memory module (DIMM)
  - PCB height: 30.48mm (1.20inch)
  - Lead pitch: 1.27mm
- 3.3V power supply
- Clock frequency: 133MHz (max.)
- LVTTL interface
- Data bus width: × 72 ECC
- Single pulsed /RAS
- 4 Banks can operates simultaneously and independently
- Burst read/write operation and burst read/single write operation capability
- Programmable burst length (BL): 1, 2, 4, 8
- 2 variations of burst sequence
  - Sequential
  - Interleave
- Programmable /CAS latency (CL): 2, 3
- Registered inputs with one clock delay
- Byte control by DQMB
- Refresh cycles: 8192 refresh cycles/64ms
- 2 variations of refresh
  - Auto refresh
  - Self refresh
- 1 piece of PLL clock driver, 3 pieces of register driver and 1 piece of serial EEPROM (2k bits) for Presence Detect (SPD) on PCB.

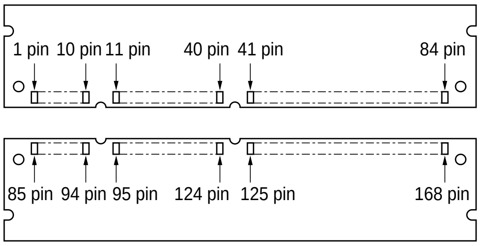
Document No. E0108E30 (Ver. 3.0)
Date Published May 2002 (K) Japan
URL: http://www.elpida.com

Ordering Information

Part number	Clock frequency MHz (max.)	/CAS latency	Package	Contact pad	Mounted devices
EBS51RC4ACFC-7A	133	2, 3	168-pin DIMM	Gold	EDS2504ACTA
EBS51RC4ACFC-75*	133	3			

Note: 100MHz operation at /CAS latency = 2.

Pin Configurations



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	VSS	43	VSS	85	VSS	127	VSS
2	DQ0	44	NC	86	DQ32	128	CKE0
3	DQ1	45	/CS2	87	DQ33	129	NC
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	VDD	48	NC	90	VDD	132	NC
7	DQ4	49	VDD	91	DQ36	133	VDD
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	VSS	54	VSS	96	VSS	138	VSS
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VDD	101	DQ45	143	VDD
18	VDD	60	DQ20	102	VDD	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	NC	105	CB4	147	REGE
22	CB1	64	VSS	106	CB5	148	VSS
23	VSS	65	DQ21	107	VSS	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VDD	68	VSS	110	VDD	152	VSS
27	/WE	69	DQ24	111	/CAS	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	/CS0	72	DQ27	114	NC	156	DQ59

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
31	NC	73	VDD	115	/RAS	157	VDD
32	VSS	74	DQ28	116	VSS	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	VSS	120	A7	162	VSS
37	A8	79	CLK2	121	A9	163	CLK3
38	A10 (AP)	80	NC	122	BA0	164	NC
39	BA1	81	NC	123	A11	165	SA0
40	VDD	82	SDA	124	VDD	166	SA1
41	VDD	83	SCL	125	CLK1	167	SA2
42	CLK0	84	VDD	126	A12	168	VDD

Pin Description

Pin name	Function
A0 to A12	Address input — Row address A0 to A12 — Column address A0 to A9, A11
BA0, BA1	Bank select address
DQ0 to DQ63	Data input/output
CB0 to CB7	Check bit (Data input/output)
/CS0, /CS2	Chip select input
/RAS	Row enable (/RAS) input
/CAS	Column enable (/CAS) input
/WE	Write enable input
DQMB0 to DQMB7	Byte data mask
CLK0 to CLK3	Clock input
CKE0	Clock enable input
REGE*[1]	Register/Buffer enable
SDA	Data input/output for serial PD
SCL	Clock input for serial PD
SA0 to SA2	Serial address input
VDD	Primary positive power supply
VSS	Ground
NC	No connection

Note: 1. REGE ≥ VIH: Register mode.
REGE ≤ VIL: Buffer mode.

Serial PD Matrix*[1]

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
0	Number of bytes used by module manufacturer	1	0	0	0	0	0	0	0	80H	128
1	Total SPD memory size	0	0	0	0	1	0	0	0	08H	256 byte
2	Memory type	0	0	0	0	0	1	0	0	04H	SDRAM
3	Number of row addresses bits	0	0	0	0	1	1	0	1	0DH	13
4	Number of column addresses bits	0	0	0	0	1	0	1	1	0BH	11
5	Number of banks	0	0	0	0	0	0	0	1	01H	1
6	Module data width	0	1	0	0	1	0	0	0	48H	72 bit
7	Module data width (continued)	0	0	0	0	0	0	0	0	00H	0 (+)
8	Module interface signal levels	0	0	0	0	0	0	0	1	01H	LVTTL
9	SDRAM cycle time (highest /CAS latency) 7.5ns	0	1	1	1	0	1	0	1	75H	CL = 3*[5]
10	SDRAM access from Clock (highest /CAS latency) 5.4ns	0	1	0	1	0	1	0	0	54H	
11	Module configuration type	0	0	0	0	0	0	1	0	02H	ECC
12	Refresh rate/type	1	0	0	0	0	0	1	0	82H	Normal (7.8125μs) Self refresh
13	SDRAM width	0	0	0	0	0	1	0	0	04H	64M × 4
14	Error checking SDRAM width	0	0	0	0	0	1	0	0	04H	× 4
15	SDRAM device attributes: minimum clock delay for back-to-back random column addresses	0	0	0	0	0	0	0	1	01H	1 CLK
16	SDRAM device attributes: Burst lengths supported	0	0	0	0	1	1	1	1	0FH	1, 2, 4, 8
17	SDRAM device attributes: number of banks on SDRAM device	0	0	0	0	0	1	0	0	04H	4
18	SDRAM device attributes: /CAS latency	0	0	0	0	0	1	1	0	06H	2, 3
19	SDRAM device attributes: /CS latency	0	0	0	0	0	0	0	1	01H	0
20	SDRAM device attributes: /WE latency	0	0	0	0	0	0	0	1	01H	0
21	SDRAM device attributes	0	0	0	1	1	1	1	1	1FH	Registered
22	SDRAM device attributes: General	0	0	0	0	1	1	1	0	0EH	VDD ± 10%
23	SDRAM cycle time (2nd highest /CAS latency) (-7A) 7.5ns	0	1	1	1	0	1	0	1	75H	CL = 2*[5]
	(-75) 10ns	1	0	1	0	0	0	0	0	A0H	
24	SDRAM access from Clock (2nd highest /CAS latency) (-7A)5.4ns	0	1	0	1	0	1	0	0	54H	
	(-75) 6ns	0	1	1	0	0	0	0	0	60H	
25	SDRAM cycle time (3rd highest /CAS latency) Undefined	0	0	0	0	0	0	0	0	00H	
26	SDRAM access from Clock (3rd highest /CAS latency) Undefined	0	0	0	0	0	0	0	0	00H	

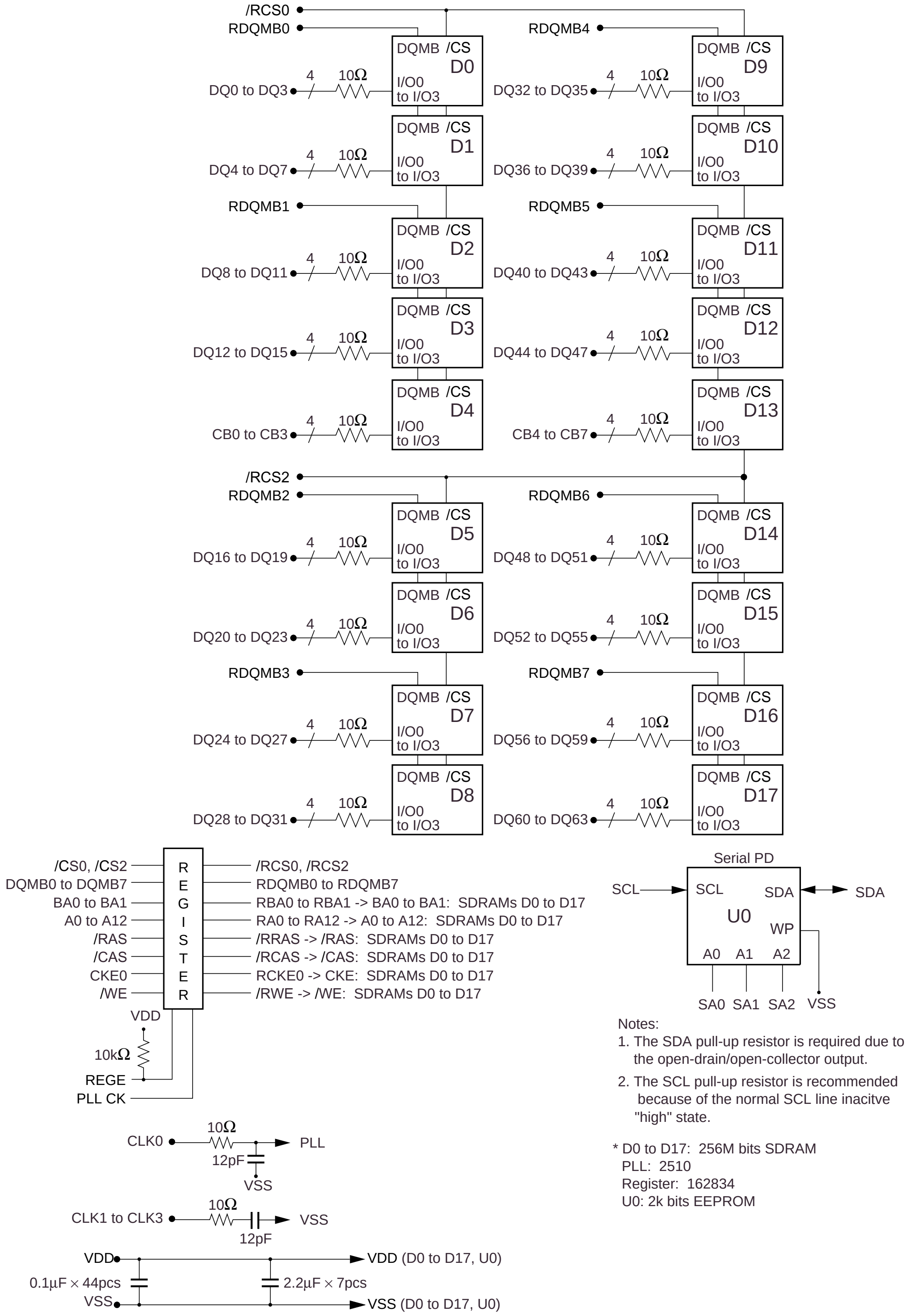
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
27	Minimum row precharge time (-7A)	0	0	0	0	1	1	1	1	0FH	15ns
	(-75)	0	0	0	1	0	1	0	0	14H	20ns
28	Row active to row active min	0	0	0	0	1	1	1	1	0FH	15ns
29	/RAS to /CAS delay min (-7A)	0	0	0	0	1	1	1	1	0FH	15ns
	(-75)	0	0	0	1	0	1	0	0	14H	20ns
30	Minimum /RAS pulse width	0	0	1	0	1	1	0	1	2DH	45ns
31	Density of each bank on module	1	0	0	0	0	0	0	0	80H	1 bank 512M byte
32	Address and command signal input setup time	0	0	0	1	0	1	0	1	15H	1.5ns*5
33	Address and command signal input hold time	0	0	0	0	1	0	0	0	08H	0.8ns*5
34	Data signal input setup time	0	0	0	1	0	1	0	1	15H	1.5ns*5
35	Data signal input hold time	0	0	0	0	1	0	0	0	08H	0.8ns*5
36 to 40	Superset information	0	0	0	0	0	0	0	0	00H	Future use
41	Minimum bank Cycle (-7A)	0	0	1	1	1	1	0	0	3CH	60ns
	(-75)	0	1	0	0	0	0	1	1	43H	67.5ns
42 to 61	Superset information	0	0	0	0	0	0	0	0	00H	Future use
62	SPD data revision code	0	0	0	1	0	0	1	0	12H	Rev. 1.2
63	Checksum for bytes 0 to 62 (-7A)	1	0	1	1	0	1	1	1	B7H	183
	(-75)	1	1	1	1	1	1	1	1	FFH	255
64 to 65	Manufacturer's JEDEC ID code	0	1	1	1	1	1	1	1	7FH	Continuation code
66	Manufacturer's JEDEC ID code	1	1	1	1	1	1	1	0	FEH	Elpida Memory
67 to 71	Manufacturer's JEDEC ID code	0	0	0	0	0	0	0	0	00H	
72	Manufacturing location	×	×	×	×	×	×	×	×	××	*2 (ASCII-8bit code)
73	Manufacturer's part number	0	1	0	0	0	1	0	1	45H	E
74	Manufacturer's part number	0	1	0	0	0	0	1	0	42H	B
75	Manufacturer's part number	0	1	0	1	0	0	1	1	53H	S
76	Manufacturer's part number	0	0	1	1	0	1	0	1	35H	5
77	Manufacturer's part number	0	0	1	1	0	0	0	1	31H	1
78	Manufacturer's part number	0	1	0	1	0	0	1	0	52H	R
79	Manufacturer's part number	0	1	0	0	0	0	1	1	43H	C
80	Manufacturer's part number	0	0	1	1	0	1	0	0	34H	4
81	Manufacturer's part number	0	1	0	0	0	0	0	1	41H	A
82	Manufacturer's part number	0	1	0	0	0	0	1	1	43H	C
83	Manufacturer's part number	0	1	0	0	0	1	1	0	46H	F
84	Manufacturer's part number	0	1	0	0	0	0	1	1	43H	C
85	Manufacturer's part number	0	0	1	0	1	1	0	1	2DH	—
86	Manufacturer's part number	0	0	1	1	0	1	1	1	37H	7
87	Manufacturer's part number (-7A)	0	1	0	0	0	0	0	1	41H	A
	(-75)	0	0	1	1	0	1	0	1	35H	5
88	Manufacturer's part number	0	0	1	0	0	0	0	0	20H	(Space)

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
89	Manufacturer's part number	0	0	1	0	0	0	0	0	20H	(Space)
90	Manufacturer's part number	0	0	1	0	0	0	0	0	20H	(Space)
91	Revision code	0	0	1	1	0	0	0	0	30H	Initial
92	Revision code	0	0	1	0	0	0	0	0	20H	(Space)
93	Manufacturing date	×	×	×	×	×	×	×	×	××	Year code (BCD)
94	Manufacturing date	×	×	×	×	×	×	×	×	××	Week code (BCD)
95 to 98	Assembly serial number	*3									
99 to 125	Manufacturer specific data	—	—	—	—	—	—	—	—	—	*4
126	Reserved (Intel specification frequency)	0	1	1	0	0	1	0	0	64H	
127	Reserved (Intel specification /CAS# latency support)	1	0	0	0	0	1	1	1	87H	

Notes: 1. All serial PD data are not protected. 0: Serial data, "Low", 1: Serial data, "High".

2. Byte72 is manufacturing location code. (ex: In case of Japan, byte72 is 4AH. 4AH shows "J" on ASCII code.)
3. Bytes 95 through 98 are assembly serial number.
4. All bits of 99 through 125 are not defined ("1" or "0").
5. These specifications are defined based on component specification, not module.

Block Diagram



Notes:
1. The SDA pull-up resistor is required due to the open-drain/open-collector output.
2. The SCL pull-up resistor is recommended because of the normal SCL line inacitve "high" state.

* D0 to D17: 256M bits SDRAM
PLL: 2510
Register: 162834
U0: 2k bits EEPROM

Electrical Specifications

- All voltages are referenced to VSS (GND).

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to VSS	VT	–0.5 to VDD + 0.5 (≤ 4.6 (max.))	V	
Supply voltage relative to VSS	VDD	–0.5 to +4.6	V	
Short circuit output current	IOS	50	mA	
Power dissipation	PD	18	W	
Operating temperature	TA	0 to +70	°C	1
Storage temperature	Tstg	–55 to +125	°C	

Notes: 1. SDRAM device specification

Caution **Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.**

DC Operating Conditions (TA = 0 to +70°C) (SDRAM device specification)

Parameter	Symbol	min.	max.	Unit	Note
Supply voltage	VDD	3.0	3.6	V	1
	VSS	0	0	V	2
Input high voltage	VIH	2.0	VDD + 0.3	V	3
Input low voltage	VIL	–0.3	0.8	V	4

Notes: 1. The supply voltage with all VDD pins must be on the same level.
2. The supply voltage with all VSS pins must be on the same level.
3. VIH (max.) = VDD + 2.0V for pulse width ≤ 3ns at VDD.
4. VIL (min.) = VSS – 2.0V for pulse width ≤ 3ns at VSS.

DC Characteristics1 (TA = 0 to 70°C, VDD = 3.3V ± 0.3V, VSS = 0V)

Parameter	Symbol	Grade	max.	Unit	Test condition	Notes
Operating current	ICC1	-7A	3035	mA	Burst length = 1 tRC = tRC (min.)	1, 2, 3
	ICC1	-75	2675	mA		
Standby current in power down	ICC2P		749	mA	CKE = VIL, tCK = 12ns	6
Standby current in non power down	ICC2N		1055	mA	CKE, /CS = VIH, tCK = 12ns	4
Active standby current in power down	ICC3P		767	mA	CKE = VIL, tCK = 12ns	1, 2, 6
Active standby current in non power down	ICC3N		1235	mA	CKE, /CS = VIH, tCK = 12ns	1, 2, 4
Burst operating current	ICC4		3035	mA	tCK = tCK (min.), BL = 4	1, 2, 5
Refresh current	ICC5	-7A	5195	mA	tRC = tRC (min.)	3
	ICC5	-75	4655	mA		
Self refresh current	ICC6		749	mA	VIH ≥ VDD – 0.2V VIL ≤ 0.2V	7

Notes: 1. ICC depends on output load condition when the device is selected. ICC (max.) is specified at the output open condition.
2. One bank operation.
3. Input signals are changed once per one clock.
4. Input signals are changed once per two clocks.
5. Input signals are changed once per four clocks.
6. After power down mode, CLK operating current.
7. After self refresh mode set, self refresh current.

DC Characteristics2 (TA = 0 to 70°C, VDD = 3.3V ± 0.3V, VSS = 0V)

Parameter	Symbol	min.	max.	Unit	Test condition	Notes
Input leakage current	ILI	–10	10	μA	0 ≤ VIN ≤ VDD	
Output leakage current	ILO	–10	10	μA	0 ≤ VOUT ≤ VDD DQ = disable	
Output high voltage	VOH	2.4	—	V	IOH = –4mA	
Output low voltage	VOL	—	0.4	V	IOL = 4mA	

Pin Capacitance (TA = 25°C, VDD = 3.3V ± 0.3V)

Parameter	Symbol	Pins	max.	Unit	Notes
Input capacitance	CI1	Address	23	pF	1, 2, 4
	CI2	/RAS, /CAS, /WE	23	pF	1, 2, 4
	CI3	CKE	23	pF	1, 2, 4
	CI4	/CS	15	pF	1, 2, 4
	CI5	CLK	40	pF	1, 2, 4
	CI6	DQMB	15	pF	1, 2, 4
Data input/output capacitance	CI/O1	DQ, CB	15	pF	1, 2, 3, 4

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. Measurement condition: f = 1MHz, 1.4V bias, 200mV swing.
3. DQMB = VIH to disable Data-out.
4. This parameter is sampled and not 100% tested.

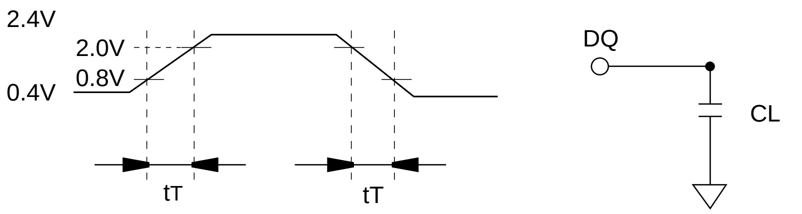
AC Characteristics (TA = 0 to 70°C, VDD = 3.3V ± 0.3V, VSS = 0V) (SDRAM device specification)

		-7A	-75			
Parameter	Symbol	min.	min.	max.	Unit	Notes
System clock cycle time	tCK	7.5	7.5	—	ns	1
CLK high pulse width	tCH	2.5	2.5	—	ns	1
CLK low pulse width	tCL	2.5	2.5	—	ns	1
Access time from CLK	tAC	—	—	5.4	ns	1, 2
Data-out hold time	tOH	2.7	2.7	—	ns	1, 2
CLK to Data-out low impedance	tLZ	1	1	—	ns	1, 2, 3
CLK to Data-out high impedance	tHZ	—	—	5.4	ns	1, 4
Input setup time	tSI	1.5	1.5	—	ns	1
Input hold time	tHI	0.8	0.8	—	ns	1
Ref/Active to Ref/Active command period	tRC	60	67.5	—	ns	1
Active to Precharge command period	tRAS	45	45	120000	ns	1
Active command to column command (same bank)	tRCD	15	20	—	ns	1
Precharge to active command period	tRP	15	20	—	ns	1
Write recovery or data-in to precharge lead time	tDPL	15	15	—	ns	1
Last data into active latency	tDAL	2CLK + 15ns	2CLK + 20ns	—		
Active (a) to Active (b) command period	tRRD	15	15	—	ns	1
Transition time (rise and fall)	tT	0.5	0.5	5	ns	
Refresh period (8192 refresh cycles)	tREF	—	—	64	ms	

Notes: 1. AC measurement assumes tT = 0.5ns. Reference level for timing of input signals is 1.4V.
2. Access time is measured at 1.4V. Load condition is C_L = 50pF.
3. tLZ (min.) defines the time at which the outputs achieves the low impedance state.
4. tHZ (max.) defines the time at which the outputs achieves the high impedance state.

Test Conditions

- Input and output timing reference levels: 1.4V
- Input waveform and output load: See following figures



Input Waveform and Output Load

Relationship Between Frequency and Minimum Latency (SDRAM device specification)

Parameter		-7A		-75		
Frequency (MHz)		133	133	133	100	
tCK (ns)		7.5	7.5	7.5	10	
/CAS latency	Symbol	CL = 3	CL = 2	CL = 3	CL = 2	Notes
Active command to column command (same bank)	IRCD	2	2	3	2	1
Active command to active command (same bank)	IRC	8	8	9	7	1
Active command to precharge command (same bank)	IRAS	6	6	6	5	1
Precharge command to active command (same bank)	IRP	2	2	3	2	1
Write recovery or data-in to precharge command (same bank)	IDPL	2	2	2	2	1
Active command to active command (different bank)	IRRD	2	2	2	2	1
Self refresh exit time	ISREX	1	1	1	1	2
Last data in to active command (Auto precharge, same bank)	IDAL	4	4	5	4	= [IDPL + IRP]
Self refresh exit to command input	ISEC	8	8	9	7	= [IRC] 3
Precharge command to high impedance	IHZP	3	2	3	2	
Last data out to active command (Auto precharge, same bank)	IAPR	1	1	1	1	
Last data out to precharge (early precharge)	IEP	–2	–1	–2	–1	
Column command to column command	ICCD	1	1	1	1	
Write command to data in latency	IWCD	0	0	0	0	
DQM to data in	IDID	0	0	0	0	
DQM to data out	IDOD	2	2	2	2	
CKE to CLK disable	ICLE	1	1	1	1	
Register set to active command	IMRD	1	1	1	1	
/CS to command disable	ICDD	0	0	0	0	
Power down exit to command input	IPEC	1	1	1	1	

Notes: 1. IRCD to IRRD are recommended value.
2. Be valid [DESL] or [NOP] at next command of self refresh exit.
3. Except [DESL] and [NOP]

Pin Functions

CLK0 to CLK3 (input pin): CLK is the master clock input to this pin. The other input signals are referred at CLK rising edge.

/CS0, /CS2 (input pin): When /CS is Low, the command input cycle becomes valid. When /CS is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

/RAS, /CAS and /WE (input pins): Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.

A0 to A12 (input pins): Row address (AX0 to AX12) is determined by A0 to A12 level at the bank active command cycle CLK rising edge. Column address (AY0 to AY9, AY11) is determined by A0 to A9, A11 level at the read or write command cycle CLK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, all banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0 and BA1 (BA) is precharged.

BA0 and BA1 (input pin)

BA0 and BA1 are bank select signal (BA). (See Bank Select Signal Table)

[Bank Select Signal Table]

	BA0	BA1
Bank 0	L	L
Bank 1	H	L
Bank 2	L	H
Bank 3	H	H

Remark: H: VIH. L: VIL.

CKE0 (input pin): This pin determines whether or not the next CLK is valid. If CKE is High, the next CLK rising edge is valid. If CKE is Low, the next CLK rising edge is invalid. This pin is used for power-down and clock suspend modes.

DQMB0 to DQMB7 (input pins): Read operation: If DQMB is High, the output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z.

Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.

DQ0 to DQ63, CB0 to CB7 (input/output pins): Data is input to and output from these pins.

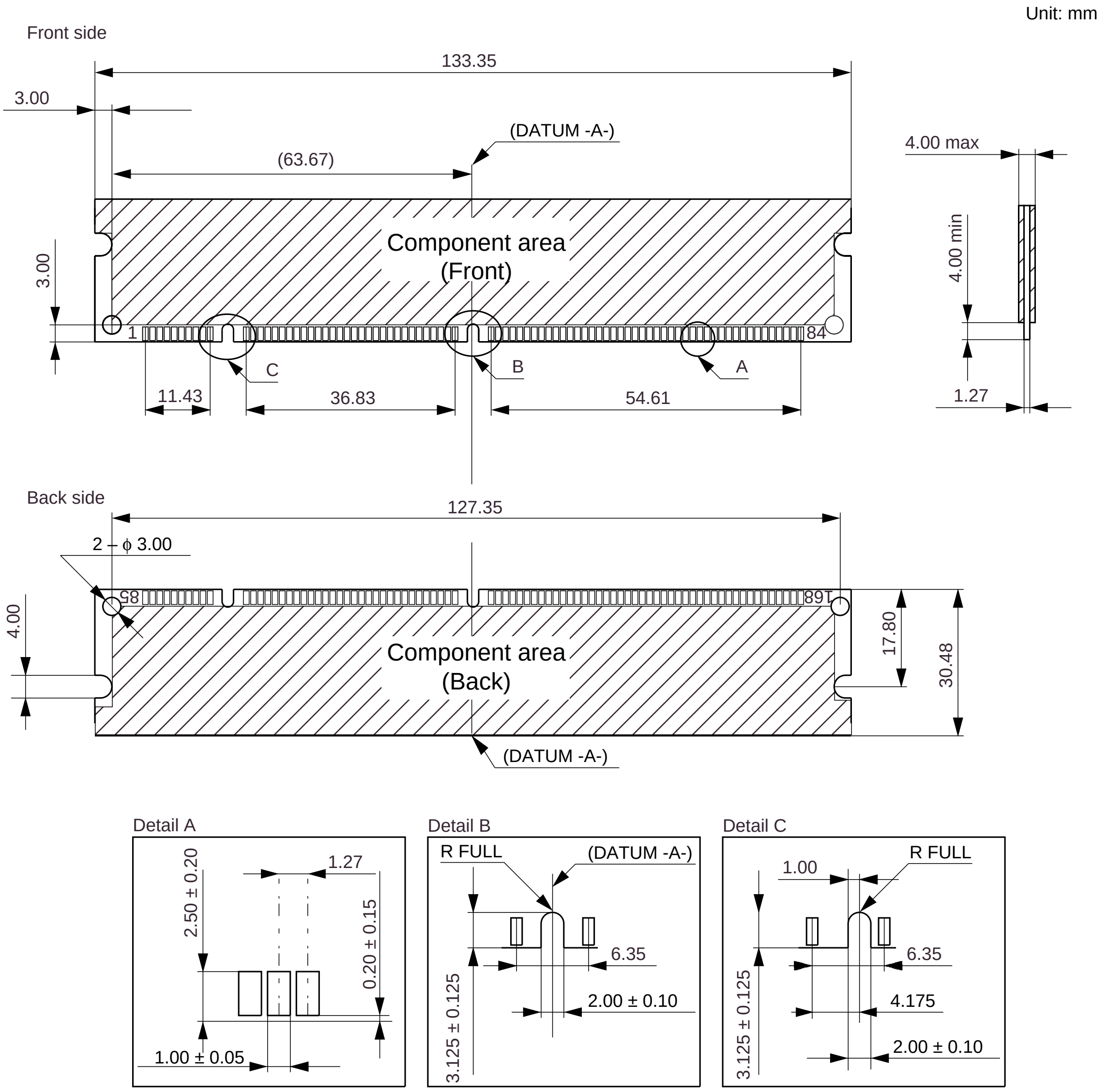
VDD (power supply pins): 3.3V is applied.

VSS (power supply pins): Ground is connected.

Detailed Operation Part

Refer to the EDS2504ACTA/08ACTA/16ACTA datasheet (E0277E).

Physical Outline



Note: Tolerance on all dimensions ± 0.15 unless otherwise specified.

ECA-TS2-0027-01

CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory ICs, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.
In particular, do not push module cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.

When re-packing memory modules, be sure the modules are not touching each other.
Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

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