PRELIMINARY

256Kx32 Static RAM CMOS, High Speed Module

The EDI8F32256C is a high speed 8 megabit Static RAM module organized as 256K words by 32 bits. This module is constructed from eight 256Kx4 Static RAMs in SOJ packages on an epoxy laminate (FR4) board.

Four chip selects ($\overline{E1}$-$\overline{E4}$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

The EDI8F32256C is offered in a 64 pin ZIP package which enables eight megabits of memory to be placed in less than 1.3 square inches of board space.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation and providing equal access and cycle times for ease of use.

Two pins, PD1 and PD2, are used to identify module memory density in applications where alternate modules can be interchanged.

Features

256Kx32 bit CMOS Static Random Access Memory
- Access Times 25, 30, 35, 45, and 55ns
- Individual Byte Selects
- Fully Static, No Clocks
- TTL Compatible I/O

High Density Package
- JEDEC Standard Pinout
- 64 Pin ZIP, No. 85
- Common Data Inputs and Outputs

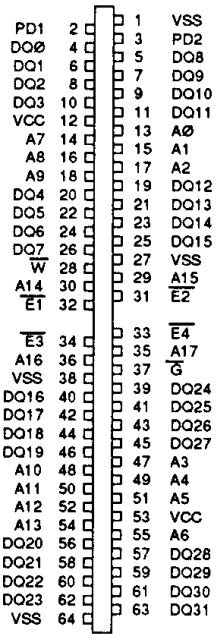
Single +5V (±10%) Supply Operation

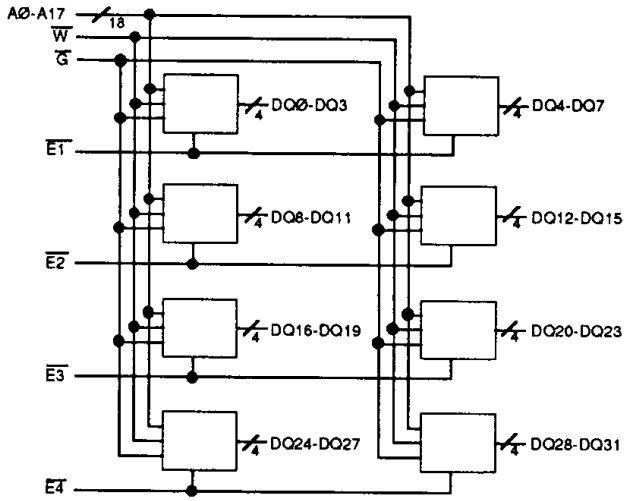
Pin Names

AØ-A17	Address Inputs
$\overline{E1}$-$\overline{E4}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ31	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground

Pin Configuration and Block Diagram

PD1 = GND
PD2 = GND





Absolute Maximum Ratings*

Voltage on any pin relative to VSS ..... -0.5V to 7.0V
Operating Temperature TA (Ambient)
Commercial. ..... 0°C to +70°C
Industrial ..... -40°C to +85°C
Storage Temperature, Plastic ..... -55°C to +125°C
Power Dissipation ..... 1 Watt
Output Current. ..... 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels ..... VSS to 3.0V
Input Rise and Fall Times 5ns
Input and Output Timing Levels 1.5V
Output Load ..... 1TTL, CL = 30pF
(note: For TEHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle	--	600	960	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH, VIN ≤ VIL or VIN ≥ VIH	--	100	180	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$ ≥ VCC-0.2V VIN ≥ VCC-0.2V or VIN ≤ 0.2V	--	5	10	mA
Input Leakage Current	ILI	VIN = 0V to VCC	--	--	80	µA
Output Leakage Current	ILO	V I/O = 0V to VCC	--	--	20	µA
Output High Voltage	VOH	IOH = -4.0mA	2.4	--	--	V
Output Low Voltage	VOL	IOL = 8.0mA	--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{E}$	$\overline{W}$	$\overline{G}$	Mode	Output	Power
H	X	X	Standby	HIGH Z	ICC3
L	H	X	Read	DOUT	ICC1
L	L	H	Write	HIGH Z	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Input Capacitance (Except DQ Pins)	CI	60	pF
Capacitance Control (DQ Pins)	CD/Q	30	pF
Input Capacitance ($\overline{E}$)	CC	20	pF
Input Capacitance ($\overline{W}$)	CN	60	pF

These parameters are sampled, not 100% tested.

AC Characteristics
Read Cycle

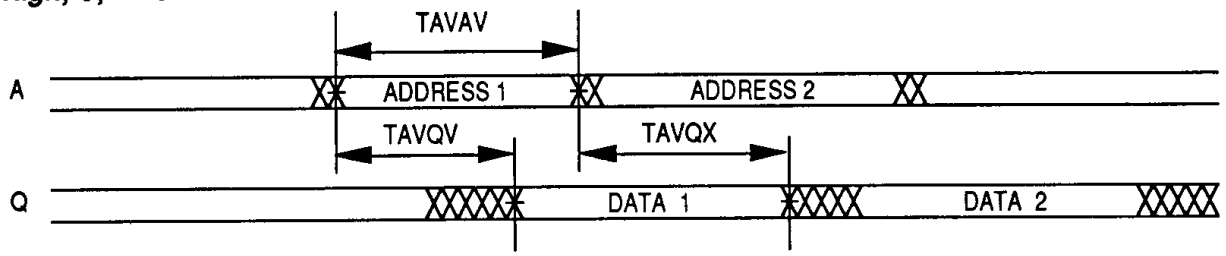
Parameter	Symbol	25ns		30ns		Units
		Min	Max	Min	Max	
Read Cycle Time	TAVAV	25		30		ns
Address Access Time	TAVQV		25		30	ns
Chip Enable Access Time	TELQV		25		30	ns
Chip Enable to Output in Low Z (1)	TELQX	3		3		ns
Output Enable to Output Valid	TGLQV		12		15	ns
Output Enable to Output in Low Z (1)	TGLQX	0		0		ns
Chip Disable to Output in High Z (1)	TEHQZ		15		15	ns
Output Disable to Output in High Z(1)	TGHQZ		15		15	ns
Output Hold from Address Change	TAVQX	3		3		ns

Note 1: Parameter guaranteed, but not tested.

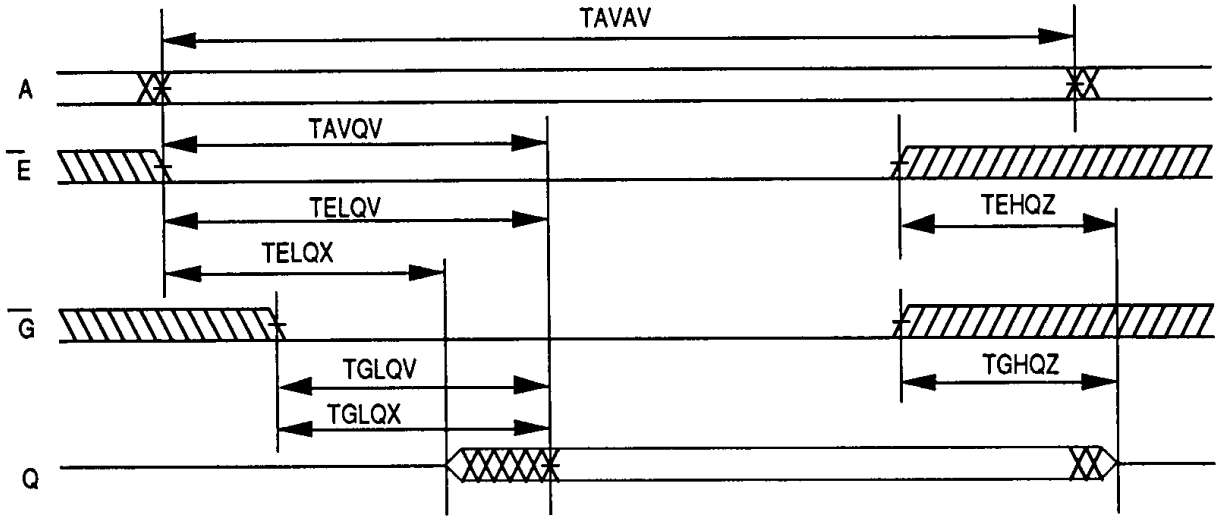
Parameter	Symbol	35ns		45ns		55ns		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	35		45		55		ns
Address Access Time	TAVQV		35		45		55	ns
Chip Enable Access Time	TELQV		35		45		55	ns
Chip Enable to Output in Low Z (1)	TELQX	3		3		3		ns
Output Enable to Output Valid	TGLQV		20		25		25	ns
Output Enable to Output in Low Z (1)	TGLQX	0		0		0		ns
Chip Disable to Output in High Z (1)	TEHQZ		20		20		20	ns
Output Disable to Output in High Z(1)	TGHQZ		20		20		20	ns
Output Hold from Address Change	TAVQX	3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1
$\overline{W}$ High; $\overline{G}$, $\overline{E}$ Low



Read Cycle 2
$\overline{W}$ High



AC Characteristics
Write Cycle

Parameter	Symbol		25ns		30ns		Units
			Min	Max	Min	Max	
Write Cycle Time	TAVAV		25		30		ns
Chip Enable to	TELWH	$\overline{W}$	20		25		ns
End of Write	TWLEH	$\overline{E}$	20		25		ns
Address Setup Time	TAVWL	$\overline{W}$	0		0		ns
	TAVEL	$\overline{E}$	0		0		ns
Address Valid to	TAVWH	$\overline{W}$	20		25		ns
End of Write	TAVEH	$\overline{E}$	20		25		ns
Write Pulse Width	TWLWH	$\overline{W}$	20		25		ns
	TELEH	$\overline{E}$	20		25		ns
Write Recovery Time	TWHAX	$\overline{W}$	3		3		ns
	TEHAX	$\overline{E}$	3		3		ns
Data Hold Time	TWHDX	$\overline{W}$	0		0		ns
	TEHDX	$\overline{E}$	0		0		ns
Write to Output in High Z (1)	TWLQZ		0	10	0	15	ns
Data to Write Time	TDVWH	$\overline{W}$	15		20		ns
	TDVEH	$\overline{E}$	15		20		ns
Output Active from End of Write (1)	TWHQX		0		0		ns

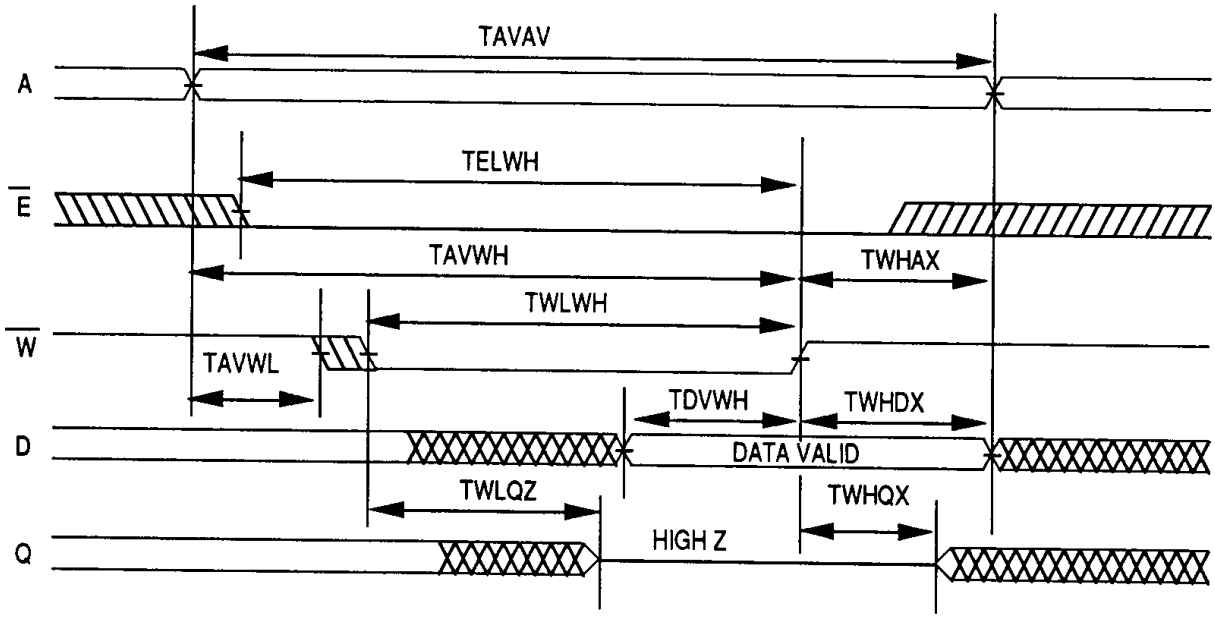
Note 1: Parameter guaranteed, but not tested.

AC Characteristics
Write Cycle

Parameter	Symbol		35ns		45ns		55ns		Units
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		35		45		55		ns
Chip Enable to	TELWH	$\overline{W}$	30		40		50		ns
End of Write	TWLEH	$\overline{E}$	30		40		50		ns
Address Setup Time	TAVWL	$\overline{W}$	0		0		0		ns
	TAVEL	$\overline{E}$	0		0		0		ns
Address Valid to	TAVWH	$\overline{W}$	30		35		40		ns
End of Write	TAVEH	$\overline{E}$	30		35		40		ns
Write Pulse Width	TWLWH	$\overline{W}$	30		35		40		ns
	TELEH	$\overline{E}$	30		35		40		ns
Write Recovery Time	TWHAX	$\overline{W}$	5		5		5		ns
	TEHAX	$\overline{E}$	5		5		5		ns
Data Hold Time	TWHDX	$\overline{W}$	0		0		0		ns
	TEHDX	$\overline{E}$	0		0		0		ns
Write to Output in High Z (1)	TWLQZ		0	15	0	20	0	20	ns
Data to Write Time	TDVWH	$\overline{W}$	15		20		20		ns
	TDVEH	$\overline{E}$	15		20		20		ns
Output Active from End of Write (1)	TWHQX		0		0		0		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled