Ultra Low Power Multi I/O Microcontroller

Features

- Low Power - typical 1.7µA active mode
  - typical 0.3µA standby mode
  @ 1.5V, 32kHz, 25°C
- Low Voltage - 1.2 to 1.7V
- buzzer - 2kHz
- ROM - 1536×16bit (Mask Programmed)
- RAM - 72 × 4bit (User Read/Write)
- 2 clocks per instruction cycle
- RISC architecture
- 3 software configurable 4-bit ports
- 1 input port
- 1 high current output port
- 1 Input or Output port - bitwise
- Up to 8 outputs (2 ports)
- Voltage level detection (1.25V)
- Timer watchdog
- 8 bit timer
- Power On Reset - POR
- Internal interrupt sources (timer,prescaler)
- External interrupt sources (portA)

Description

The EM6604 series is an advanced single chip, mask programmed low-power low-voltage CMOS 4-bit microcontroller. It contains ROM, RAM, timer, prescaler, watchdog timer, voltage level detector and stepper motor driver capability. Its low voltage and low power operation make it the most suitable controller for battery, stand alone and mobile equipment. The EM66XX series is manufactured using EM Microelectronic's Advanced Low Power (ALP) CMOS Process.

Typical Applications

- sensor interfaces
- domestic appliances
- security systems
- detectors
- automotive control
- clocks
- measurement equipment

Figure 1 Architecture

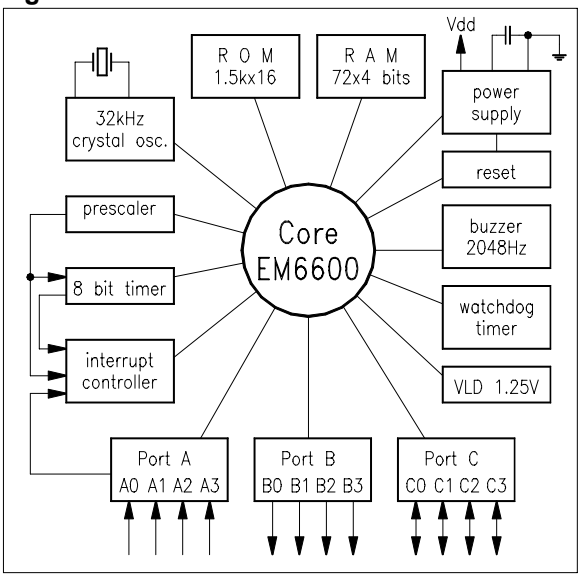
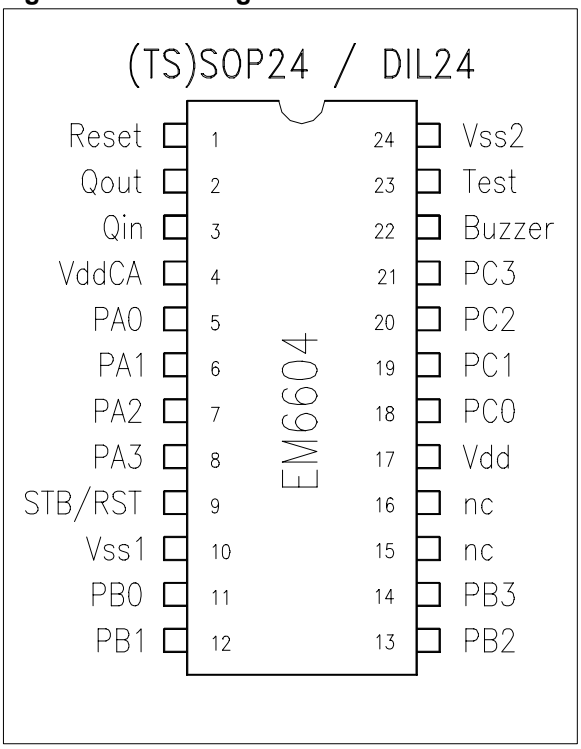


Figure 2 Pin Configuration



EM6604 at a glance

- **Power Supply**

- Low Voltage, low power architecture
- Switch between Vdd (output buffers supply) and VddCA (logic supply)
- 1.2V ... 1.7V battery voltage
- 1.7µA in active mode typ. @ 1.5V, 25°C
- 0.3µA in standby mode @ 1.5V, 25°C
- 32 kHz Oscillator

- **RAM**

- 72 x 4 bit, direct addressable

- **ROM**

- 1536 x 16 bit metal mask programmable

- **CPU**

- 4 bit RISC architecture
- 2 clock cycles per instruction
- 72 basic instructions

- **Main Operating Modes and Resets**

- Active mode (CPU is running)
- Standby mode (CPU in Halt)
- Initial reset on Power-On (POR)
- External reset pin
- Watchdog timer (time-out) reset

- **4-Bit Input PortA**

- Direct input read
- Interrupt request on input's rising or falling edge, selectable by metal mask.
- Pull-up, Pull-down or none, selectable by metal mask
- Software test variables for conditional jumps

- **4-Bit Output PortB**

- High-current output buffers
- min. 4.5mA at 0.15V voltage drop at Vdd=1.2V
- differential motor driving capability (a motor with 180 Ω between two pads of PortB is driven with at least 4.75mA

- **4-Bit Input/Output PortC**

- separate input or output selection by metal mask
- direct input read
- Pull-up, Pull-down or none, selectable by metal mask if used as Input

- **Buzzer Output**

- separate buzzer output
- 2kHz output or continuous High or Low

- **Prescaler**

- 15 stage system clock divider down to 1 Hz
- 3 interrupt requests : 2Hz/8Hz/128Hz
- Prescaler reset (from 8kHz to 1Hz)

- **8-bit Timer**

- 8-bit auto-reload count-up timer
- 4 timer clocks : 2Hz/8Hz/32Hz/256Hz
- parallel load
- interrupt request when comes to FF hex.

- **Supply Voltage Level Detector**

- Fixed level - 1.25V typical
- Busy flag during measure
- Active only on request to reduce power consumption

- **Interrupt Controller**

- 4 external interrupt sources from PortA
- 2 internal interrupt sources, prescaler and timer
- each interrupt request is individually maskable
- interrupt request flag is cleared automatically on register read
- general interrupt request to CPU can be disabled

Table of Contents

Table of Figures

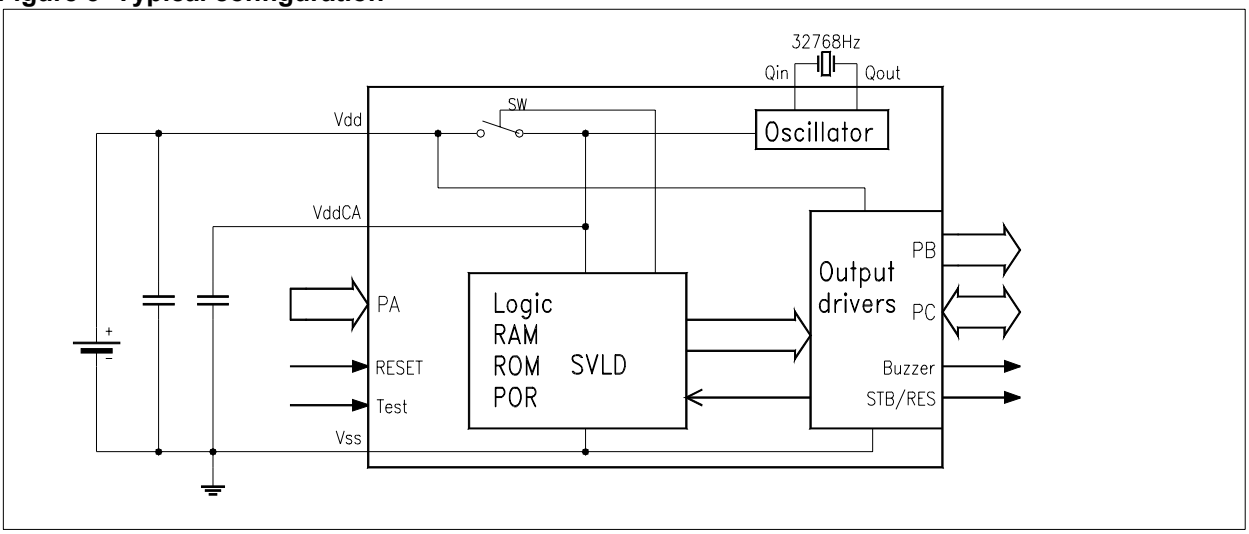
Table of Tables

Table 1. Pin Description

Pin	Pin Name	Function	Remarks
1	reset	reset input terminal	
2	Qout/ocs1	crystal terminal 1	
3	Qin/osc2	crystal terminal 2 (input)	
4	VddCA	Switched logic supply	
5	port A, 0	input 0 port A	interrupt request; tvar 1
6	port A, 1	input 1 port A	interrupt request; tvar 2
7	port A, 2	input 2 port A	interrupt request; tvar 3
8	port A, 3	input 3 port A	interrupt request
9	STB/RST	strobe/reset status output	µC reset state + port B & C write
10	Vss	negative power supply terminal	common with pin 24 (note1)
11	port B, 0	output 0 port B	High current output
12	port B, 1	output 1 port B	High current output
13	port B, 2	output 2 port B	High current output
14	port B, 3	output 3 port B	High current output
15,16	N C	not connected	
17	Vdd	positive power supply terminal	
18	port C, 0	input / output 0 port C	
19	port C, 1	input / output 1 port C	
20	port C, 2	input / output 2 port C	
21	port C, 3	input / output 3 port C	
22	Buzzer	buzzer output	
23	test	test input terminal	for EM test purpose only
24	Vss	negative power supply terminal	common with pin 10 (note1)

Note1: It is recommended that both Vss pins (10 and 24) are connected together.

Figure 3 Typical configuration



1. Operating modes

The EM6604 has a low power dissipation StandBy mode.

1.1 STANDBY Mode

Executing a HALT instruction puts the EM6604 into the StandBy mode. The voltage regulator, oscillator, Watchdog timer, interrupts and timer are operating. However, the CPU stops since the clock related to instruction execution stops, registers, RAM, and I/O pins retain their states prior to StandBy mode. StandBy is canceled by a RESET or an Interrupt request, if enabled.

Table 1.1 shows the state of the EM6604 functions mode.

Figure 4 Mode transition diagram

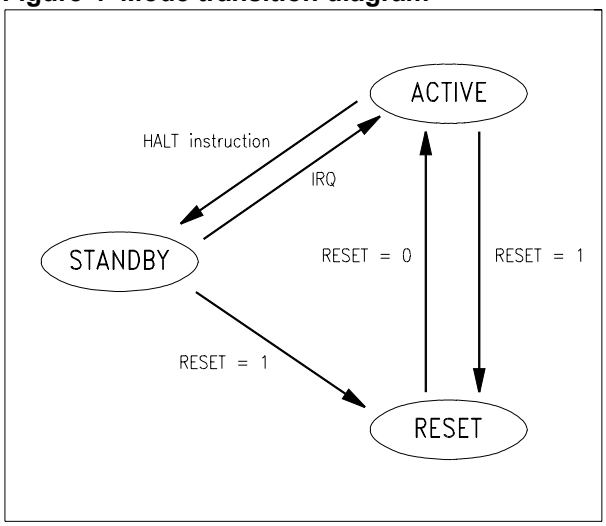


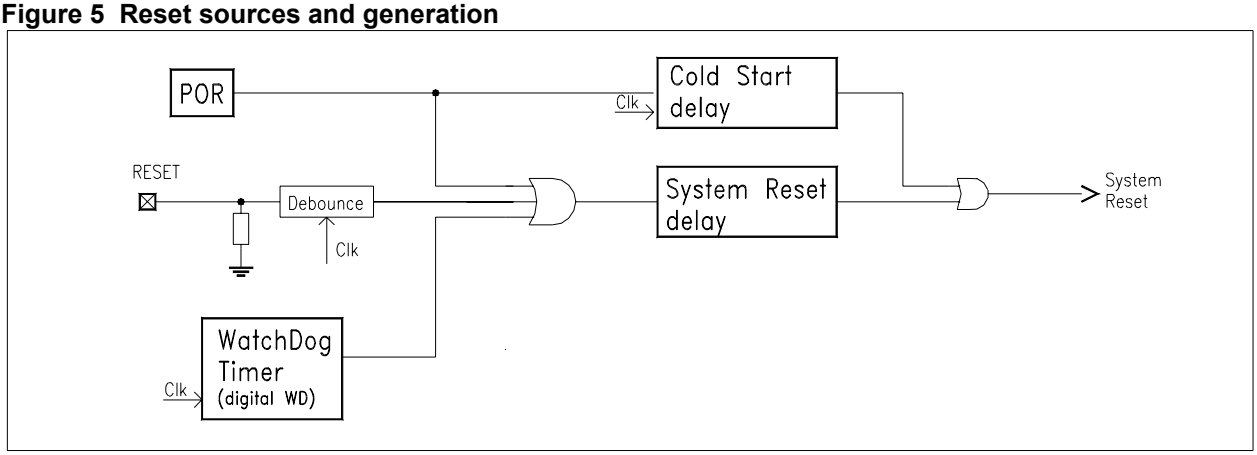
Table 1.1 STANDBY activities

FUNCTION	STANDBY
Oscillator	Active
Instruction Execution	Stopped
Registers and Flags	Retained
Interrupt Functions	Active
RAM	Retained
Timer	Active
Watchdog	Active
I/O pins	Active
Supply VLD	Stopped
Reset pin	Active

2. Power Supply

Circuit is supplied by single external power supply between VDD and VSS. Circuit reference is at VSS (ground). To overcome problems with high power output buffers when they are active, internal logic VDDCA can be switched-off from main VDD *(SW bit set to "1" in* ***SwCtr*** *register)* and is maintained by an external capacitor. High power outputs are supplied directly from main VDD.

Figure 5 Reset sources and generation



3. Reset

To initialize the EM6604, a system RESET must be executed. This can be performed in three ways:

(1) Initial RESET from the Power-On-Reset circuit.
(2) External RESET from the RESET PIN.
(3) Watchdog RESET (metal option).

During any of these RESET's the STB/RES output pin is high.

3.1 Power-On-Reset (POR) circuit

At power on, POR circuit with additional cold start delay resets the microcontroller. The cold start delay logic counts the first 32768 oscillator clocks after power-on and holds the system in RESET to guarantee oscillator stability and duty cycle. The system will consequently remain in RESET for at least one second after power up during which the STB/RES pin is driven high..

3.2 Reset Pin

During active or StandBy mode the RESET terminal has a debouncer to reject noise and therefore the signal must be active high for at least 2ms (CLK = 32kHz) .

3.3 Watchdog Timer RESET

The Watchdog Timer will generate a RESET if it is not cleared. See section 5 for details.

3.4 CPU State After RESET

RESET initializes the CPU as shown in the table 3.2 below.

Table 3.2 Initial Value After RESET

name	bits	symbol	initial value
program counter 0	12	PC0	$000 (as a result of JUMP 0)
program counter 1	12	PC1	undefined
program counter 2	12	PC2	undefined
stack pointer	2	SP	SP(0) selected
index register	7	IX	undefined
carry flag	1	CY	undefined
halt	1	HALT	0
instruction register	16	IR	JUMP 0
periphery register	4		see peripheral memory map

4. Oscillator

A built-in crystal oscillator circuit generates the system operating clock for the CPU and peripheral circuits from an externally connected crystal (typ. 32.768kHz).
EM's special design techniques guarantee the low current consumption of this oscillator. The external impedance between the pads « osc-in » and « osc-out » must be greater than 10MΩ. Connection of any other components to the two oscillator pads must be confirmed by EM Microelectronic-Marin SA.

4.1 Prescaler

The input to the prescaler is the system clock signal. The prescaler consists of a fifteen element divider chain which delivers clock signals for the peripheral circuits such as the timer, buzzer, clocked pull-up/down resistors, watchdog timer, as well as generating prescaler interrupts.
Prescaler interrupt request is generated on falling edge of the selected clock. The frequency of prescaler interrupts is software selectable, as shown in table 4.1.

Prescaler reset **PRST** resets dividers from 8kHz down to 1Hz.

Table 4.1 Prescaler interrupt source

Interrupt frequency	PSF1	PSF0
0 = no interrupt	0	0
2 Hz	0	1
8 Hz	1	0
128 Hz	1	1

Table 4.2 Prescaler control register - PRESC

Bit	Name	Reset	R/W	Description
3	-	0	R	No function , R=0
2	PRST	-	W (R=0)	Prescaler reset
1	PSF1	0	R/W	Prescaler Interrupt freq. select 1
0	PSF0	0	R/W	Prescaler Interrupt freq. select 0

*Note: The Prescaler and the Microprocessor clock's are usually non-synchronous, therefore timebases generated are max **n**, min **n-1** clock long **n** being the selected timer start value in count up mode). However the prescaler clock can be synchronized with the µP commands using the prescaler reset function).*

5. Watchdog Timer

If for any reason the CPU crashes, then the watchdog timer can detect this situation and output a system reset signal. This function can be used to detect program overrun. For normal operation the watchdog timer must be reset periodically by software at least once every three seconds (CLK = 32kHz) or a system reset signal is generated to CPU and periphery. The watchdog reset function can be de-selected with a metal option. The watchdog is active during StandBy.

In worst case, because of prescaler reset function, watchdog time-out can come down to 2 seconds.

Table 5.1 Watchdog register - WD

Bit	Name	Reset	R/W	Description
3	WDRST	-	W (R=0)	Watchdog timer reset
2	WD1	0	R	WD Timer data 1/4 Hz
1	WD0	0	R	WD Timer data 1/2 Hz
0	INTEN	0	R/W	General Interrupt mask

6. Input / Output Ports

The EM6604 has three independent 4-bit ports as shown in Table 6.0

Table 6.1 Input / Output ports Overview

port	mode	mask option	functions
PA(0:3)	input	clocked or fixed pull-up/down	input interrupt on falling/rising edge software test variable
PB(0:3)	high current output		
PC(0:3)	input or output	Input or Output clocked or fixed pull-up/down	input or output

6.1 PortA

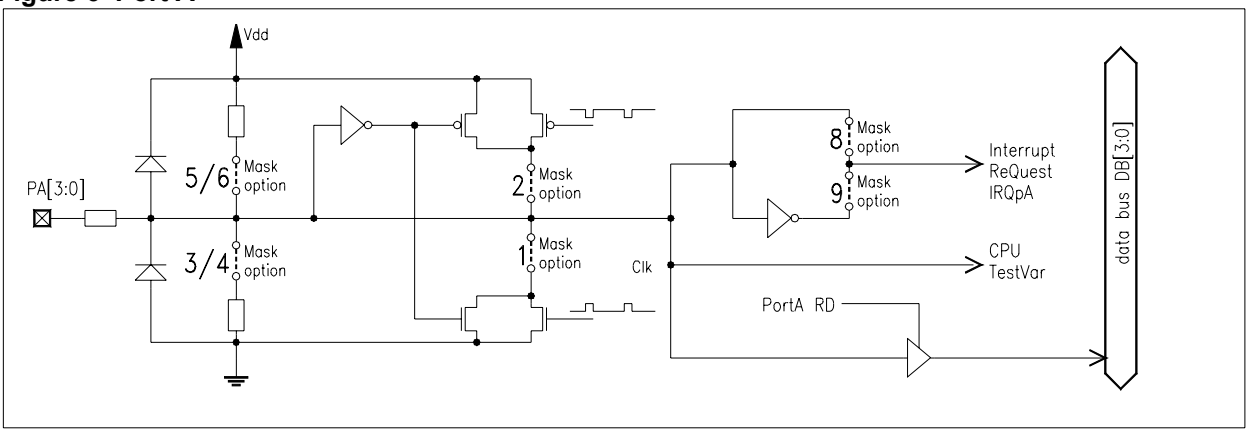
The EM6604 has one four bit general purpose input port. Each of the input port terminals PA3..PA0 has an internal pull-up/down resistor, which can be selected for each bit with mask options. Pull-up/down can be clocked R > 1MOhm or fixed R = 30 kOhm or 150 kOhm. Port information is read directly from the pin into a register.

Input PortA terminals PA0, PA1 and PA2 are also used as input conditions for conditional software branches as shown below :

PA0 is connected to CPU **TestVar1**
PA1 is connected to CPU **TestVar2**
PA2 is connected to CPU **TestVar3**

All four bits of the input port PA(0:3) can provide an interrupt, each pin with its own interrupt mask bit in the **MPortA** register.
When a falling edge (for PA3, PA2 and PA1) or a rising edge (for PA0) is detected at the input terminal, the relative interrupt request flag **IRQpa**x is set to “1“ in the interrupt request register **IRQPortA** (only if the corresponding interrupt mask is at “1“). When an interrupt occurs inspection of the **IRQPortA** and the **IntCtr** registers allows the source of the interrupt to be identified.
The **IRQPortA** register is automatically cleared by a RESET and by reading the register. At initial RESET the **MPortA** is set to 0, thus disabling any input interrupts.
See also section 9 for further details about the interrupt controller.

Figure 6 Port A



6.2 PortA Registers

Table 6.2 PortA input status register - PortA

Bit	Name	Reset	R/W	Description
3	PA3	-	R	PA3 input status
2	PA2	-	R	PA2 input status
1	PA1	-	R	PA1 input status
0	PA0	-	R	PA0 input status

Table 6.3 PortA Interrupt request register - IRQPortA

Bit	Name	Reset	R/W	Description
3	IRQpa3	0	R	input PA3 interrupt request flag
2	IRQpa2	0	R	input PA2 interrupt request flag
1	IRQpa1	0	R	input PA1 interrupt request flag
0	IRQpa0	0	R	input PA0 interrupt request flag

Table 6.4 PortA interrupt mask register - MportA

Bit	Name	Reset	R/W	Description
3	MPA3	0	R/W	interrupt mask for input PA3
2	MPA2	0	R/W	interrupt mask for input PA2
1	MPA1	0	R/W	interrupt mask for input PA1
0	MPA0	0	R/W	interrupt mask for input PA0

6.3 PortB

The EM6604 has one four bit general High-power output port which can be used to drive LEDs or stepper motors etc.... Each output can be driven high or low. Output data is written to register **PortB**.
At initial RESET the register is set to 1, thus setting the output port to high = Vdd. When not active driving outputs to high is recommended in order to reduce leakage currents.

6.4 PortB registers

Table 6.5 PortB output register - PortB

Bit	Name	Reset	R/W	Description
3	PB3	1	R/W	Output data PB3
2	PB2	1	R/W	Output data PB2
1	PB1	1	R/W	Output data PB1
0	PB0	1	R/W	Output data PB0

PB1 and PB2 can be shorted but in this case they must be driven identically.

Figure 7 Port B

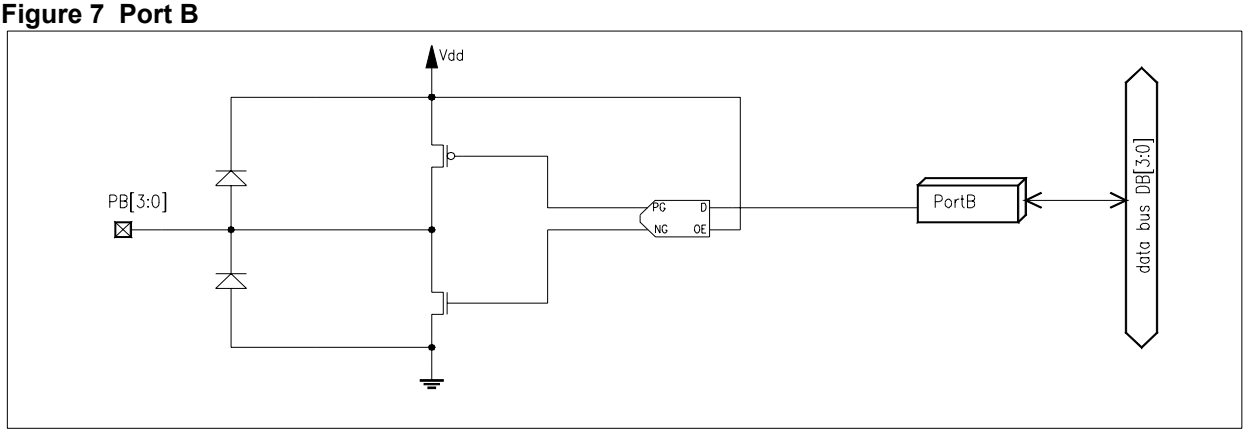
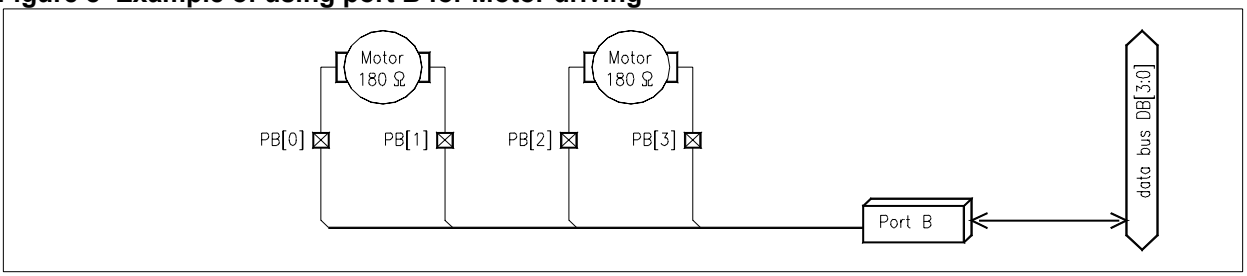


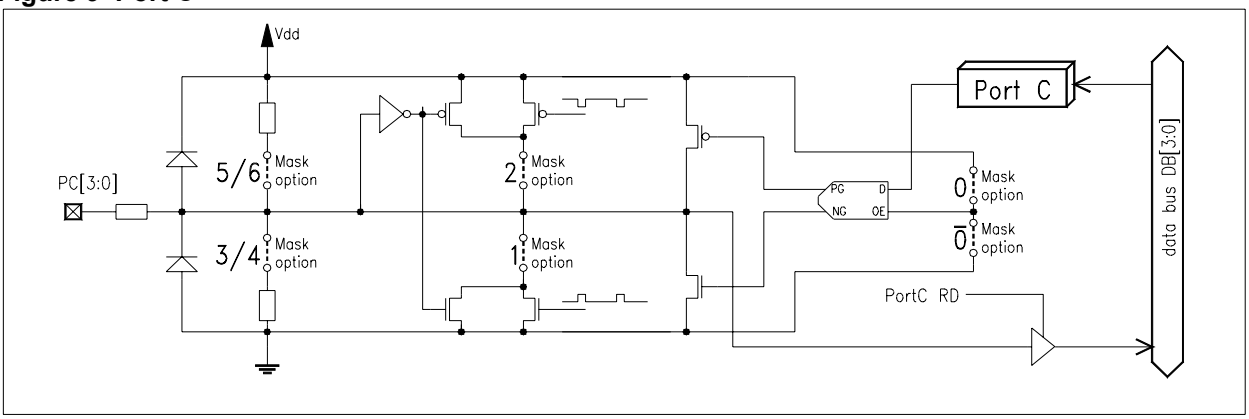
Figure 8 Example of using port B for Motor driving



6.5 PortC

The EM6604 has four individually selectable (metal option) Input/Output PC3..PC0 terminals. Each terminal can be only input or output.

Figure 9 Port C



6.6 PortC register

Table 6.6 PortC Input / Output register - PortC

Bit	Name	Reset	R/W	Description
3	PC3	-	R/W	Input/Output data PC3
2	PC2	-	R/W	Input/Output data PC2
1	PC1	-	R/W	Input/Output data PC1
0	PC0	-	R/W	Input/Output data PC0

7. Buzzer output

The EM6604 has one separate buzzer output which is controlled by the buzzer control register **BEEP** (BCF1 and BCF0 bits). Table 7.0 below shows how to select the output by writing to the **BCF1** and **BCF0** control flags in the **BEEP** register.

Table 7.1 Buzzer frequency selection

Tone frequency	BCF1	BCF0
continuous low	0	0
continuous high	0	1
1024 / 2048 Hz option	1	0
2048 Hz	1	1

7.1 Buzzer Register

Table 7.2 Buzzer control register - BEEP

Bit	Name	Reset	R/W	Description
3	-	0	R	R = 0
2	-	0	R	R = 0
1	BCF1	0	R/W	Buzzer Frequency control
0	BCF0	0	R/W	Buzzer Frequency control

8. Timer

The EM6604 has a built-in 8 bit auto-reload count-up Timer with 256Hz/32Hz/8Hz/2Hz selectable clock inputs from the prescaler. It can be enabled or disabled by writing **TimEn** in **TimCtr** register. When the timer reaches $FF it generates an interrupt request and the flag **TimIRQ** is set. If the timer interrupt is enabled by setting the mask flag **MTimC** set to 1, then an interrupt request is generated to the CPU. See also section 9.

The timer clock input is selected in the timer control register **TimCtr** (TEC1 and TEC0 bits).

At any time during the count-up process, the timer can be initialized to the data written in the load timer registers **LTimLS** (low four bits) and **HTimLS** (high four bits). It starts to count up with the first rising edge of the selected timer clock input after the new **LTimLS** value was written (the low four bits writing operation causes the parallel load of the timer). To load the timer, it is important to first write **TimCtr** register or **HTimLS** and then **LTimLS.** During count up, the timer can always be loaded with a new value, but the high four bits will be accepted only during the write of the low four bits.

If the auto reload function is selected in **TimCtr** register (**TimAuto** bit), the timer is automatically reloaded with the value contained in **LTimLS** and **HTimLS** when it reaches value $FF. Reload is made on the next rising 8kHz clock and is active during half a period of this 8kHz clock. **TimAuto** bit's value is internally taken into account only during low four bits timer load operation (writing **TimAuto** to 1 does not start the timer counting up with the last value in the timer load registers but it waits until a new **LTimLS** load). The timer counting to $FF generates a timer interrupt event **TimIRQ** and reloads the registers before starting to count up again.

To stop the timer at any time, a write of $FF is made to the timer load registers, this sets the **TimAuto** flag to 0. If the timer is stopped by writing the **TimEn** bit to 0, the timer status can be read. The currenttimer status can be always obtained by reading the timer registers **LTimLS** and **HTimLS**. For proper operation read ordering should be respected such that the first read should be of the **LTimLS** register followed by the **HTimLS** register (which was stored on reading **LTimLS**).

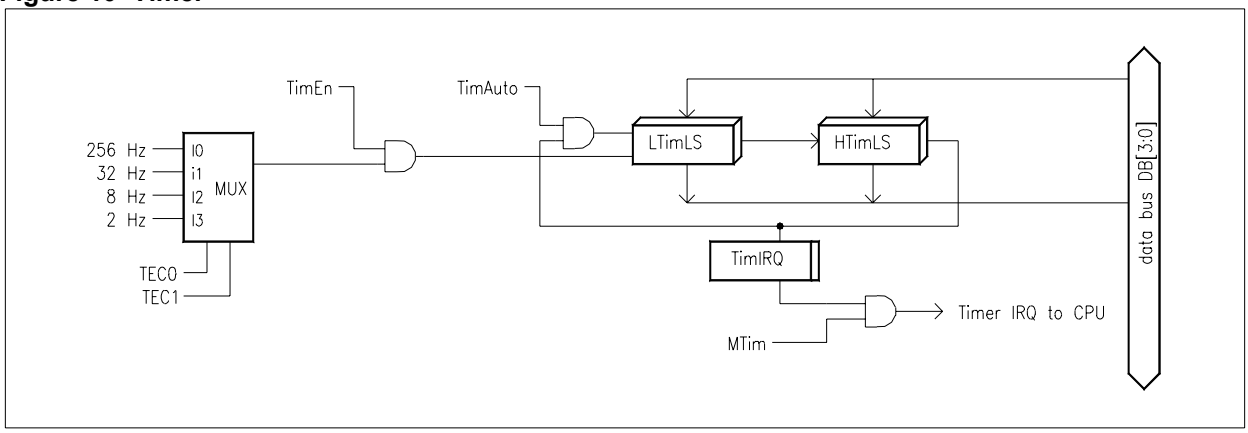
Table 8.1 shows the selection of inputs to the timer.

Table 8.1 Timer clock selection

TEC1	TEC0	Timer clock input
0	0	256 Hz
0	1	32 Hz
1	0	8 Hz
1	1	2 Hz

At initial reset, the timer is disabled, the auto-reload function is not active and the timer input clock is 256Hz.

Figure 10 Timer



8.1 Timer registers

Table 8.2 Timer control register - TimCtr

Bit	Name	Reset	R/W	Description
3	TimAuto	0	R/W	Timer AUTO reload
2	TimEn	0	R/W	Timer enable - active high
1	TEC1	0	R/W	Timer Clock selection 1
0	TEC0	0	R/W	Timer Clock selection 0

Table 8.3 LOW Timer Load/Status register - LTimLS (4 low bits)

Bit	Name	Reset	R/W	Description
3	TL3/TS3	0	R/W	Timer load/status bit 3
2	TL2/TS2	0	R/W	Timer load/status bit 2
1	TL1/TS1	0	R/W	Timer load/status bit 1
0	TL0/TS0	0	R/W	Timer load/status bit 0

Table 8.4 HIGH Timer Load/Status register - HTimLS (4 high bits)

Bit	Name	Reset	R/W	Description
3	TL7/TS7	0	R/W	Timer load/status bit 7
2	TL6/TS6	0	R/W	Timer load/status bit 6
1	TL5/TS5	0	R/W	Timer load/status bit 5
0	TL4/TS4	0	R/W	Timer load/status bit 4

9. Interrupt controller

There are two internal and four external interrupt sources in EM6604 :

1) prescaler interrupt at 128Hz, 8Hz or 2Hz
2) timer interrupt when value changes from $FE to $FF
3) portA interrupt on falling edge (for PA3, PA2 and PA1) and rising edge (for PA0)

A general interrupt mask is defined in the watchdog control register **WD** (**INTEN** bit).

9.1 Internal interrupt sources

The interrupt request flags and relative interrupt masks are defined in the interrupt control register **INTctr** (**PrscIRQ** and **Mprsc** bits for the prescaler - **TimIRQ** and **Mtim** bits for the timer).

An interrupt mask set to “1“ allows CPU interrupt.
An interrupt request flag may be set to “1“ even if the relative interrupt mask is at “0“ ; but in this case, the CPU will not be interrupted.
Interrupt request flags are cleared after **INTctr** reading operation. At initial reset, interrupt requests are disabled.

Figure 11 Interrupt sources and generation

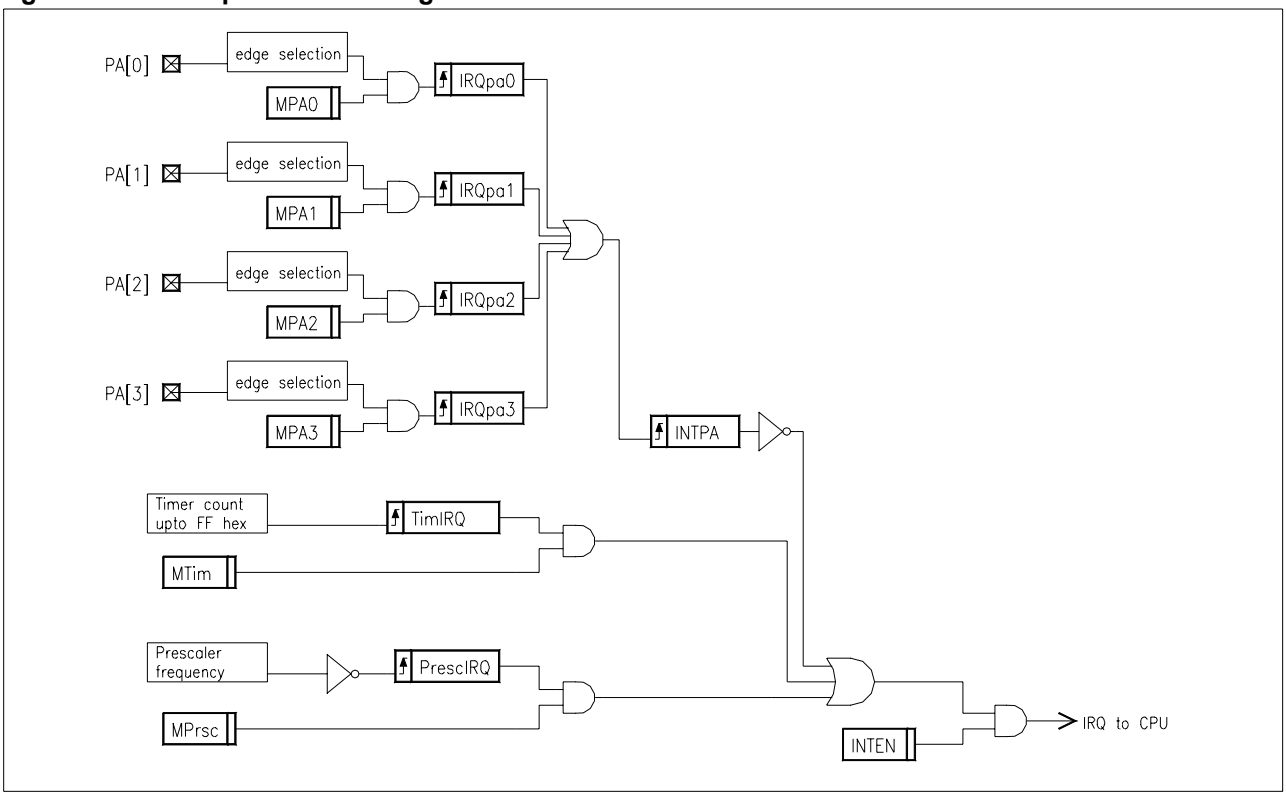


Table 9.1 Interrupt control register INTctr

Bit	Name	Reset	R/W	Description
3	PrscIRQ	0	R	Prescaler Interrupt ReQuest
2	Mprsc	0	R/W	Prescaler Interrupt mask
1	TimIRQ	0	R	Timer Interrupt ReQuest
0	Mtim	0	R/W	Timer Interrupt mask

9.2 External interrupt sources : see PortA description

10. Supply Voltage Level Detector

SVLD detects if the supply voltage is lower/higher than 1,25V. It can be enabled or disabled by writing **SLVDst** bit in **SLVD** register.

The measurement period lasts 1,923 ms (= 2 * 1024 Hz clock period), and the busy flag is cleared when measurement is finished to indicate a valid result.
SVLDres bit at “0“ means that power supply level is higher than 1,25V.
SVLDres bit at “1“ means that power supply level is lower than 1,25V. The result **SVLDres** of the last measurement remains until the new one is started. The start of a new SVLD measurement resets the result of the previous one (SVLDres => 0).
When SVLD is activated power consumption increases by approximately 3µA.

Table 10.1 SVLD control register - SVLD

Bit	Name	Reset	R/W	Description
3	SVLDres	0	R	SVLD result (0=higher 1=lower)
2	busy	0	R	measurement in progress
1	-	0	R=0	-
0	SVLDst	0	W/R=0	SVLD start measurement

11. STroBe/RESet

The STB/RES output pin is used to indicate:
1.) The EM6604 write operations to ports B and C. For a PortB and PortC write operation the STROBE signal goes high for half of the system clock period. Write is effected on falling edge of the strobe signal and it can this be used to indicate when data changes at the output port pins.
2.) Any microcontroller EM6604 reset condition. Additionally, any EM6604 internal RESET condition is indicated by a continuous high level on STB/RES for the period of the RESET.

12. Test at EM - Active Supply Current test

For this purpose, five instructions at the end of the ROM will be added.

```
Testloop:   STI     00H, 0AH
            LDR     1BH
            NXORX
            JPZ     Testloop
            JMP     00H
```

To stay in the testloop, these values must be written in the corresponding addresses before jumping in the loop:

```
1BH:    0101b
32H:    1010b
6EH:    0010b
6FH:    0011b
```

Free space after last instruction: JMP 00H (0000)

Remark: empty space within the program are filled with NOP (FOFF).

13. EM6604 Metal Mask Options

The following options can be selected at the time of programming the metal mask ROM.
To select an option put a cross - **X.**

Table 13.1 Input / Output ports option

		Output	Clocked Pull-Down R > 1MΩ	Clocked Pull-Up R > 1MΩ	Pull-Down R = 30kΩ	Pull-Down R = 150kΩ	Pull-Up R = 30kΩ	Pull-Up R = 150kΩ	No Input Pull-Up or Pull-Down
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
A0	**PA0 input**		Pa0opt1	Pa0opt2	Pa0opt3	Pa0opt4	Pa0opt5	Pa0opt6	Pa0opt7
A1	**PA1 input**		Pa1opt1	Pa1opt2	Pa1opt3	Pa1opt4	Pa1opt5	Pa1opt6	Pa1opt7
A2	**PA2 input**		Pa2opt1	Pa2opt2	Pa2opt3	Pa2opt4	Pa2opt5	Pa2opt6	Pa2opt7
A3	**PA3 input**		Pa3opt1	Pa3opt2	Pa3opt3	Pa3opt4	Pa3opt5	Pa3opt6	Pa3opt7
C0	**PC0 In/Out**	Pc0opt0	Pc0opt1	Pc0opt2	Pc0opt3	Pc0opt4	Pc0opt5	Pc0opt6	Pc0opt7
C1	**PC1 In/Out**	Pc1opt0	Pc1opt1	Pc1opt2	Pc1opt3	Pc1opt4	Pc1opt5	Pc1opt6	Pc1opt7
C2	**PC2 In/Out**	Pc2opt0	Pc2opt1	Pc2opt2	Pc2opt3	Pc2opt4	Pc2opt5	Pc2opt6	Pc2opt7
C3	**PC3 In/Out**	Pc3opt0	Pc3opt1	Pc3opt2	Pc3opt3	Pc3opt4	Pc3opt5	Pc3opt6	Pc3opt7

(ONE option in each line MUST be selected)

Table 13.2 PortA interrupt edge option

		Interrupt on Input's rising edge	Interrupt on Input's falling edge
		8	**9**
I0	**PA0 - IRQ**	IrqPa0_R	IrqPa0_F
I1	**PA1 - IRQ**	IrqPa1_R	IrqPa1_F
I2	**PA2 - IRQ**	IrqPa2_R	IrqPa2_F
I3	**PA3 - IRQ**	IrqPa3_R	IrqPa3_F

If not used the default is falling edge. However, an interrupt will not be generated if the corresponding bit in this register **MPortA** is 0. (ONE option in each line MUST be selected)

Table 13.3 Watchdog timer metal option

		Watch-Dog timer ACTIVE	Watch-Dog timer INACTIVE
W0	**WD timer**	Wd_yes	Wd_no

(ONE option MUST be selected)

Table 13.4 Buzzer 1024 / 2048 Hz option when BCF1,BCF0 = 10

		Buzzer freq. of 1k (and 2k)	Buzzer freq. of 2k only
B1	**Buzzer**	Buz_1k_2k	Buz_2k

(ONE option MUST be selected)

The customer should specify the required options at the time of ordering.
A copy of this sheet, as well as the « Software ROM characteristic file » generated by the assembler (*.STA) should be attached to the order.

14. PERIPHERAL MEMORY MAP

The following table shows the peripheral memory map of the EM6604. The address space is between $00 and $7F (Hex). Any addresses not shown can be considered to be reserved.

Register name	add hex	add dec	reset value	write_bits	read_bits	Remarks
			b'3210	Read/Write_bits		
RAM	00- 47	0-71	xxxx	0: D0 1: D1 2: D2 3: D3		direct addressing
SwCtr	6B	107	xxx0	0: SW 1: - 2: - 3: -		Supply switch control
SVLD	6C	108	0000	0: SVLDst 1: - 2: - 3: -	0: 0 1: 0 2: busy 3: SVLDres	voltage level detector control
Index LOW	*6E*	*110*	*xxxx*			*internally used for INDEX register*
Index HIGH	*6F*	*111*	*xxxx*			*internally used for INDEX register*
LTimLS	70	112	1111	0: TL0 1: TL1 2: TL2 3: TL3	0: TS0 1: TS1 2: TS2 3: TS3	low nibble of 8bit timer load and status register
HTimLS	71	113	1111	0: TL4 1: TL5 2: TL6 3: TL7	0: TS4 1: TS5 2: TS6 3: TS7	high nibble of 8bit timer load and status register
TimCtr	72	114	0000	0: TEC0 1: TEC1 2: TimEn 3:TimAuto		timer control register with frequency selector
WD	73	115	0000	0: INTEN 1: - 2: - 3: WDrst	0: INTEN 1: WD0 2: WD1 3: 0	global interrupt enable watchdog timer control
PRESC	74	116	0000	0: PSF0 1: PSF1 2: PRST 3: -	0: PSF0 1: PSF1 2: 0 3: 0	Prescaler control
PortA	75	117	xxxx		0: PA0 1: PA1 2: PA2 3: PA3	Port A status
MPortA	76	118	0000	0: MPA0 1: MPA1 2: MPA2 3: MPA3		Port A mask

Register name	add hex	add dec	reset value	write_bits	read_bits	Remarks
			b'3210	Read/Write_bits		
IRQportA	77	119	0000		0: IRQpa0 1: IRQpa1 2: IRQpa2 3: IRQpa3	Port A interrupt request
PortB	78	120	1111	0: PB0 1: PB1 2: PB2 3: PB3		Port B Output
PortC	7A	122	xxxx	0: PC0 1: PC1 2: PC2 3: PC3		Port C Input/Output data
INTctr	7D	125	0000	0: MTim 1: - 2: MPrsc 3: -	0: MTim 1: TimIRQ 2: MPrsc 3: PrescIRQ	prescaler and timer interrupt mask and request
BEEP	7E	126	0000	0: BCF0 1: BCF1 2: - 3: -		Buzzer control
RegTestEM	*7F*	*127*	----	----	----	*reserved*

15. Electrical specifications

15.1 Absolute maximum ratings

	Min.	Max.	Units
Power supply VDD-VSS	- 0.2	+ 3.6	V
Input voltage	VSS - 0.2	VDD+0.2	V
Storage temperature	- 40	+ 125	°C
Electrostatic discharge to MIL-STD-883C method 3015	-2000	+2000	V
Maximum soldering conditions		10s x 250°C	

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified electrical characteristics may affect device reliability or cause malfunction.

15.2: Standard Operating Conditions

Parameter	Value	Description
Temperature	-20°C...+65°C	
VDD	+1.2 ...+1.70V	
VSS	0 V (reference)	
CVDDCA	min. 100nF (note1)	switched logic supply capacitor
fq	32768 Hz	nominal frequency
Rqs	35 kOhm	typical quartz serial resistor
CL	8.2pF	typical quartz load capacitance
df/f	+/- 30 ppm	quartz frequency tolerance

Note1: This capacitor maintains the Supply to the core when the core has been isolated by the internal Supply switch during driving the high current outputs. The user should be aware that the selection of this capacitor will dictate the time that the core can be isolated.

15.3 Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions should be taken as for any other CMOS component.
Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range.

15.4: DC characteristics - Power Supply Pins

Vdd=1.5V, T=25°C (unless otherwise specified)

Parameter	Conditions	Symb.	Min.	Typ.	Max.	Unit
ACTIVE Supply Current	+25°C (note2)	**I**VDDa		1.7	5.0	µA
ACTIVE Supply Current (in active mode)	(note2) (note3) -20°C...+65°C	**I**VDDa			15.0	µA
STANDBY Supply Current	+25°C	**I**VDDh		0.3	0.6	µA
STANDBY Supply Current (in Halt mode)	(note3) -20°C...+65°C	**I**VDDh			10.0	µA
RAM data retention		Vrd	1.1			V
Resistor Of VDDCA switch f(**I**VDD)	VDD=1.3V VDDCA=1.5V	**R**doff **R**don	300	450	2000	kOhm Ohm
POR voltage	-20..+65 °C	**V**POR		0.7	1.05	V
SVLD voltage		**V**SVLD	1.10	1.25	1.38	V

Note2: test loop with successive writing and reading of two different addresses with an inverted values (five instructions should be reserved for this measurement),
Note3: NOT tested if delivered in chip form.

15.5: DC characteristics - Input/Output Pins

Vdd=1.5V, -20°C<T< +65°C, (unless otherwise specified)

Parameter	Conditions	Symb.	Min.	Typ.	Max.	Unit
Input Low voltage						
I/O ports +	Pin at hi-impedance	**V**IL	Vss		0.3VDD	V
TEST			Vss		0.3VDD	V
Reset			Vss		0.3VDD	V
Qin			Vss		0.1VDD	V
Input High voltage						
I/O ports A,C	Pin at hi-impedance	**V**IH	0.7VDD		VDD	V
TEST			0.7VDD		VDD	V
Reset			0.7VDD		VDD	V
Qin			0.9VDD		VDD	V
High Current Outputs	RL01 = RL23 = 180 Ohm					
Output port B	VDD=1.2V	**I**RL	+/- 4.75			mA
(Differential current between	VDD=1.5V	**I**RL		+/- 6.7		mA
two outputs)	VDD=1.7V	**I**RL		+/- 7.7		mA
Output Low Current						
Port B	VOL = 0.15V, VDD = 1.2V	**I**OL	4.5	7.0		mA
Output Low Current						
PortC, Buzzer, STB/RST	VOL = 0.3V, VDD = 1.2V	**I**OL	500	700		µA
Output Low Current						
PortC, Buzzer, STB/RST	VOL = 0.3V, VDD = 1.5V	**I**OL		700		µA
Output High Current						
Port B	VOH = 1.05V, VDD=1.2V	**I**OH	3.0	5.0		mA
Output High Current						
PortC, Buzzer, STB/RST	VOH = 0.9V, VDD=1.2V	**I**OH	250	450		µA
Output High Current						
PortC, Buzzer, STB/RST	VOH = 1.2V, VDD=1.5V	**I**OH		600		µA

Input CLK'd Pull-up/down (if selected) on PortA and PortC

Vdd=1.5V, -20°C<T< +65°C, (unless otherwise specified)

Parameter	Conditions	Symb.	Min.	Typ.	Max.	Unit
pull-up/down active time		**t**pd		61		µs
frequency of CLK'd Pull		**f**pd		128		Hz
Input CLK'd Pull-down	Input at VDD					
input current (PA0..PC3)	option 1	**IOH**lp			5	µA
average input current	Input at VDD	**IOH**la			40	nA
peak current	tmax=2 µs	**Ipd**max			300	µA
Input CLK'd Pull-up	Input at VSS					
input current (PA0..PC3)	option 2	**IOL**lp			5	µA
average input current	Input at VSS	**IOL**la			40	nA
peak current	tmax=2 µs	**Ipu**max			300	µA

Input static Pull-up/down (if selected) on PortA and PortC, Test, Reset

Vdd=1.5V, -20°C<T< +65°C, (unless otherwise specified)

Parameter	Conditions	Symb.	Min.	Typ.	Max.	Unit
Input static Pull-down	Input at VDD					
I/O ports A,C	30 kOhm option	**R**in	12	30	60	kOhm
I/O ports A,C	150 kOhm option	**R**in	60	150	300	kOhm
TEST		**R**in	8	20	50	kOhm
Reset		**R**in	50	100	250	kOhm
Input static Pull-up	Input at VSS					
I/O ports A,C	30 kOhm option	**R**in	12	30	60	kOhm
I/O ports A,C	150 kOhm option	**R**in	60	150	300	kOhm

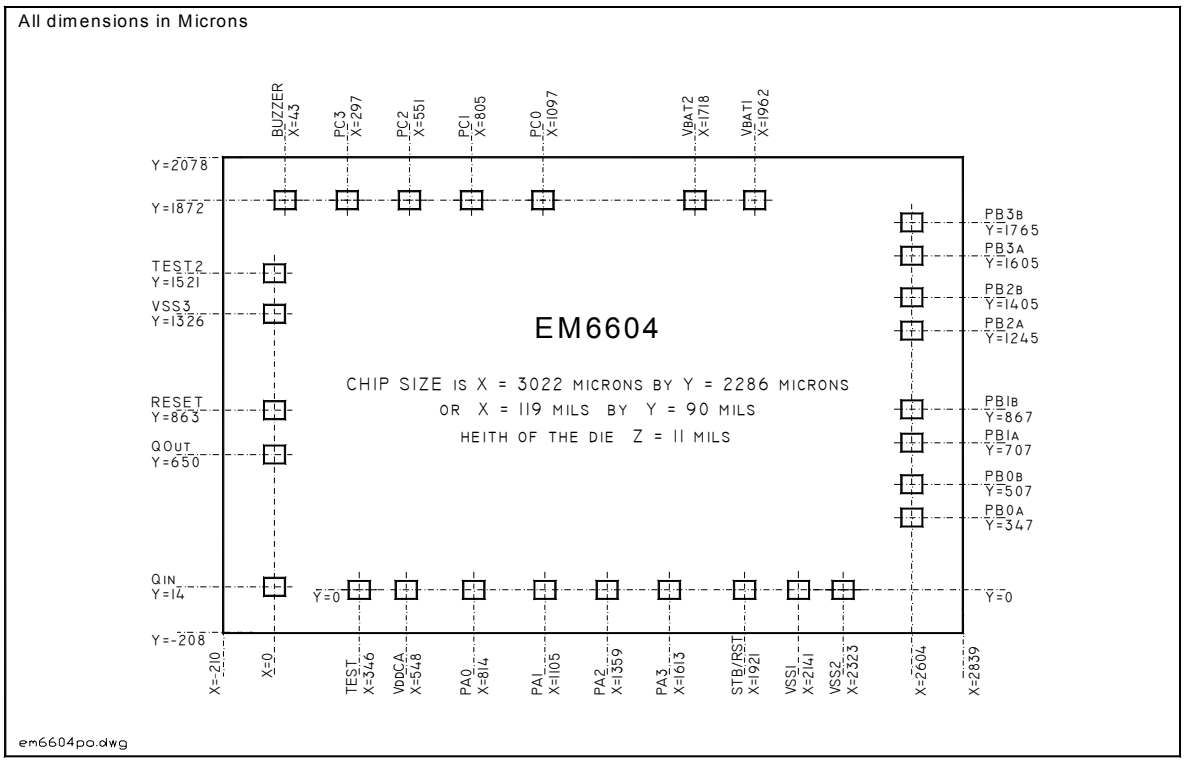
15.6 Oscillator

1.2V<Vdd<1.7V, T= +25°C, (unless otherwise specified)

Parameter	Conditions	Symb.	Min.	Typ.	Max.	Unit
Temperature stability	15 - 35 °C	Df / f * DT			0.3	ppm/°C
Voltage stability	1.4 - 1.6 V	Df /f * DU			5	ppm/V
Input capacitor	Ref Vss	CQin	5.6	7	8.4	pF
Output capacitor	Ref Vss	CQout	12.0	14	15.9	pF
Start voltage	Tstart < 10 s	Ustart	1.2			V
Oscillator start time		tdosc		1	9	s
System start time (oscillator+cold start+reset)		tdsys		2	10	s
CQin external (note4)					5.6	pF

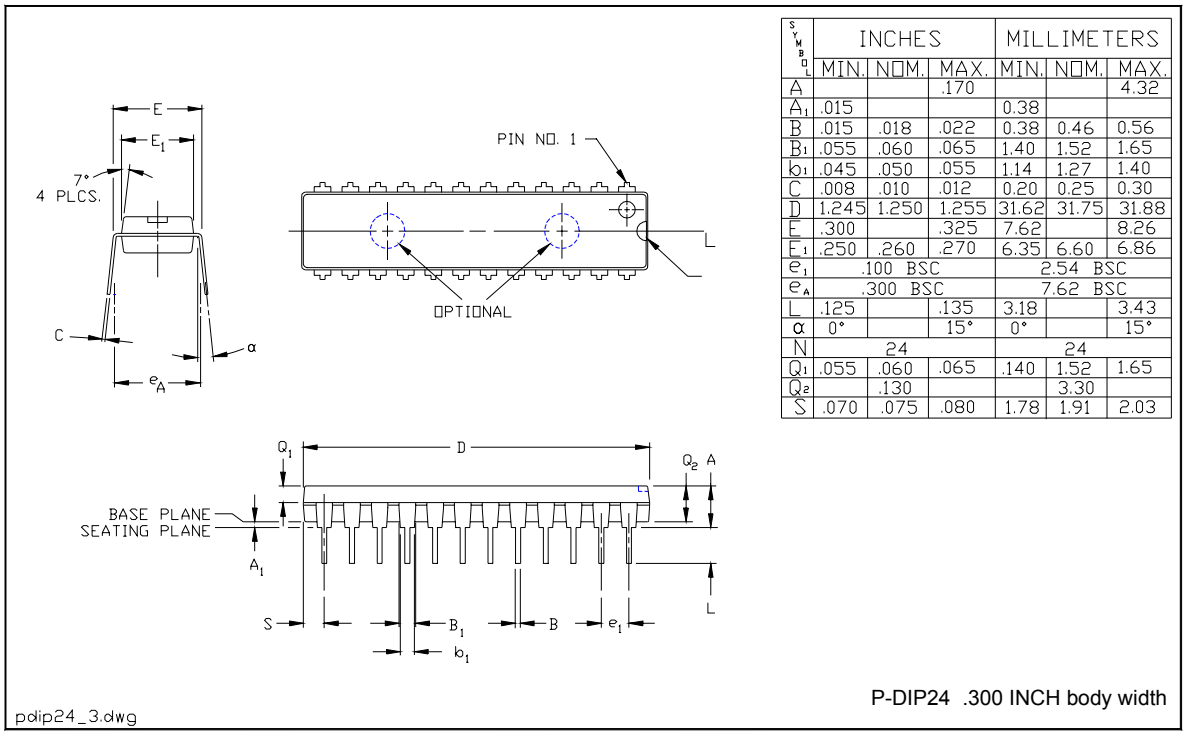
Note4: Oscillator frequency can be trimmed with an external capacitance **CQin** between Qin and Vss.

16. Pad Location Diagram



17. Package and Ordering Information

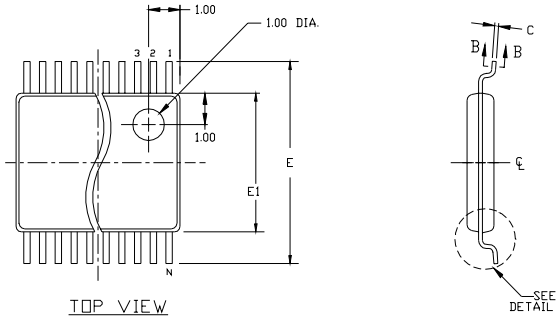
Dimensions of PDIP24 Package



SYMBOL	INCHES			MILLIMETERS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			.170			4.32
A_1	.015			0.38		
B	.015	.018	.022	0.38	0.46	0.56
B_1	.055	.060	.065	1.40	1.52	1.65
b_1	.045	.050	.055	1.14	1.27	1.40
C	.008	.010	.012	0.20	0.25	0.30
D	1.245	1.250	1.255	31.62	31.75	31.88
E	.300		.325	7.62		8.26
E_1	.250	.260	.270	6.35	6.60	6.86
e_1	.100 BSC			2.54 BSC		
e_A	.300 BSC			7.62 BSC		
L	.125		.135	3.18		3.43
α	0°		15°	0°		15°
N	24			24		
Q_1	.055	.060	.065	.140	1.52	1.65
Q_2		.130			3.30	
S	.070	.075	.080	1.78	1.91	2.03

P-DIP24 .300 INCH body width

Dimensions of TSSOP24 Package

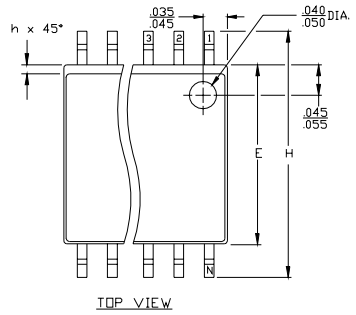


SYMBOL	DIMENSIONS in MILLIMETERS		
	MIN.	NOM.	MAX.
A	——	——	1.10
A_1	0.05	——	0.15
A_2	0.85	0.90	0.95
b	0.19	–	0.30
b1	0.19	0.22	0.25
c	0.09	–	0.20
D	7.80 BSC		
E1	4.30	4.40	4.50
e	0.65 BSC		
E	6.40 BSC		
L	0.50	0.60	0.70
θ	0°	——	8°

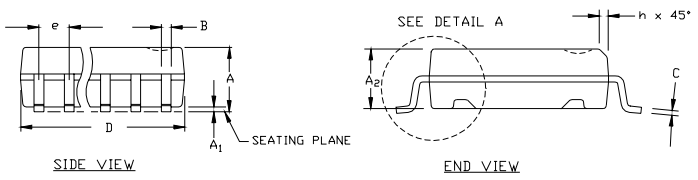
tssop-24.dwg

TSSOP24 (0.65mm pitch, 4.4mm body width)

Dimensions of SOP24 Package



SYMBOL	DIMENSIONS in INCHES			DIMENSIONS in MILLIMETERS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	.097	.101	.104	2.46	2.56	2.64
A_1	.0050	.009	.0115	0.127	0.22	0.29
A_2	.090	.092	.094	2.29	2.34	2.39
B	.014	.016	.019	0.35	0.41	0.48
C	.0091	.010	.0125	0.23	0.25	0.32
D	.602	.607	.612	15.29	15.42	15.54
E	.292	.296	.299	7.42	7.52	7.59
e	.050 BSC			1.27 BSC		
H	.400	.406	.410	10.16	10.31	10.41
h	.010	.013	.016	0.25	0.33	0.41
L	.024	.032	.040	0.61	0.81	1.02
N	24			24		
θ	0°	5°	8°	0°	5°	8°



Sop-24.dwg

SOP-24(1.27mm pitch, 300mils body width)

17.1 Ordering *Information*

Packaged Device:

EM6604 %%% SO24 B

Customer Version:
customer-specific number
given by EM Microelectronic

Package:
SO24 = 24 pin SOIC
TP24 = 24 pin TSSOP
DL24 = 24 pin DIP (note 1)

Delivery Form:
A = Stick
B = Tape&Reel (for SO24 and TP24 only)

Device in DIE Form:

EM6604 %%% WS 11

Customer Version:
customer-specific number
given by EM Microelectronic

Die form:
WW = Wafer
WS = Sawn Wafer/Frame
WP = Waffle Pack

Thickness:
11 = 11 mils (280um), by default
27 = 27 mils (686um), not backlapped
(for other thickness, contact EM)

Note 1: Please contact EM Microelectronic-Marin S.A. for availability of DIP package.

Ordering Part Number (selected examples)

Part Number	Package/Die Form	Delivery Form/Thickness
EM6604%%%SO24A	24 pin SOIC	Stick
EM6604%%%SO24B	24 pin SOIC	Tape&Reel
EM6604%%%TP24B	24 pin TSSOP	Tape&Reel
EM6604%%%WS11	Sawn wafer	11 mils
EM6604%%%WP11	Die in waffle pack	11 mils
EM6604%%%WW27	Unsawn wafer	27 mils

Please make sure to give the complete Part Number when ordering, including the 3-digit version. The version is made of 3 digits %%%: the first one is a letter and the last two are numbers, e.g. P01 , P12, etc.

17.2 Package *Marking*

DIP and SOIC marking:

First line:	E	M	6	6	0	4		0	%	%	Y
Second line:	P	P	P	P	P	P	P	P	P	P	P
Third line:	C	C	C	C	C	C	C	C	C	C	C

TSSOP marking:

E	M	6	6	0	4	%	%
P	P	P	P	P	P	P	P
		C	C	C	C	Y	P

Where: %% = last two-digits of the customer-specific number given by EM (e.g. 05, 12, etc.)
Y = Year of assembly
PP…P = Production identification (date & lot number) of EM Microelectronic
CC…C = Customer specific package marking on third line, selected by customer

17.3 Customer Marking

There are **11** digits available for customer marking on **DIP24** and **SO24**.
There are **4** digits available for customer marking on **TSSOP24**.

Please specify below the desired customer marking.

Changed on Jan. 6th 1999

Table of contents/ Figures / Tables (page 3)

Table 6.4 PortB … -> Table 6.5 PortB … (page 9)

SVLDres bit at "1" means that power supply level is lower than 1,25V. The result **SVLDres** of the last measurement remains until the new one is started. The start of a new SVLD measurement resets the result of the previous one (SVLDres => 0). (page 14)

Updates since Rev C/401 (november 01)

Date of Update Name	Chapter concerned	New Version	Changes
01.11.01	All	11/01 C/401	Change Header & footer, Add URL mention
22.03.02	17 & 18	D/440	Change pad loc. Diagram ordering information