EM78862C

8-Bit Microcontroller

Product Specification

DOC. VERSION 2.1

ELAN MICROELECTRONICS CORP.

July 2005

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Contents

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial version	Nov-16-2004
1.1	■ To match with EM78808: 1. Modified the LCD RAM address block diagram. 2. Renamed the SEGMENT pins. ■ LCD Driver circuit Added one pin/pad for the voltage converter capacitor.	Nov-23-2004
1.2	■ Changed the LCD RAM address: 30h~3Fh → 20h~2Fh, B0h~BFh → A0h~Afh. ■ Cancelled all functions of Port B and Port C. ■ Added LCD segment from Seg32 to Seg47. ■ Modified the Pin pad sequence. ■ Added Port 7 (INT) wakeup function from sleep mode.	Dec-20-2004
1.3	■ DC Electrical Characteristic → LCD Driver Voltage: 1. Ilcd=0μA , 4.5V →1.5VDD 2. Ilcd=-150μA , 4.4V →1.47VDD	Dec-21-2004
1.4	■ Modified the VDD range: 2.2 ~ 5.5V → 2.2~3.6V	Dec-23-2004
1.5	■ Modified the pin pad sequence ■ Cancelled the IOC REGISTER: IOC5 PAGE 1 (LCD bias control)	Jan-12-2005
1.6	■ Added Counters 1 & 2 Wake-up function	Jan-14-2005
1.7	■ Modified the pin pad sequence ■ Application notes → Look-up table issue ■ TBL instruction action→ R2+1, R2+A	Feb-04-2005
1.8	■ Deleted the information on IOC6 Register ■ Added Application Note on the proper use of the Reset register ■ Provided separate registers info for ICE-808 & EM788862C	Mar-02-2005
1.9	■ Revised the Operation Register RE real chip initial value 1. RE Page 0 Bit 4 fixed → flexible 2. RE Page 1 Bit 7…0 →1	Mar-08-2005
2.0	■ Added Bonding Coordinates Subsidiary	Apr-14-2005
2.1	■ Modified the DC Electrical Characteristics 1. Modified the VOH, VOL condition value. 2. Added LCD enable/disable of IDLE mode current value.	Jul-13-2005

1 General Description

The EM78862C is an 8-bit RISC type microprocessor with low power, high speed CMOS technology. Integrated into the single chip are built-in watchdog (WDT), RAM, ROM, programmable real-time clock/counter, internal interrupt, power-down mode, LCD driver, and bi-directional I/O. The EM78862C provides a single chip solution for scientific calculator design applications.

2 Features

2.1 CPU

- Operating voltage range: 2.2V ~ 3.6V
- 16K x 13 on-chip ROM
- 1.25K x 8 on-chip RAM
- 144 byte working register
- Up to 24 bi-directional I/O ports (16 shared with LCD segment pins)
- 8 level stack for subroutine nesting
- 8-bit real time clock/counter (TCC) can be configured as interrupt sources with prescaler
- Two sets of 8 bit counters are set as interrupt sources with prescaler
- Programmable free running on-chip watchdog timer
- Four modes (internal PLL clock 3.579MHz)
  - SLEEP Mode:CPU and 3.579MHz clock turn off, 32.768kHz clock turn off
  - IDLE Mode:CPU and 3.579MHz clock turn off, 32.768kHz clock turn on
  - GREEN Mode: 3.579MHz clock turn off, CPU and 32.768kHz clock turn on
  - NORMAL Mode:3.579MHz clock turn on, CPU and 32.768kHz clock turn on
- Input port wake up function
- Six interrupt sources: three internal, three external
  - Internal:
    1. TCIF for TCC timer overflow interrupt
    2. CNT1 for COUNTER 1 overflow interrupt
    3. CNT2 for COUNTER 2 overflow interrupt
  - External:
    1. INT 0 for Port 70, Port 71, Port 72, or Port 73, has a falling edge trigger interrupt
    2. INT 1 for Port 74, Port 75, or Port 76, has a falling edge trigger interrupt
    3. INT 3 for Port 77 has a rising edge or falling edge trigger (by CONT register) interrupt
- 67-pin die chip (EM78862CH)
- Port key scan function
- Clock frequency 32.768kHz or RC mode

2.2 LCD

- LCD operation voltage**:** 4.5 V (VDD must be fixed at 3V)
- Common driver pins**:** 16
- Segment driver pins**:** 32
- 1/4 bias
- 1/16 duty

3 Applications

- Data Bank
- Message display box
- Scientific calculator

3.1 Application Notes

- In switching the main clock (from high frequency to low frequency or vice versa), or waking up from idle mode, 6 ~ 8 delay instructions (NOP) must be added.
- Avoid directly switching to Idle mode or Sleep mode from Normal mode. You must initially switch to Green mode, and then to Idle mode or Sleep mode.
- Under DATA RAM least address (A0~A7), when "INC" instruction is in use and overflow occurs, the middle address will automatically be incremented. If "DEC" instruction and least address from 0x00→0xFF is used, the middle address cannot and will not be automatically decremented.
- The Look-up table instruction can only change the program counter's Bit 7 ~ Bit 0 at a time and only 256 address can be searched on one occasion. If each 256 address is called as "zone" and each program page contains 1024 address, then each page contains four zones. When two zones overlap within a table, a bug will occur during address search. So you must examine the *.LST file after each compilation. The *.LST file will jot down the information, instruction address, etc., as well as the error messages if bug is found.
- During a reset, the values of the registers in the target chip (EM78862C) and that of ICE-808 may differ from each other. As the 808 ROMless chip of ICE is used to develop a program for EM78862C, its reset (initial) values cannot be repeated as reset values for the target chip. Otherwise, error may occur. The register reset values for the target chip should be those described in the EM78862C specification, not those from ICE-808.
- Applicable MASK, OTP, and ICE

MASK	OTP	ICE
EM78862C	EM78P808	ICE 808

4 Pin Configurations

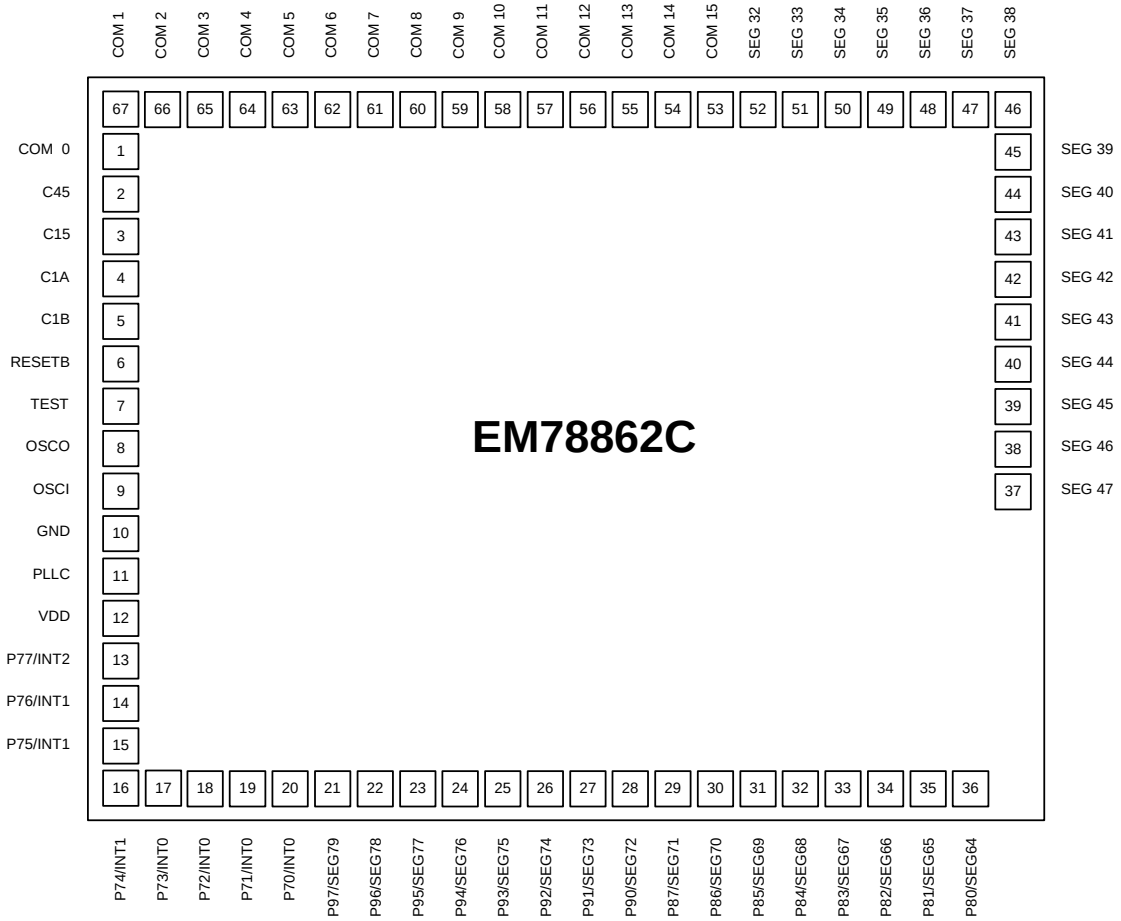


Fig. 1 EM78862C Pin Configuration for Die Form

4.1 Pin Description

Pin Name	Pin #	I/O Type	Description
VDD	12	Power	Digital power and analog power
GND	10	Power	Digital and analog ground
OSCI	9	I	Input pin for 32.768 kHz oscillatoror installing a resistor for RC mode
OSCO	8	O	Output pin for 32.768 KHz oscillator
COM0 ~ COM15	1 53~67	O	Common driver pins of LCD driver
SEG32 ~ SEG47 SEG64 ~ SEG79	37 ~ 52 21 ~ 36	O	Segment driver pins of LCD driver
PLLC	11	I	Phase loop lock capacitor. Connect a capacitor 0.01μ to 0.047μ with GND
INT0	17 ~ 20	I	Interrupt sources which have the same interrupt flag. Any pin from PORT70 to PORT73 has a falling edge signal, it will generate an interruption.
INT1	14 ~ 16	I	Interrupt sources which have the same interrupt flag. Any pin from PORT74 to PORT76 has a falling edge signal, it will generate an interruption.
INT2	13	I	Interrupt source. Once PORT77 receives a falling edge or rising edge signal (controlled by CONT register), it will generate an interruption.
P7.0 ~ P7.7	13 ~ 20	I/O	PORT7 (INPUT or OUTPUT port per bit) Internal Pull-high function Key scan function
P8.0 ~ P8.7	29 ~ 36	I/O	PORT8 (INPUT or OUTPUT port per bit) Shared with LCD segment signals
P9.0 ~ P9.7	21 ~ 28	I/O	PORT9 INPUT or OUTPUT port per bit And is shared with Segment signal
C1A	4	I	Capacitor C1 (1μF) connector pin for Voltage converter .
C1B	5	I	Capacitor C1 (1μF) connector pin for voltage converter .
C15 , C45	3 , 2	I	Connect each with a capacitor (1μF) to GND for voltage converter pin.
TEST	7	I	Test pin during Test mode only. Normally LOW
RESETB	6	I	System reset pin (LOW ACTIVE)

5 Functional Block Diagram

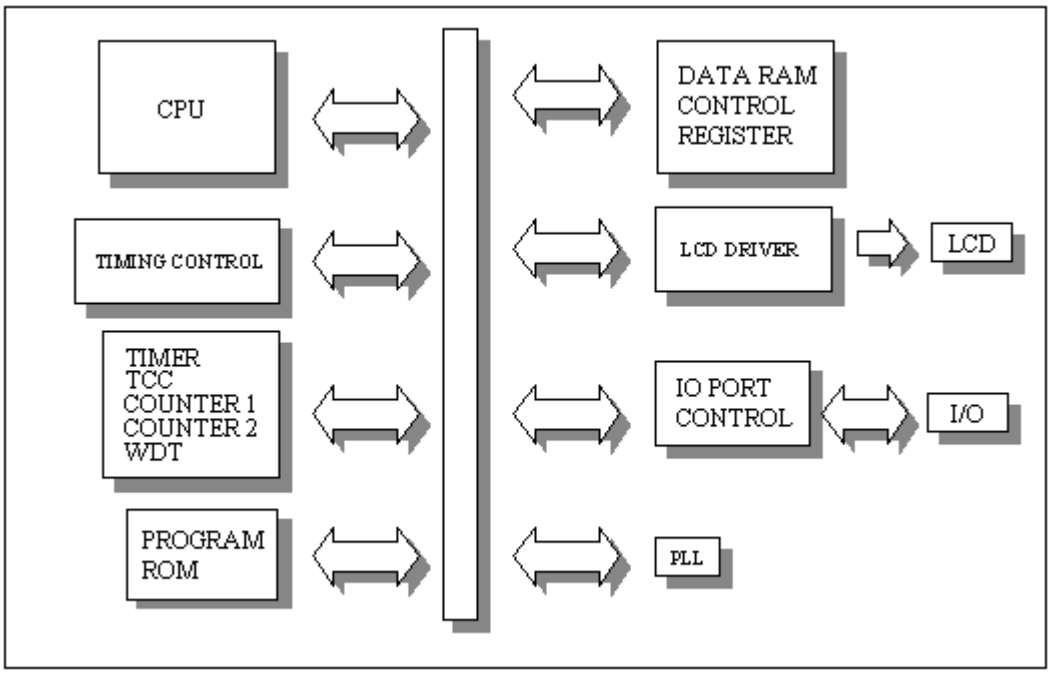


Fig. 2a System Overview Block Diagram

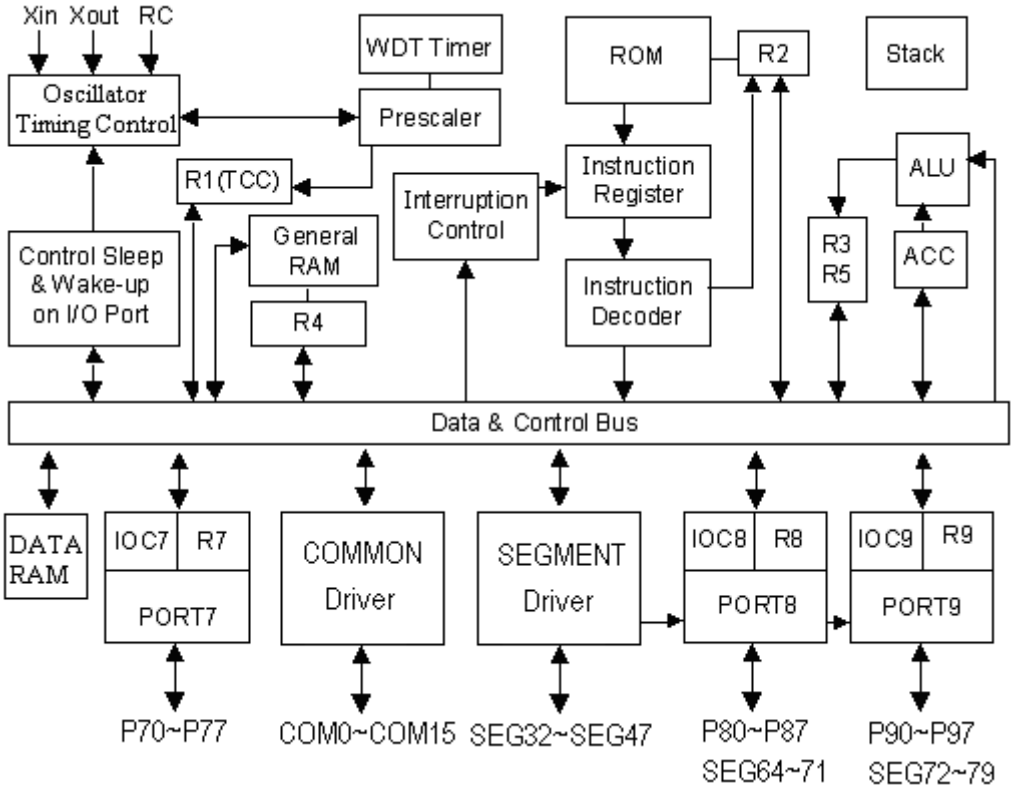


Fig. 2b System Functional Block Diagram

6 Functional Descriptions

6.1 Operational Registers

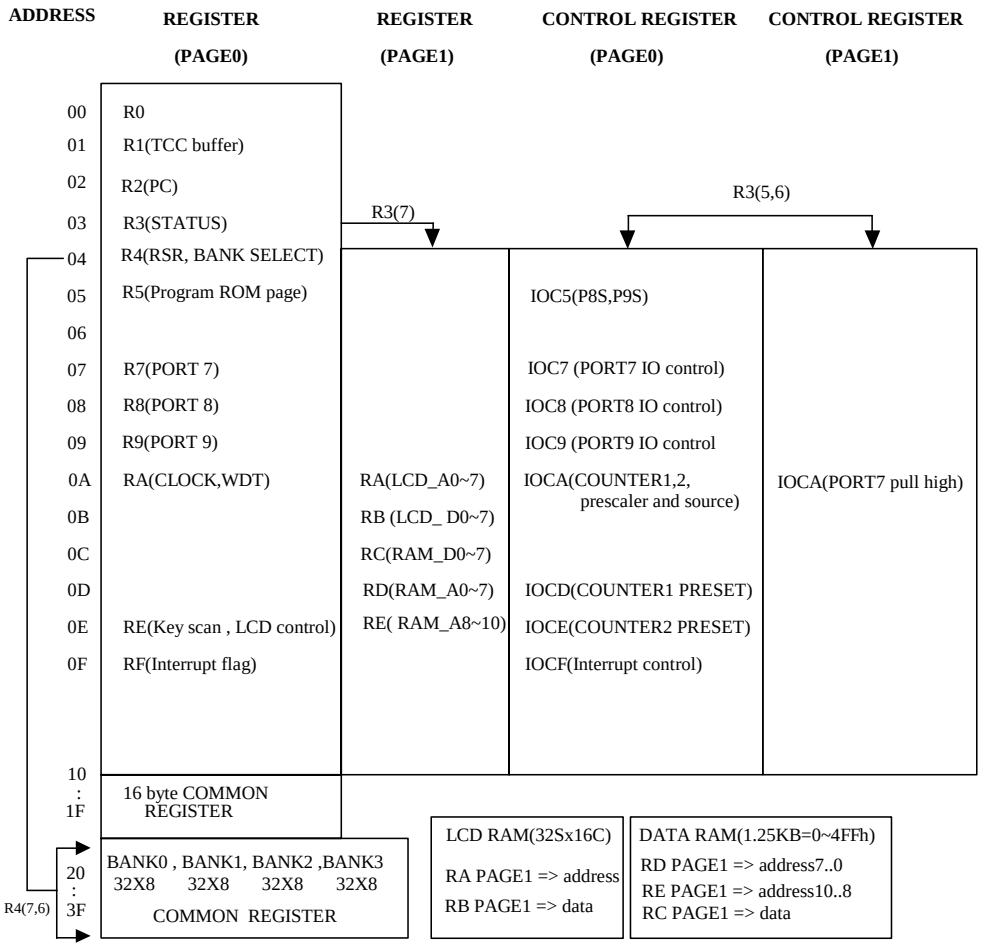


Fig. 3 Data Memory Configuration

6.1.1 R0 (Indirect Address Register)

R0 is not a physically implemented register. It is useful as indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

Example:

```
MOV   A,@0x20   ;Store an address at R4 for indirect addressing
MOV   0x04,A
MOV   A,@0xAA   ;Write data 0xAA to R20 at Bank0 through R0
MOV   0x00,A
```

6.1.2 R1 (TCC)

- TCC data buffer. Increased by 16.38kHz, RC/2 or by the instruction cycle clock (controlled by CONT register).
- Written and read by the program as any other register.

6.1.3 R2 (Program Counter)

- The structure is depicted in Fig. 4 below.
- Generates 16K × 13 on-chip PROGRAM ROM addresses to the relative programming instruction codes.
- "JMP" instruction allows the direct loading of the low 10 program counter bits.
- "CALL" instruction loads the low 10 bits of the PC, PC+1, and then push it into the stack.
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of stack.
- "MOV R2,A" allows loading of an address from the A register to the PC, and the ninth and tenth bits are cleared to "0'.'
- "ADD R2,A" allows a relative address to be added to the current PC, and contents of the ninth and tenth bits are cleared to "0'.'
- "TBL" allows a relative address to be added to the current PC, and contents of the ninth and tenth bits do not change. The most significant bit (A10~A13) will be loaded with the content of bit PS0 ~ PS3 in the status register (R5) upon execution of a "JMP',' "CALL',' "ADD R2,A,', or "MOV R2,A" instruction.
- If an interrupt triggers, the PROGRAM ROM will jump to address 0008H at Page 0. The CPU will automatically store the ACC, R3 status and R5 PAGE. It will be restored after instruction RETI is executed.

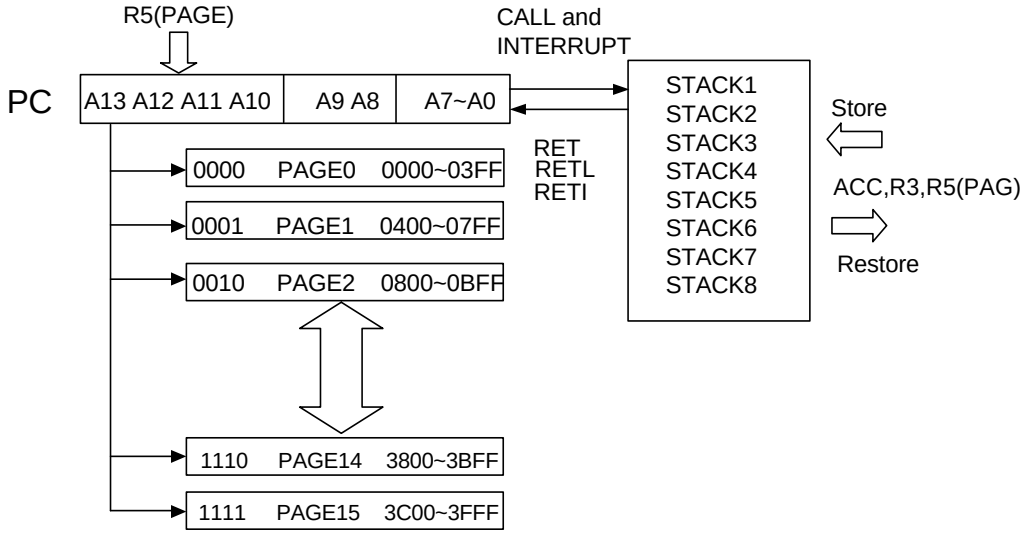


Fig. 4 Program Counter Organization

6.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAGE	IOCP1S	IOCPAGE	T	P	Z	DC	C

Bit 0 (C): Carry flag

Bit 1 (DC): Auxiliary carry flag

Bit 2 (Z): Zero flag

Bit 3 (P): Power down bit.
Set to 1 during power on or by "WDTC" command and reset to 0 by "SLEP" command.

Bit 4 (T): Time-out bit.
Set to 1 by the "SLEP" and "WDTC" command, or during power up. Reset to 0 by WDT timeout.

Event	T	P	Remark
WDT wake-up from sleep mode	0	0	
WDT time out (not sleep mode)	0	1	
RESET wake up from sleep	1	0	
Power up	1	1	
Low pulse on RESET pin	X	X	X =Don't care

Bit 5 (IOCPAGE): Change IOC5 ~ IOCE to another page,
0/1 → Page0/Page1 or 2 (determined by R3 Bit 6)

Bit 6 (IOCP1S): Change IOC PAGE1 and PAGE2 to another option register
0/1 → page1/page2

(Refer to Fig. 3, *Data Memory Configuration* for the control register Configuration details.)

Bit 6 (IOCP1S)	Bit 5 (IOCPAGE)	Page Select	Remark
X	0	PAGE 0	X =Don't care
0	1	PAGE 1	
1	1	PAGE 2	

Bit 7 (PAGE): Change RA ~ RE to another page
0/1 → page0/page1

(Refer to Fig. 3, *Data Memory Configuration* for the control register Configuration details.)

6.1.5 R4 (Register Bank Select Register) --- Page 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBK1	RBK0	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0

Bit 0 ~ Bit 5 (RSR0 ~ RSR5): Indirect addressing for common Registers R20 ~ R3F RSR bits are used to select up to 32 registers (R20 to R3F) in indirect addressing mode.

Bit 6 ~ Bit 7 (RBK0 ~ RBK1): Bank selection bits for common Registers R20 ~ R3F These selection bits are used to determine which bank is activated among the 4 banks of 32 registers (R20 to R3F) each.

(Refer to Fig. 3, *Data Memory Configuration* for the control register Configuration details.)

6.1.6 R5 (Program Page Select Register) --- Page 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	PS3	PS2	PS1	PS0

Bit 0 ~ 3 (PS0 ~ PS3): Page select bits as shown below:

PS3	PS2	PS1	PS0	Program Memory Page (Address)
0	0	0	0	Page 0
0	0	0	1	Page 1
0	0	1	0	Page 2
::				::
1	1	1	0	Page 14
1	1	1	1	Page 15

You can use PAGE instruction to change and maintain program page. Otherwise, use **far jump** (FJMP) or **far call** (FCALL) MACRO instructions to program user's code. ELAN's complier supports program page maintenance and can change your program by inserting the appropriate instructions within the program.

Bit 4 ~ 7: Not used

6.1.7 R7 (Port 7) --- Page 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P77	P76	P75	P74	P73	P72	P71	P70

Bit 0 ~ Bit 7 (P70 ~ P77): 8-bit PORT7 (0 ~ 7) I/O data register
You can use IOC7 Page 0 register to define each bit as input or output.

6.1.8 R8 (Port8) --- Page 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P87	P86	P85	P84	P83	P82	P81	P80

Bit 0 ~ Bit 7 (P80 ~ P87): 8-bit PORT8 (0 ~ 7) I/O data register
You can use IOC8 Page 0 register to define each bit as input or output.

6.1.9 R9 (Port9) --- Page 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P97	P96	P95	P94	P93	P92	P91	P90

Bit 0 ~ Bit 7 (P90 ~ P97): 8-bit PORT9 (0 ~ 7) I/O data register
You can use IOC9 Page 0 register to define each bit as input or output.

6.1.10 RA (Mode Control Register) --- Page 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IDLE	PLLEN	CLK1	CLK0	-	-	-	WDTEN

Bit 0 (WDTEN): Watch dog control register
0/1 → disable/enable
You can use WDTC instruction to clear watch dog timer. The timer's clock source is 32.768k/2 Hz. If the prescaler is assigned to TCC, the watchdog timer will time out by (1/32768) * 2 * 256 = 15.616ms. If assigned to WDT, the time out time will be longer than 15.616ms depending on the prescaler ratio.

Bit 1 ~ Bit 3: Not used

Bit 4 ~ Bit 5 (CLK0 ~ CLK1): Main clock = 3.579Mhz, CLK0 ~ CLK1 are set to '1'.

Bit 6 (PLLEN): PLL enable control bit
0/1 → disable/enable
This is the CPU mode control register. If PLL is enabled, CPU will operate under Normal mode (high frequency, main clock). Otherwise, it will run under Green mode (low frequency, 32.768kHz).
The relation between 32.768K and 3.579M crystal is explained in the following figure.

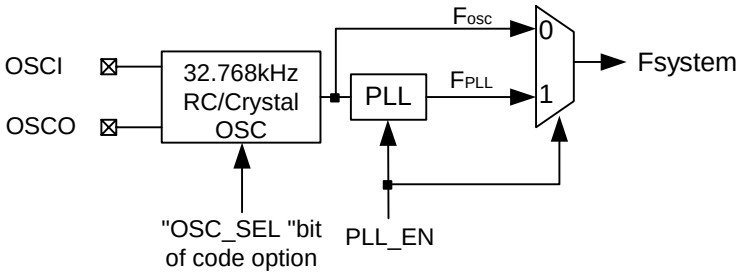


Fig. 5 The Relation between 32.768KHz and 3.579MHz

Bit 7 (IDLE): Power saving mode control register

When PLL is disabled, you can set this bit with **SLEP** instruction to define SLEEP/IDLE mode selection, i.e., 0/1 → SLEEP mode/IDLE mode.

This bit determines which mode will be set for **SLEP** instruction.

Wakeup Signal	SLEEP Mode	IDLE Mode	GREEN Mode	NORMAL Mode
	RA(7,6)=(0,0) + SLEP	RA(7,6)=(1,0) + SLEP	RA(7,6)=(x,0) no SLEP	RA(7,6)=(x,1) no SLEP
TCC Time-Out	X	Wake-up + Interrupt + Next instruction	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
Counter 1 Time-Out	X	Wake-up + Interrupt + Next instruction	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
Counter 2 Time-Out	X	Wake-up + Interrupt + Next instruction	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
Port7.0 ~ 7.7 (INT0~2)	RESET	Wake-up + Interrupt + Next instruction	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
WDT Time-Out	RESET	Wake-up + Next instruction	RESET	RESET

NOTE

1. *PORT 70 ~ PORT 73's wake-up function is controlled by IOCF Bit 3 and ENI instruction. They are triggered by a falling edge.*
2. *PORT 74 ~ PORT 76's wake-up function is controlled by IOCF Bit 4 and ENI instruction. They are triggered by a falling edge.*
3. *PORT 77's wake-up function is controlled by IOCF Bit 5 and ENI instruction. It is triggered by a falling edge or a rising edge (controlled by CONT register).*

6.1.11 RA (LCD Address0~7) --- Page 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCD_A7	LCD_A6	LCD_A5	LCD_A4	LCD_A3	LCD_A2	LCD_A1	LCD_A0

Bit 0 ~ Bit 7 (LCD_A0 ~ LCD_A7): LCD address for LCD RAM reading or writing
The LCD RAM corresponds to the COMMON and SEGMENT signals as shown in the following table**:**

COM15 ~COM8	COM7 ~ COM0	SEGMENT
Address 80H	Address 00H	Dummy
:	:	:
Address 9FH	Address 1FH	Dummy
Address A0H	Address 20H	SEG 32
Address A1H	Address 21H	SEG 33
:	:	:
Address AEH	Address 2EH	SEG 46
Address AFH	Address 2FH	SEG 47
Address B0H	Address 30H	Dummy
:	:	:
Address BFH	Address 3FH	Dummy
Address C0H	Address 40H	SEG 64
Address C1H	Address 41H	SEG 67
:	:	:
Address CEH	Address 4EH	SEG78
Address CFH	Address 4FH	SEG79
Address D0H	Address 50H	Dummy
:	:	:
Address FFH	Address 7FH	Dummy

6.1.12 RB (LCD Data Buffer) --- Page 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCD_D7	LCD_D6	LCD_D5	LCD_D4	LCD_D3	LCD_D2	LCD_D1	LCD_D0

Bit 0 ~ Bit 7 (LCD_D0 ~ LCD_D7): LCD data buffer for LCD RAM reading or writing

Example.

```
MOV     A,@0
MOV     R9_PAGE1,A
MOV     RA_PAGE1,A          ;Address
MOV     A,@0XAA
MOV     RB_PAGE1,A          ;Write data 0xAA  to LCD RAM
MOV     A,RB_PAGE1          ;Read data from LCD RAM
```

6.1.13 RC (DATA RAM Data Buffer) ---Page 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RAM_D7	RAM_D6	RAM_D5	RAM_D4	RAM_D3	RAM_D2	RAM_D1	RAM_D0

Bit 0 ~ Bit 7 (RAM_D0 ~ RAM_D7) : Data RAM data buffer for RAM reading or writing.

Example:

```
MOV    A , @1
MOV    RD_PAGE1 , A
MOV    A , @0
MOV    RE_PAGE1 , A
MOV    A , @0x55
MOV    RC_PAGE1 , A    ;Write data 0x55 to DATA RAM which address is "0001"
MOV    A , RC_PAGE1    ;Read data
```

6.1.14 RD (DATA RAM Address0~7) --- Page 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RAM_A7	RAM_A6	RAM_A5	RAM_A4	RAM_A3	RAM_A2	RAM_A1	RAM_A0

Bit 0 ~ Bit 7(RAM_A0~RAM_A7): Data RAM address for RAM reading or writing

6.1.15 RE (KEYSCAN, LCD Control) --- Page 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	K_SCAN	LCD_C1	LCD_C0	LCD_M1	LCD_M0

Bit 0 ~ Bit 1 (LCDM0~LCDM1): Set to “0” for 1/16 duty, 1/4 bias.

Bit 2 ~ Bit 3 (LCD_C0~LCD_C1): LCD operation function definition.

LCD_C1, LCD_C0	LCD Operation
0,0	Disable
0,1	Blanking
1,0	Reserved
1,1	LCD enable

Bit 4 (K_SCAN): Key scan function enable control bit. 0/1 → disable/enable
Once you enable this bit, all of the LCD signal will have a low pulse during a common or segment period. This pulse has a 30μs width. Use the following procedures to implement the key scans function**:**

a) Set Port 7 as input port
b) Set IOCA Page 1 Port 7 to pull high
c) Enable scan key signal
d) Once a key is pressed, set RA (6) = 1, and switch to normal mode
e) Blank LCD. Disable scan key signal

f) Set P9SL = 0, P9SH = 0. Port9 sends probe signal to Port7 and read Port7 to get the key. Note that a probe signal instruction delay will occur before the next instruction is performed.

g) Set P9SH = 1, P9SL = 1. Define Port9 as LCD signal and enable LCD.

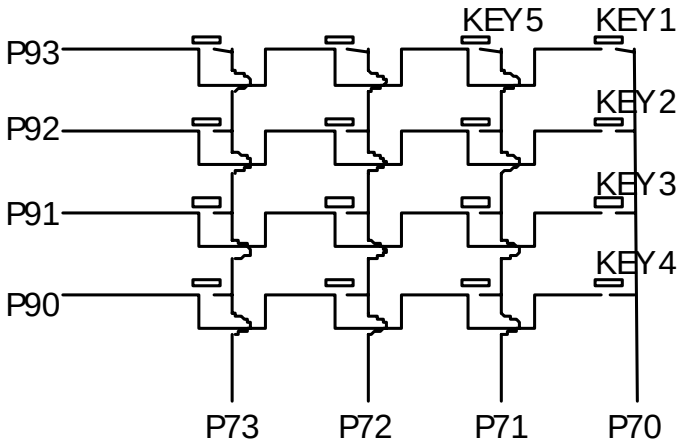


Fig. 6 Scan Key Circuit

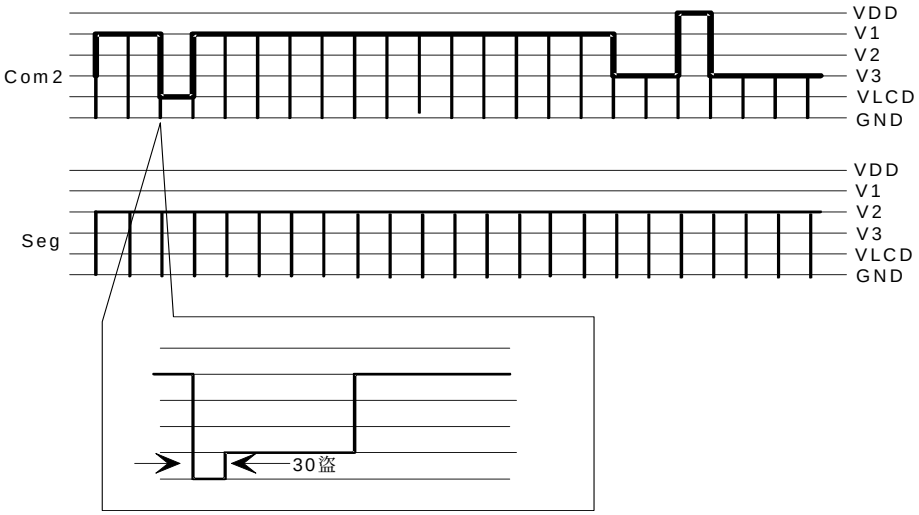


Fig. 7 Key Scan Waveform

NOTE

1. *The controller can drive the LCD directly. LCD block is made up of LCD driver, display RAM, segment output pins, common output pins, and LCD operating voltage converter capacitor pins. LCD voltage converter pins C1A & C1B should be connected with a C1 (1uF) capacitor. C14 & C45 need to be connected with 1uF capacitors to the ground.*
2. *The number of common and frame frequency are determined by LCD mode Register RE PAGE0 Bit 0~ Bit 1.*
3. *LCD driver can be regulated into different levels of driving mode (refer to Section 6.2.4, "IOC6 PAGE2" register).*
4. *The basic structure contains a timing control which uses the basic frequency 32.768kHz to generate the proper timing for display access. RE PAGE0 register is a command register for LCD driver and display. The LCD display (disable, enable, blanking) is controlled by RE PAGE0 Bit 2 ~ Bit 3 and the driving duty is decided by RE PAGE Bit 0 ~ Bit 1. LCD display data is stored in LCD RAM which address and data access are controlled by registers RA PAGE1 and RB PAGE1.*

Bits 5 ~ Bit 7: Not used

6.1.16 RE (DATA RAM Address8 ~ 10) --- Page 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	RAM_A10	RAM_A9	RAM_A8

Bit 0 ~ Bit 2 (RAM_A8~RAM_A10): Data RAM address (Address8 to Address10) for RAM reading (can be addressed from 0h to 4FFh maximum).

Bit 3 ~ Bit 7: Not used.

6.1.17 RF (INTERRUPT Flags)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	INT2	INT1	INT0	CNT2	CNT1	TCIF

* "1" = interrupt request; "0" = non-interrupt

Bit 0 (TCIF): TCC timer overflow interrupt flag
When TCC timer overflows, interrupt is set.

Bit 1 (CNT1): Counter1 timer overflow interrupt flag
When Counter1 timer overflows, interrupt is set.

Bit 2 (CNT2): Counter2 timer overflow interrupt flag
When Counter2 timer overflows, interrupt is set.

Bit 3 (INT0): External INT0 pin interrupt flag
When PORT70, PORT71, PORT72, or PORT73 encounters a falling edge trigger signal, CPU sets this bit to interrupt.

Bit 4 (INT1): External INT1 pin interrupt flag

When PORT74, PORT75, or PORT76 encounters a falling edge trigger signal, CPU sets this bit to interrupt.

Bit 5 (INT2): External INT2 pin interrupt flag
When PORT77 encounters a falling s this bit to interrupt.

Bits 6 ~ 7: Not used.

6.1.18 R10 ~ R1F and R20 ~ R3F (General Purpose Registers)

R10 ~ R1F & R20 ~ R3F (Banks 0~3) are general-purpose registers

6.2 Special Purpose Registers

6.2.1 A (Accumulator, ACC)

Internal data transfer, or instruction operand holding. This is not an addressable register.

6.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT_EDGE	INT	TS	-	PAB	PSR2	PSR1	PSR0

Bit 0 ~ Bit 2 (PSR0~PSR2): TCC/WDT pre-scale bits

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Bit 3 (PAB): Prescaler assigned bit
0/1 → TCC/WDT

Bit 4: Not used

Bit 5 (TS): TCC signal source
0 → Instruction clock
1 → 16.384kHz or RC/2
Instruction clock = MCU Clock/2. Refer to RA Bit 4 ~ Bit 6 Page 0 for PLL (Section 6.1.10) and Main Clock selection (Section 6.3, Fig.8).

Bit 6 (INT): INT enable flag

0 → interrupt masked by DISI or hardware interrupt

1 → interrupt enabled by **ENI**/**RETI** instructions

Bit 7 (INT_EDGE): interrupt edge type of P77

0 → P77's interrupt source is a rising edge and falling edge signal.

1 → P77's interrupt source is a falling edge signal.

CONT register is readable (CONTR) and writable (CONTW).

6.2.3 IOC5 (Port8 & Port9 Port Switch Register) --- Page 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	P9SH	P9SL	P8SH	P8SL

Bit 0 (P8SL) : Switch low nibble I/O PORT8 or LCD segment output for share pins SEGnn/P8n pins

0 → select normal P80 ~ P83 for low nibble PORT8

1 → select SEG64 ~ SEG67 output for LCD SEGMENT output

Bit 1 (P8SH): Switch high nibble I/O PORT8 or LCD segment output for share pins SEGnn/P8n

0 → select normal P84 ~ P87 for high nibble PORT8

1 → select SEG68 ~ SEG71 output for LCD SEGMENT output

Bit 2 (P9SL): Switch low nibble I/O PORT9 or LCD segment output for share pins SEGnn/P9n pins

0 → select normal P90 ~ P93 for low nibble PORT9

1 → select SEG72 ~ SEG75 output for LCD SEGMENT output

Bit 3 (P9SH): Switch high nibble I/O PORT9 or LCD segment output for share pins SEGnn/P9n pins

0 → select normal P94 ~ P97 for high nibble PORT9

1 → select SEG76 ~ SEG79 output for LCD SEGMENT output.

Bits 4 ~ 7: Not used

6.2.4 IOC7 (Port7 I/O Control Register) --- Page 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70

Bit 0 ~ Bit 7(IOC70 ~ IOC77): PORT7(0~7) I/O direction control register

0 → set the relative I/O pin as output

1 → set the relative I/O pin as input (high impedance)

6.2.5 IOC8 (Port8 I/O Control Register) --- Page 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC87	IOC86	IOC85	IOC84	IOC83	IOC82	IOC81	IOC80

Bit 0 ~ Bit 7(IOC80 ~ IOC87): PORT8(0~7) I/O direction control register
0 → set the relative I/O pin as output
1 → set the relative I/O pin as input (high impedance)

6.2.6 IOC9 (Port9 I/O Control Register) --- Page 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC97	IOC96	IOC95	IOC94	IOC93	IOC92	IOC91	IOC90

Bit 0 ~ Bit 7(IOC90 ~ IOC97): PORT9 (0~7) I/O direction control register
0 → set the relative I/O pin as output
1 → set the relative I/O pin into high impedance (input)

6.2.7 IOCA (CNT1 & CNT2 Clock Source and Scaling) --- Page 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNT2S	C2P2	C2P1	C2P0	CNT1S	C1P2	C1P1	C1P0

Bit 0 ~ Bit 2 (C1P0 ~ C1P2): Counter1 scaling

C1P2	C1P1	C1P0	Counter 1
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3 (CNT1S): Counter 1 clock source
0/1 → (16.384kHz or RC/2) / instruction clock

Bit 4 ~ Bit 6 (C2P0 ~ C2P2): Counter2 scaling

C2P2	C2P1	C2P0	Counter 2
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 7 (CNT2S): Counter 2 clock source
0/1 → (16.384kHz or RC/2) / instruction clock

6.2.8 IOCA (PORT 7 Pull-High Control Register) --- Page 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH77	PH76	PH75	PH74	PH73	PH72	PH71	PH70

Bit 0 ~ Bit 7 (PH70 ~ PH77): PORT7 (0~7) pull high control register
0 → disable pull high function
1 → enable pull high function

6.2.9 IOCD (COUNTER 1 Data Buffer Register) --- Page 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNT1_D7	CNT1_D6	CNT1_D5	CNT1_D4	CNT1_D3	CNT1_D2	CNT1_D1	CNT1_D0

Bit 0 ~ Bit 7 (CNT1_D0~CNT1_D7): Counter1's data buffer
User can read and write to this buffer. Counter1 is an 8-bit up-counter with 8-bit prescaler that uses IOCD to preset and read the counter (write = preset). After an interruption, it will reload the preset value.

Examples:

```
Write: IOW  0x0D      ;write the data at accumulator to Counter1
                      ;(preset)
Read:  IOR  0x0D      ;read IOCD data and write to accumulator
```

6.2.10 IOCE (COUNTER 2 Data Buffer Register) --- Page 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNT2_D7	CNT2_D6	CNT2_D5	CNT2_D4	CNT2_D3	CNT2_D2	CNT2_D1	CNT2_D0

Bit 0 ~ Bit 7 (CNT2_D0 ~ CNT2_D7): Counter2's data buffer
User can read and write this buffer. Counter 2 is an 8-bit up-counter with 8-bit pre-scale that uses IOCE to preset and read the counter (write = preset). After an interruption, it will reload the preset value.

Examples:

```
Write: IOW  0x0E      ;write the data at accumulator to Counter2 (preset)
Read:  IOR  0x0E      ;read IOCE data and write to accumulator
```

6.2.11 IOCF (INTERRUPT Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	INT2	INT1	INT0	CNT2	CNT1	TCIF

Bit 0 ~ Bit 5: Interrupt enable bits
0/1 → disable interrupt/enable interrupt

Bit 6 ~ Bit 7: Not used

6.3 TCC/WDT Prescaler

- An 8-bit counter is available as prescaler for the TCC or WDT. The prescaler is available only to either the TCC or WDT at a time.
- An 8-bit counter is made available for TCC or WDT as determined by the status of Bit 3 (PAB) of CONT register.
- The prescaler ratio is described in Section 6.2.2, *CONT (Control Register)*.
- The TCC/WDT circuit diagram is shown in Fig. 10 below.
- Both TCC and prescaler are cleared by instructions.
- The prescaler will be cleared by the **WDTC** and **SLEP** instructions when running under WDT mode.
- However, the prescaler cannot be cleared by **SLEP** instruction when running under TCC mode.

NOTE
CONT is a readable and writable register.

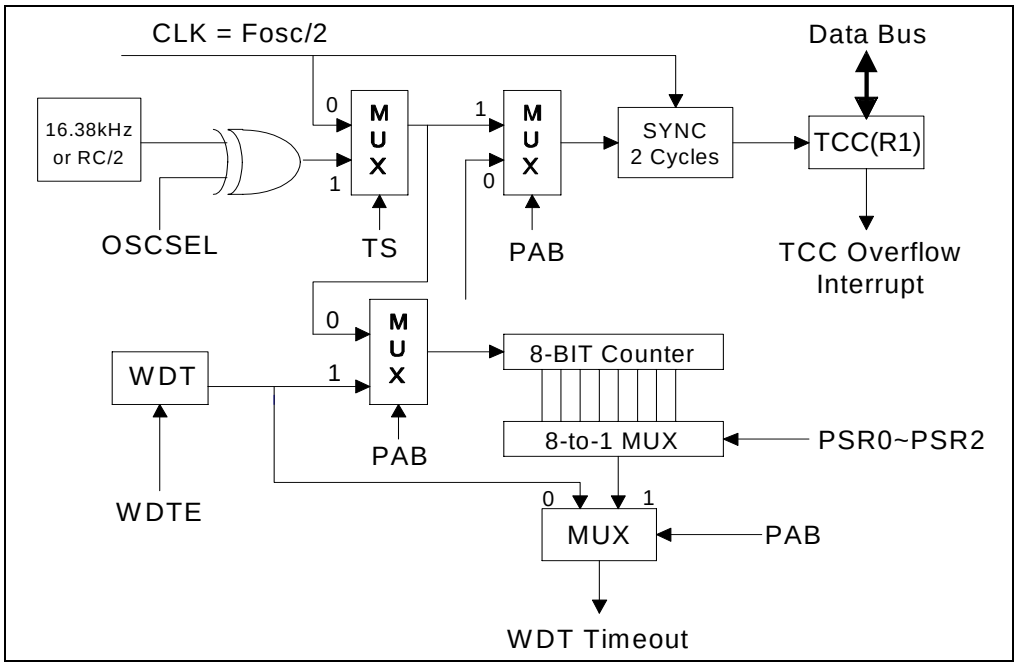


Fig. 8 TCC WDT Block Diagram

6.4 I/O Ports

The I/O registers (Ports 7, 8, and 9), are bi-directional tri-state I/O ports. Port 7 can be pulled-high internally by software. Furthermore, each I/O pin can be defined as "input" or "output" pin by the I/O control registers (IOC7 ~ IOC9). The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits are shown in Fig. 9 below.

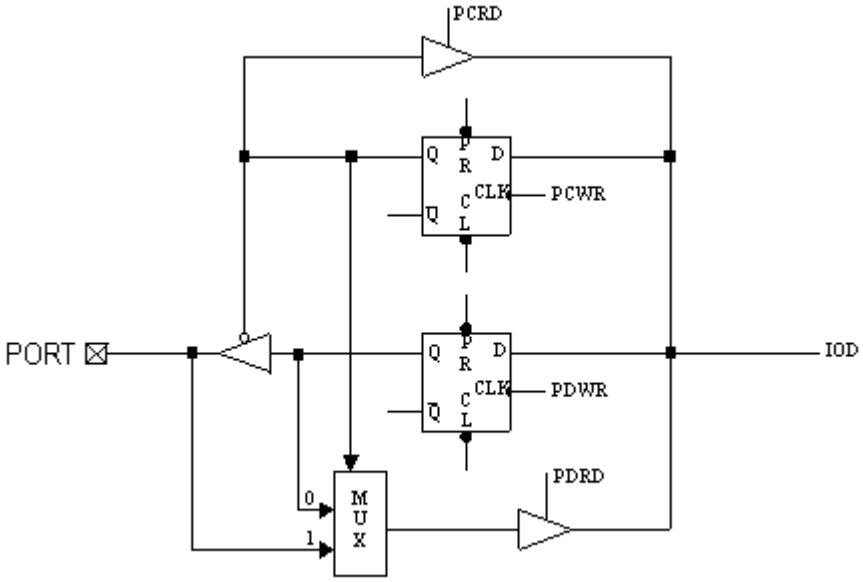


Fig. 9 Ports 7, 8, & 9 I/O Port and I/O Control Register Circuit

6.5 RESET

RESET will occur during any of the following conditions:

- Power on reset
- WDT timeout (if WDT is enabled during SLEEP, GREEN, or NORMAL mode)
- RESET pin pull low

Once a RESET occurs, the following functions are performed:

- The oscillator will continue running and the Program Counter (R2) is set to all "0"
- All I/O port pins are configured to input mode (high-impedance state)
- The TCC/Watchdog timer and prescaler are cleared and Watchdog timer is disabled
- When power is switched on, the upper 3 bits of R3 and the upper 2 bits of R4 are cleared
- The bits of the CONT register are set to all "1"

■ For the other registers (Bit 7 ~ Bit 0), refer to the following table:

ICE-808 Registers

Address	R Register Page0	R Register Page1	IOC Register Page0	IOC Register Page1	IOC Register Page2
4	00xxxxxx	00000000	-	-	xxxxxxxx
5	xxxx0000	xxxxxxxx	11100000	00000000	00000000
6	xxxxxxxx	xxxxxxxx	11111111	00000000	00000000
7	xxxxxxxx	xxxxxxxx	11111111	11111111	xxxxxxxx
8	xxxxxxxx	xxxxxxxx	11111111	11111111	xxxxxxxx
9	xxxxxxxx	xxxxxxxx	11111111	00000000	xxxxxxxx
A	00000xx0	xxxxxxxx	00000000	00000000	xxxxxxxx
B	xxxxxxxx	xxxxxxxx	11111111	00000000	xxxxxxxx
C	xxxxxxxx	xxxxxxxx	11111111	00000000	xxxxxxxx
D	00000000	xxxxxxxx	00000000	00000000	xxxxxxxx
E	00000000	00xxxxxx	00000000	00000000	00000000
F	00000000	-	00000000	-	

EM78862C Registers

Address	R Register Page0	R Register Page1	IOC Register Page0	IOC Register Page1	IOC Register Page2
4	00xxxxxx	00000000	-	-	-
5	00000000	00000000	11100000	11000000	00000000
6	00000000	00000000	11111111	00000000	00000000
7	xxxxxxxx	00000000	11111111	11111111	-
8	xxxxxxxx	00000000	11111111	11111111	-
9	xxxxxxxx	00000000	11111111	00000000	-
A	00110110	xxxxxxxx	00000000	00000000	-
B	00000000	xxxxxxxx	11111111	00000000	-
C	00000000	xxxxxxxx	11111111	00000000	-
D	00110000	xxxxxxxx	00000000	00000000	-
E	10000000	10000xxx	00000000	00000000	00000000
F	00000000	-	00000000	-	-

Shaded bits are circuit fixed value

6.6 WAKE-UP

The WAKE-UP signals are as follows:

Wake-Up Signal	Sleep Mode RA(7,6)=(0,0) + SLEP	Idle Mode RA(7,6)=(1,0) + SLEP	Green Mode RA(7,6)=(x,0) No SLEP	Normal Mode RA(7,6)=(x,1) No SLEP
TCC time out IOCF Bit0=1	X	Wake-up+ Interrupt + Next instruction	Interrupt	Interrupt
Counter 1 time out IOCF Bit1=1	X	Wake-up+ Interrupt + Next instruction	Interrupt	Interrupt
Counter 2 time out IOCF Bit2=1	X	Wake-up+ Interrupt + Next instruction	Interrupt	Interrupt
INT0 pin(P70~3) IOCF Bit3=1	RESET	Wake-up+ Interrupt + Next instruction	Interrupt	Interrupt
INT1 pin(P74~6) IOCF Bit4=1	RESET	Wake-up+ Interrupt + Next instruction	Interrupt	Interrupt
INT2 pin(P77) IOCF Bit5=1	RESET	Wake-up+ Interrupt + Next instruction	Interrupt	Interrupt
WDT time out	RESET	Wake-up+ next instruction	RESET	RESET

X = No function

6.7 Oscillator

The oscillator system is used to generate the device clock. The oscillator system is composed of an RC or crystal oscillator and a PLL oscillator as illustrated below.

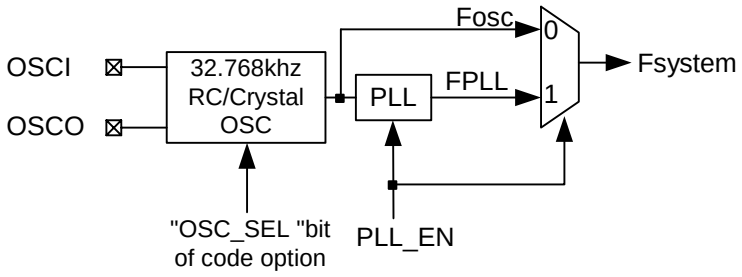


Fig. 10 Oscillator and PLL Function Block

NOTE

1. *Under RC oscillator mode, the pull-up resistor that connects to OSCI pin and OSC0 pin should be floating.*
2. *Under 32.768kHz crystal oscillator mode, the crystal is connected between OSCI pin and OSCO pin. A 20~30pF capacitor should be connected between each of the pins and ground.*

6.8 Interrupt

The EM78862C IC has two types of internal interrupts which are falling edge triggered**:**

- TCC timer overflow interrupt (internal)
- Two 8-bit counters overflow interrupt

If these interrupt sources change signal from high to low, the RF register will generate '1' flag to the corresponding register if IOCF register is enabled.

RF is the interrupt status register which records the interrupt request in flag bit. IOCF is the interrupt mask register. Global interrupt is enabled by **ENI** instruction and is disabled by **DISI** instruction. When one of the interrupts (if enabled) is generated, the next instruction will be fetched from address 008H. Once in the interrupt service routine, the source of the interrupt can be determined by polling the flag bits in the RF register.

Four external interrupt pins, i.e., INT0, INT1, INT2, & INT3, and three internal interrupts are available**:**

- External interrupt signals (INT0, INT1 and INT2) are from Port7 Bit 0 to Bit 7. If IOCF is enabled, then these signals will activate interrupt. Otherwise, these signals will be treated as general input data.
- Internal signals include TCC, CNT1, and CNT2.
- After a reset, the next instruction will be fetched from Address 000H and the hardware interrupt is 008H.
- After timeout, TCC will go to Address 008H when in GREEN mode or NORMAL mode. When in IDLE mode, TCC will go to Address 008H run interrupt service. After RETI instruction jump to the next instruction after “SLEP” instruction. These two conditions will set a RF flag.
- The interrupt flag bit must be cleared in software before leaving the interrupt service routine in order to prevent and avoid recursive interrupts.

NOTE

It is very important to save ACC, R3, and R5 when processing an interrupt as illustrated below:

```
0×08    DISI                        ;Disable interrupt
0×09    MOV     A_BUFFER, A         ;Save ACC
0×0A    SWAP    A_BUFFER
0×0B    SWAPA   0x03                ;Save R3 status
0×0C    MOV     R3_BUFFER, A
0×0D    MOV     A, 0x05             ;Save ROM page register
0×0E    MOV     R5_BUFFER, A
        :
        :
  :     MOV     A, R5_BUFFER        ;Return R5
  :     MOV     0X05,A
  :     SWAPA   R3_BUFFER           ;Return R3
  :     MOV     0X03,A
  :     SWAPA   A_BUFFER            ;Return ACC
  :     RETI
```

6.9 LCD Driver

The IC can drive LCD directly and has 32 segments and 16 commons that can drive a total of 32*16 dots. LCD block is made up of LCD driver; display RAM, segment output pins, common output pins, and LCD operating power supply pins.

The basic structure (as illustrated in Figs 11, 12, & 13) contains a timing control which uses the basic frequency 32.768kHz or RC to generate the proper timing for display access. RE register is a command register for LCD driver. The LCD display (disable, enable, & blanking) is controlled by LCD_C and the driving duty and bias is decided by LCD_M. The display data is stored in data RAM which address and data access are controlled by registers RA Page1 and RB Page1.

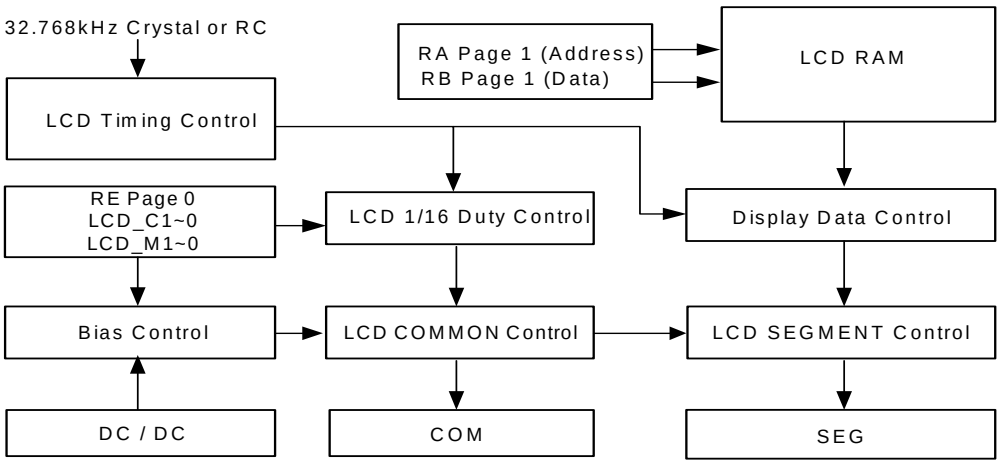


Fig. 11 LCD Driver Control Block

COM Signal: The number of COM pins varies according to the duty cycle in use as described in the next paragraph.

SEG Signal**:** The 32 segment signal pins are connected to the corresponding display RAM Address 20h ~ 2Fh, 40h ~ 4Fh, A0h ~ AFh, and C0h to CFh. All data address from Com0 ~ Com7 (located within Adress 20h ~ 2Fh, 40h ~ 4Fh) and Com8 ~ Com15 (located within Address A0h ~ AFh and C0h ~ CFh) are needed.

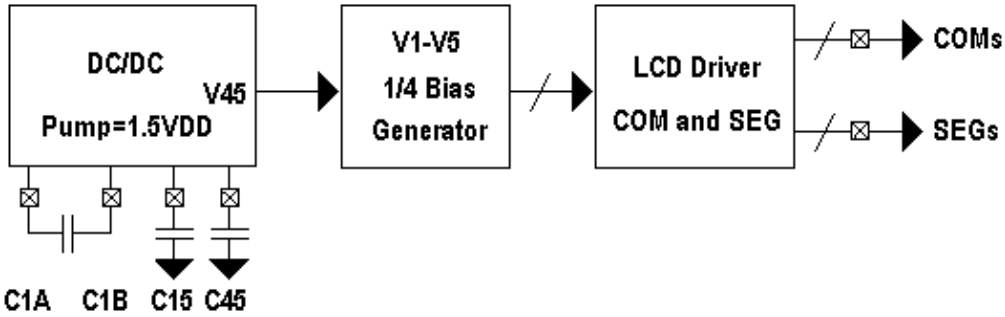


Fig.12 LCD DC/DC and Bias Generator

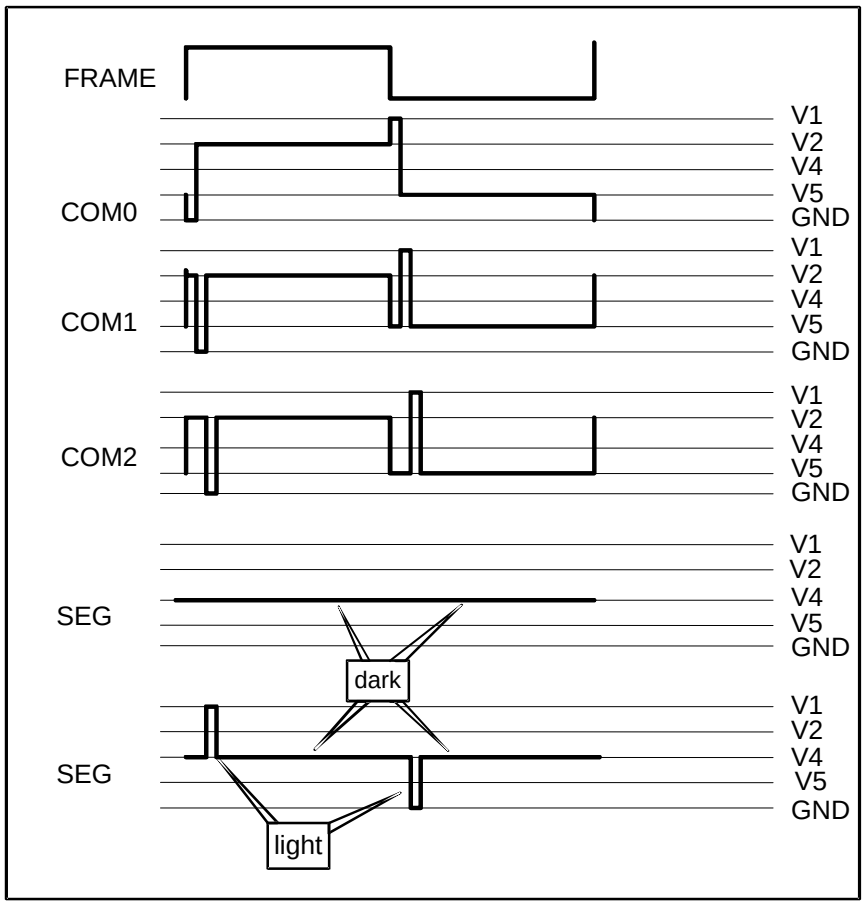


Fig.13 Relation Between Bias and V1 to V5

6.10 Code Options

The EM78862C IC has a built-in CODE option register that is not a part of the normal program memory. The option bits cannot be accessed during normal program execution.

Bit 0
OSCSEL

Bit 0 (OSCSEL): Oscillator option
0: RC mode
1: Crystal mode
RC or crystal oscillator is selected by OSCSEL bit of code option.

6.11 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods).

Unless the program counter is changed by instructions "MOV R2, A," "ADD R2, A," or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2, A," "BS(C) R2, 6," "CLR R2," etc.). Under this condition, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows**:**

a) Change one instruction cycle to consist of 4 oscillator periods.

b) Execute within two instruction cycles, "JMP," "CALL," "RET," "RETL," & "RETI," or the conditional skip ("JBS," "JBC," "JZ," "JZA," "DJZ," & "DJZA") instructions which were tested to be true. Also execute within two instruction cycles the instructions that are written to the program counter.

Furthermore, the instruction can provide the following features**:**

- Every bit of any register can be set, cleared, or tested directly.
- The I/O register can be regarded as a general register. That is, the same instruction can operate on the I/O register.

BINARY INSTRUCTION	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None 1
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None 1
0 0000 0010 0000	0020	TBL	R2+1 → R2 , R2+A → R2 Bits 8~9 of R2 unchanged	Z, C, DC
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R 2	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R (R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 (A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 (R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 (A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 (R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) (A(n-1), R(0) (C, C (A(7)	C

1. This instruction is applicable to IOC5 ~ IOC9, IOCA, IOCB, IOCC, IOCD, IOCE, & IOCF only.

2 Source and destination must be the same.

BINARY INSTRUCTION	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
0 0110 01rr rrrr	06rr	RRC R	R(n) (R(n-1), R(0) (C, C (R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) (A(n+1), R(7) (C, C (A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) (R(n+1), R(7) (C, C (R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → (A(4-7), R(4-7) → (A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 (A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 (R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 (R(b)	None [3]
0 101b bbrr rrrr	0xxx	BS R,b	1 (R(b)	None [4]
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 ([SP], (Page, k) (PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) (PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k (A	None
1 1001 kkkk kkkk	19kk	OR A,k	A (k (A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k (A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A (k (A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k (A, [Top of Stack] (PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A (A	Z, C, DC
1 1110 0000 0010	1E02	INT	PC+ 1 [SP], 001H (PC	None
1 1110 1000 kkkk	1E8k	PAGE k	k->R5(3:0)	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A (A	Z, C, DC

3. This instruction is not recommended for RF operation.

4. This instruction cannot operate under RF.

The symbol "R" in the instruction set represents a register designation that specifies which one of the registers (including operational registers and general purpose registers) is to be utilized by the instruction.

The symbol "b" represents a bit field designator that selects the value for the bit that is located in the register "R" and affects operation.

The symbol "k" represents an 8 or 10-bit constant or literal value.

7 Absolute Maximum Ratings

RATING	SYMBOL	VALUE	UNIT
DC Supply Voltage	Vdd	–0.3 to 5.5	V
Input Voltage	Vin	Vdd ±0.5	V
Operating Temperature Range	Ta	0 to 70	℃

8 DC Electrical Characteristics

Ta=0℃ ~ 70℃, VDD=3V, VSS=0V

Symbol	Parameter	Condition	Min	Type	Max	Unit
IIL1	Input Leakage Current for input pins	VIN = VDD, VSS	-	-	±1	μA
IIL2	Input Leakage Current for bi-directional pins	VIN = VDD, VSS	-	-	±1	μA
VIH	Input High Voltage	-	0.8VDD	-	VDD	V
VIL	Input Low Voltage	-	VSS	-	0.2VDD	V
VIHT	Input High Threshold Voltage	RESET	0.4VDD	-	-	V
VILT	Input Low Threshold Voltage	RESET	-		0.16VDD	V
VIHX	Clock Input High Voltage	OSCI	0.7VDD	-	-	V
VILX	Clock Input Low Voltage	OSCI	-		0.3VDD	V
VOH1	Output High Voltage (Port 8,9)	IOH = –1.26mA	0.8VDD	-	VDD	V
	(Port7)	IOH = –2.15mA	0.8VDD	-	VDD	V
VOL1	Output Low Voltage (Port 8,9)	IOL = 3.8mA	VSS	-	0.2VDD	V
	(Port 7)	IOL = 6.8mA	VSS	-	0.2VDD	V
Vlcd	LCD driver voltage	Ilcd = 0 uA	-	-	1.5VDD	V
		Ilcd = -150 uA	-	-	1.47VDD	V
IPH	Pull-high current	Pull-high active input pin at VSS	-	–8	–12	μA
ISB1	Power down current (SLEEP mode)	All input and I/O pin at VDD, output pin floating, WDT disabled. No load.	-	1	4	μA
ISB2	Power down current (IDLE mode)	All input and I/O pin at VDD, output pin are floating, WDT disabled, LCD disabled. No load.	-	15	25	μA
		All input and I/O pin at VDD, output pin are floating, WDT disabled, LCD enabled. No load.	-	45	75	μA
ISB3	Low clock current (GREEN mode)	CLK=32.768kHz, all input and I/O pin at VDD, output pin floating, WDT disabled, LCD enabled. No load.	-	50	80	μA
ICC	Operating supply current (NORMAL mode)	RESET=High, CLK=3.579MHz, output pin floating, LCD enabled. No load.	-	1.0	1.3	mA

9 AC Electrical Characteristics

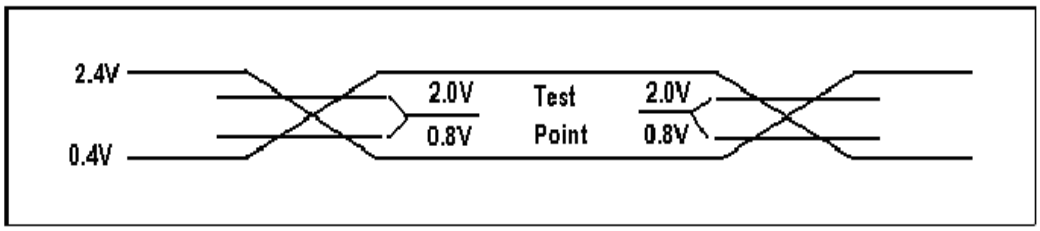
Ta=0℃ ~ 70℃, VDD=3V, VSS=0V

Symbol	Parameter	Conditions	Min	Type	Max	Unit
Dclk	Input CLK duty cycle		45	50	55	%
Tins	Instruction cycle time	32.768K 3.579M	-	60 550	-	μs ns
Tdrh	Device delay hold time		-	16	-	ms
Twdt	Watchdog timer period	Ta = 25°C		16		ms

Description	Symbol	Min	Type	Max	Unit
OSC start up (32.768Hz) (3.579MHz PLL)	Tosc	--		440 16	ms

10 Timing Diagram

AC test Input / Output Port Waveform



AC Testing : Input are driven at 2.4V for logic "1" , and 0.4V for logic "0".
Timing measurements are made at 2.0V for logic "1" , and 0.8V for logic "0".

Reset Timing

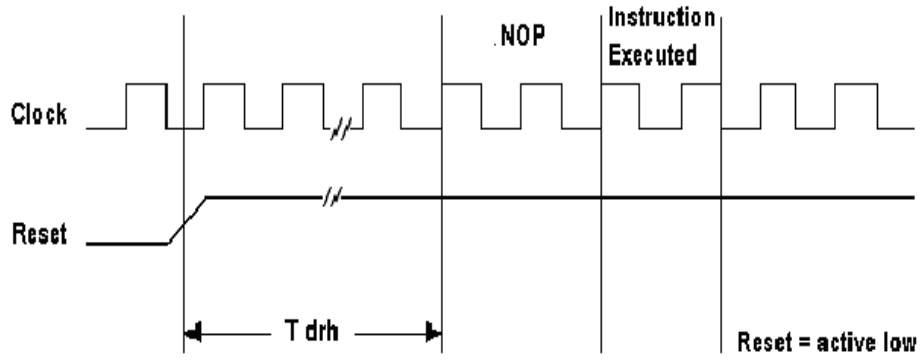


Fig. 14 AC Timing

11 Application Circuit

11.1 Application with Crystal Mode

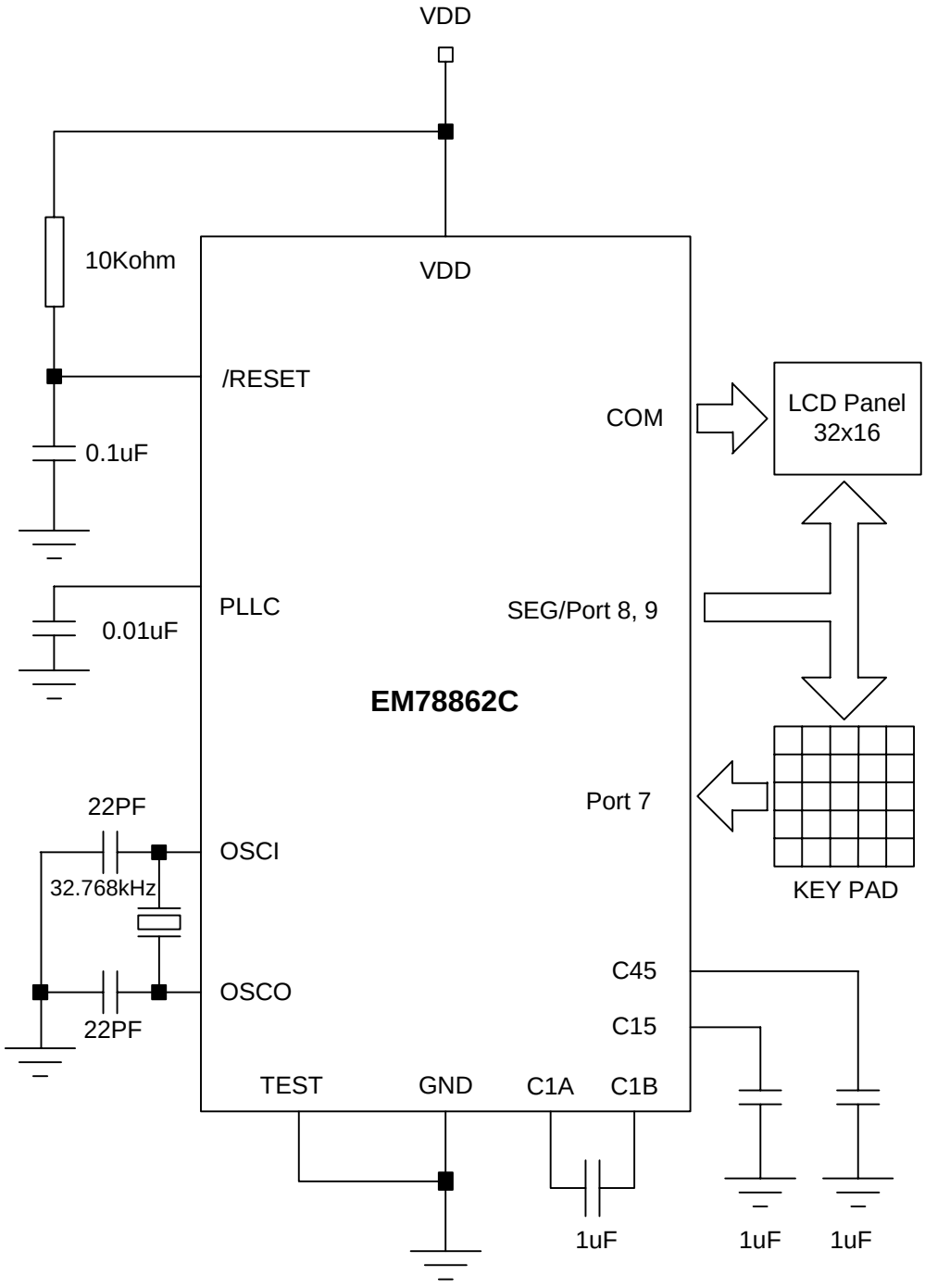


Fig. 15. Application with Crystal Mode

11.2 Application with RC Mode

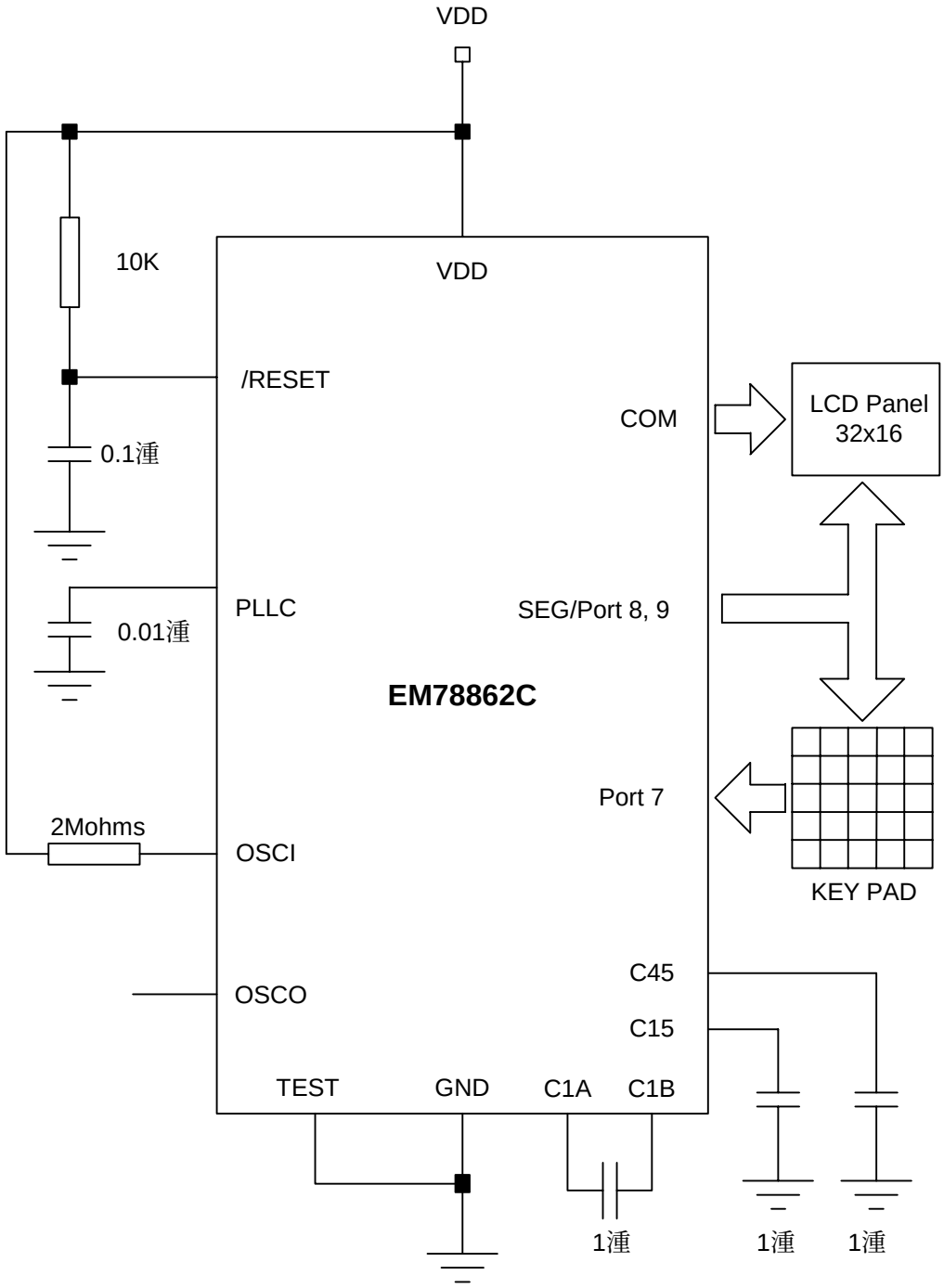


Fig. 16. Application with RC Mode

12 Bonding Coordinates Subsidiary

12.1 Pad Configuration

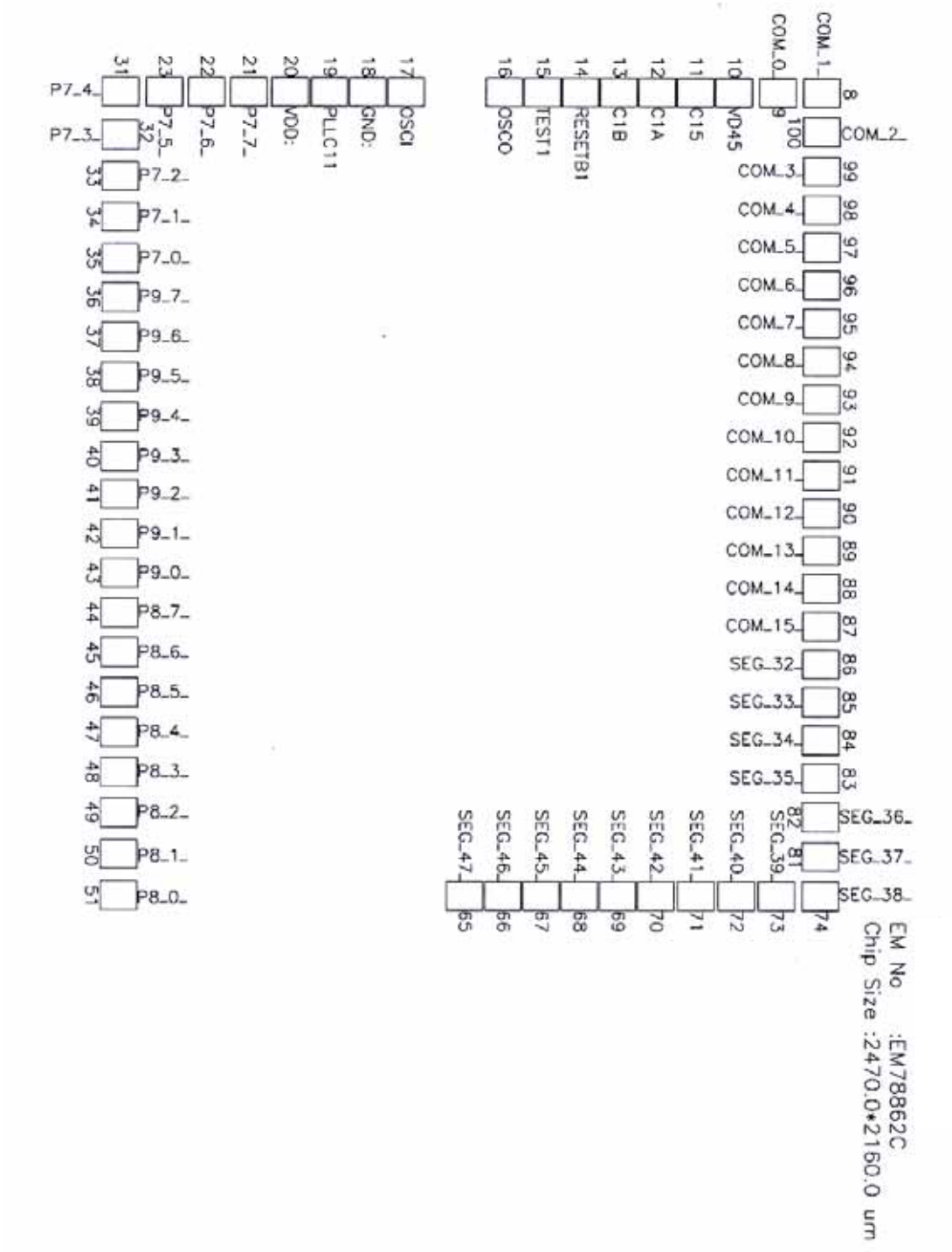


Fig. 17 ePV6300 Pad Configuration

12.2 Pad Name and Coordinates Table

Pad Name & Cordinates Table		
Chip Size:2470.0*2160.0 um		
Pin No	Pad Name	Coordinate (X , Y)
8	COM_1_	-1115.5, 960.5
9	COM_0_	-1115.5, 840.5
10	VD45	-1115.0, 719.5
11	C15	-1115.0, 614.5
12	C1A	-1115.0, 509.5
13	C1B	-1115.0, 404.5
14	RESETB1	-1115.0, 299.5
15	TEST1	-1115.0, 194.5
16	OSCO	-1115.0, 89.5
17	OSCI	-1115.0, -180.0
18	GND:	-1115.0, -285.0
19	PLLC11	-1115.0, -390.0
20	VDD:	-1115.0, -497.0
21	P7_7_	-1115.0, -610.0
22	P7_6_	-1115.0, -725.0
23	P7_5_	-1115.0, -840.0
31	P7_4_	-1115.0, -960.0
32	P7_3_	-995.0, -960.0
33	P7_2_	-880.0, -960.0
34	P7_1_	-765.0, -960.0
35	P7_0_	-650.0, -960.0
36	P9_7_	-542.55, -960.0
37	P9_6_	-432.55, -960.0
38	P9_5_	-322.55, -960.0
39	P9_4_	-212.55, -960.0

Pad Name & Cordinates Table		
Chip Size:2470.0*2160.0		
Pin No	Pad Name	Coordinate (X , Y)
40	P9_3_	-102.55, -960.0
41	P9_2_	2.45, -960.0
42	P9_1_	112.45, -960.0
43	P9_0_	222.45, -960.0
44	P8_7_	332.45, -960.0
45	P8_6_	442.45, -960.0
46	P8_5_	552.45, -960.0
47	P8_4_	662.45, -960.0
48	P8_3_	772.45, -960.0
49	P8_2_	885.0, -960.0
50	P8_1_	1000.0, -960.0
51	P8_0_	1115.0, -960.0
65	SEG_47_	1115.5, -14.5
66	SEG_46_	1115.5, 90.5
67	SEG_45_	1115.5, 195.5
68	SEG_44_	1115.5, 300.5
69	SEG_43_	1115.5, 405.5
70	SEG_42_	1115.5, 510.5
71	SEG_41_	1115.5, 620.5
72	SEG_40_	1115.5, 730.5
73	SEG_39_	1115.5, 840.5
74	SEG_38_	1115.5, 960.5
81	SEG_37_	1005.5, 960.5
82	SEG_36_	895.5, 960.5
83	SEG_35_	787.5, 960.5

Pad Name & Cordinates Table		
Chip Size:2470.0*2160.0 um		
Pin No	Pad Name	Coordinate (X , Y)
84	SEG_34_	682.5, 960.5
85	SEG_33_	577.5, 960.5
86	SEG_32_	472.5, 960.5
87	COM_15_	367.5, 960.5
88	COM_14_	262.5, 960.5
89	COM_13_	157.5, 960.5
90	COM_12_	52.5, 960.5
91	COM_11_	-52.5, 960.5
92	COM_10_	-157.5, 960.5
93	COM_9_	-262.5, 960.5
94	COM_8_	-367.5, 960.5
95	COM_7_	-472.5, 960.5
96	COM_6_	-577.5, 960.5
97	COM_5_	-682.5, 960.5
98	COM_4_	-787.5, 960.5
99	COM_3_	-895.5, 960.5
100	COM_2_	-1005.5, 960.5

Pad Name & Cordinates Table		
Chip Size:2470.0*2160.0		
Pin No	Pad Name	Coordinate (X , Y)