EP520 SDRAM Controller

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Features

- Supports Virtex™, Virtex™-E, and Spartan™-II FPGAs
- Supports industry standard SDRAM and PC100 SDRAM DIMM.
- Supports register mode and non-register mode PC100 SDRAM DIMM.
- Programmable memory size and data width.
- Supports industrial standard 16Mbit, 64Mbit, 128Mbit and 256Mbit SDRAMs.
- Supports burst size of 1 to 8 and full page burst.
- Supports zero wait state burst data transfer to maximize data bandwidth.
- Programmable SDRAM access timing parameters.
- Automatic refresh generation with programmable refresh intervals.
- Optional Error Correction Code (ECC).
- Multiple external SDRAM partitions.
- Supports external data buffer between user device and SDRAM data bus

AllianceCORE™ Facts

Core Specifics	
Supported Family	Virtex
Device Tested	V50-6
CLB Slices	287
Clock IOBs[1]	1
IOBs[1]	116
Performance (MHz)	91
Xilinx Tools	3.2i
Special Features	None
Provided with Core	
Documentation	User guide
Design File Formats	EDIF netlist
Constraints File	Top520.ucf
Verification	VHDL or Verilog test bench
Instantiation Templates	VHDL, Verilog
Reference designs & application notes	None
Additional Items	None
Simulation Tool Used	
Model Technology Modelsim™ 5.4b	
Support	
Support provided by Eureka Technology	

Notes:
1. Assuming all core I/Os are routed off-chip

Applications

- Networking equipment
- Communication equipment
- Video systems
- Image processing equipment
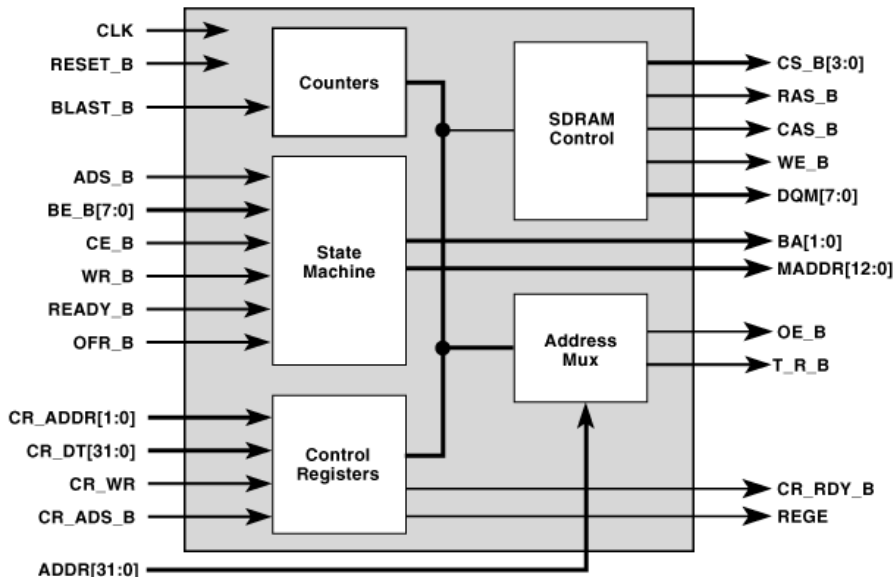- Medical equipment
- Avionics
- PC peripherals

Figure 1: EP520 SDRAM Controller Block Diagram

General Description

The EP520 SDRAM controller interfaces between a processor or DMA device with an SDRAM. It performs SDRAM read and write access based on processor or DMA requests.

SDRAM timing such as row and column latency, precharge timing, and row access length are automatically handled by the SDRAM controller. All these timing parameters are set by the SDRAM controller on system reset and can be programmed by the user during run time to optimize system performance.

The EP520 supports all industry standard SDRAM organizations, ranging from 16Mbit to 256Mbit devices, and from X4 data width to X16 data width. The user can use multiple SDRAMs to build access word size from16-bit to 64-bit wide, or use standard SDRAM DIMMs to build the memory system. The SDRAM size and word size are programmable by the memory controller.

Zero wait state data bursting is supported by the SDRAM controller to maximize data throughput. The back-end interface to user device such as CPU or DMA controller is a standard microprocessor bus with wait state control. It can be optimized easily to meet different application requirements.

Functional Description

The EP520 core is partitioned into modules as shown in Figure 1 and described below

State Machine

Based on the request signals ADS_B and CE_B, the state machine sends control signals to the Counters, Address Mux, and SDRAM control blocks to access to SDRAM. READY_B is asserted for each read data that is returned from the SDRAMs, or for each data that is written to the SDRAMs. If an access to the Control Registers block is requested on the CR_ADS_B input, the State Machine sends appropriate control signals to the Control Registers block to perform a register write.

SDRAM Control

The SDRAM control block generates the CS_B, CAS_B, RAS_B and WE_B signals and drives the appropriate address and DQM[7:0] at the proper timing.

Counters

Under the control of the state machine, the counters keep track of the burst length and various SDRAM timing parameters, such as RAS_B-to-CAS_B delay, active command-to-precharge time, etc, so that every command is issued at the correct timing. These timing parameters are programmable through the Control Registers.

Address Mux

The Address Mux takes the input address on ADDR[31:0] and drives the correct bank address on BA and row or column address on MADDR.

Control Registers

The user can program the SDRAM controller to support different SDRAM sizes, burst lengths, and SDRAM timing parameters. The registers are accessed through the control register access signals, CR_XX (all CR_ signals).

Core Modifications

The SDRAM controller is designed in the XCV50PQ240 device. Cores for other packages can also be supported. Eureka Technology will contract to modify the core to your specifications.

Pinout

The pinout of the EP520 core has not been fixed to specific FPGA I/O, thereby allowing flexibility with a user's application. Signal names are shown in Figure 1 and described in Table 2.

Verification Methods

Functional simulation has been done using Model Technology ModelsimTM 5.4b. Static timing analysis has been done for all paths using the timing analyzer in Xilinx Foundation Series 2.1i.Recommended Design Experience

The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment.

Recommended Design Experience

Users should have a basic knowledge about SDRAM and decide the target device.

Ordering Information

If you have inquiries or want to license our core, please contact Eureka Technology directly. Eureka Technology retains the right to make changes to these specifications at any time without notice.

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Table 1: Core Signal Pinout

Signal	Signal Direction	Description
ADDR[31:0]	Input	Address input
ADS_B	Input	Address strobe
BE_B[7:0]	Input	Byte enable
BLAST_B	Input	Burst last
CE_B	Input	Chip enable
CLK	Input	System clock
CR_ADR[1:0]	Input	Register address
CR_ADS_B	Input	Control register access
CR_DT[31:0]	Input	Register data
CR_RDY_B	Output	Control register ready
CR_WR	Input	Register write
OE_B	Output	Output enable
OFR_B	Output	Out of range
READY_B	Output	Ready
RESET_B	Input	System reset
T_R_B	Output	Transmit/Receive
WR	Input	Write enable
BA[1:0]	Output	Bank address
CAS_B	Output	Column address select
CS_B[3:0]	Output	Chip select
DQM[7:0]	Output	Data mask
MADDR[12:0]	Output	Memory address
RAS_B	Output	Row address select
REGE	Output	Register mode select
WE_B	Output	Write enable

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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