SUMITOMO ELECTRIC

Advance

02.07.30

F0532506Q

3.3 V 2.5 Gb/s NRZ Data Rate

Laser Diode Driver

♦ *Features*

- Up to 2.5 Gb/s high speed operation
- Clocked (MS-D/FF) or Non-clocked operation can be selected
- Disable function of modulation current and bias current
- Bias current monitoring
- 3.3 V or - 3.3 V single Voltage Supply operation
- Up to 50 mA modulation current
- Up to 50 mA bias current
- Differential ECL compatible interface
- On-chip 50 Ω terminations
- Internal voltage reference for AC coupling

♦ *Applications*

- Laser diode driver of an optical transmitter circuit up to 2.5 Gb/s

♦ *Functional Description*

The F0532506Q is a high performance GaAs laser diode driver IC applicable in an optical transmitter circuit up to 2.5 Gb/s NRZ data rate (especially suitable for SDH [STM-16] / SONET [OC-48]).

The F0532506Q specifies the rise time and the fall time of 80 ps (20 % - 80 %, 25 Ω load) typically. It features the single +3.3 V or - 3.3 V supply operation, the modulation current between 4 mA and 50 mA, and the bias current between 4 mA and 50 mA.

♦ *Absolute Maximum Ratings*

Ta=25°C, unless specified.

Parameter	Symbol	Value	Units
Supply Voltage	V_{DD} - V_{SS}	- 0.3 to +4.0V	V
Supply Current *1	I_{CC}	200	mA
Input Voltage (D_{IN}, D_{INB}, CK_{IN},CK_{INB})	V_{IN}	V_{DD} - 2.5 to V_{DD}	V
Input Voltage (DIS_{IN}, SEL_{IN})	V_{INC1}	V_{SS} to V_{DD} + 0.5	V
Input Voltage (V_{M1}, V_{B1})	V_{INC2}	V_{SS} to V_{SS} + 1.7	V
Input Voltage (V_{M0}, V_{B0})	V_{INC3}	V_{SS} to V_{SS} + 0.7	V
Input Voltage (V_{REG})	V_{INC4}	V_{SS} to V_{DD}	V
Output Voltage (OUT, OUT_B, OUT_{BIAS})	V_{OUT}	V_{DD} - 2.0 to V_{DD} + 0.5	V
Output Current (OUT, OUT_B, OUT_{BIAS})	I_{OUT}	0 to 70	mA
Output Voltage (BM, BM_B)	V_{OUTM}	V_{SS} to V_{DD} + 0.5	V
Termination Voltage (V_{TTD}, V_{TTCK})	V_{TT}	V_{DD} - 2.5 to V_{DD} + 0.5	V
Storage Temperature	Tstg	- 55 to + 125	°C
Ambient Operating Temperature	T_a	0 to + 70	°C

*1 Excluding the input current, the modulation current and the bias current.

♦ *Recommended Operating Conditions*

Parameter	Symbol	Value			Units
		Min.	Typ.	Max.	
Supply Voltage	V_{DD} - V_{SS}	3.10	3.30	3.50	V
Ambient Operating Temperature	T_a	0	25	70	°C

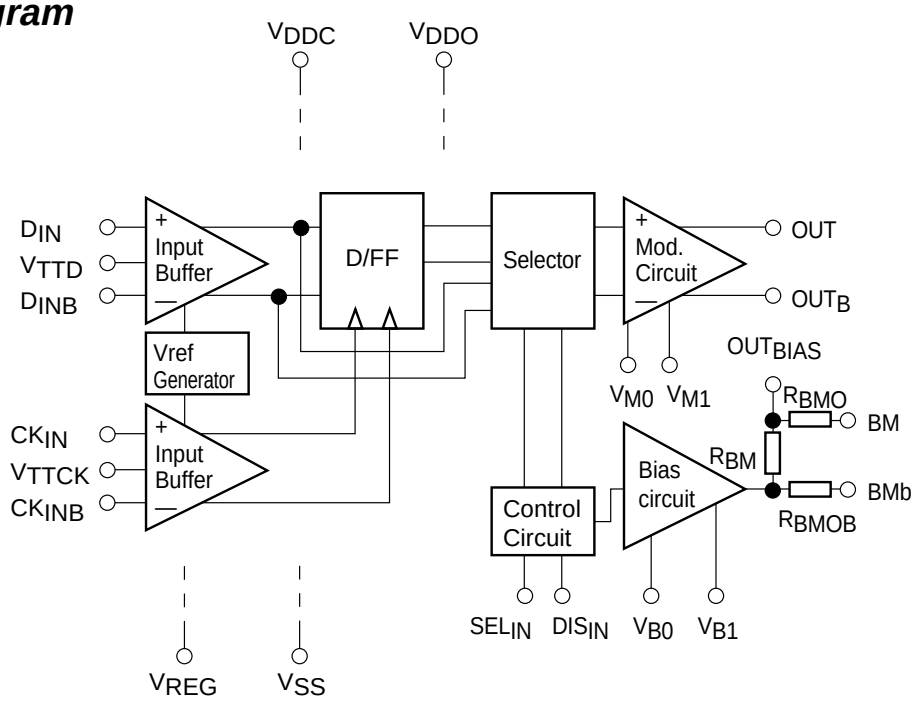
♦ *Electrical Characteristics*

Ta=25°C, V_{DD}- V_{SS} = 3.1 V to 3.5 V, V_{SS}=0 V, unless specified

Parameters	Symbol	Test Conditions	Value			Units
			Min.	Typ.	Max.	
Circuit Current *1	I_{CKT}	DC	-	80	115	mA
Input Voltage (ECL Interface)	V_{IH}	Differential Input	V_{DD} - 1.0	V_{DD} - 0.9	V_{DD} -0.7	V
	V_{IL}		V_{DD}- 1.9	V_{DD} - 1.7	V_{DD} - 1.6	V
Input Voltage (AC coupled interface)	V_{IN}	Differential Input	0.3	0.8	1.2	VP-P
Input Resistor	R_{IN}	-	-	50	-	Ω
Modulation Peak Current	I_{MMAX}	-	50	-	-	mA
	I_{MMIN}	V_{M1} =V_{SS}	-	-	4	mA
	I_{MDIS}	V_{DISIN} =V_{DD} - 0.2 V	-	-	1	mA
Bias Current	I_{BMAX}	-	50	-	-	mA
	I_{BMIN}	V_{B1} =V_{SS}	-	-	4	mA
	I_{BDIS}	V_{DISIN} =V_{DD} - 0.2 V	-	-	1	mA
Input Voltage (DIS)	V_{DISIH}	Disable operation	V_{DD} - 0.2	-	V_{DD}	mA
	V_{DISIL}	Enable operation	V_{SS}	OPEN	V_{SS}+0.2	mA
Input Voltage (SEL)	V_{SELIH}	Non - Clocked op.	V_{DD} - 0.2	-	V_{DD}	mA
	V_{SELIL}	Clocked operation	V_{SS}	OPEN	V_{SS} + 0.2	mA
Bias Monitor Resistor	R_{BM}		-	5	-	Ω
Rise Time	tr	RL = 25 Ω 20% - 80%	-	80	-	ps
Fall Time	tf	RL = 25 Ω 20% - 80%	-	80	-	ps
Setup Time	ts		-	100	-	ps
Hold Time	th		-	50	-	ps
Maximum Clock Frequency	fmax	V_{SEL}=OPEN or V_{DD} - 0.2 V to V_{DD}	2.5	-	-	GHz
Maximum Data Rate	fopr	V_{SEL}= V_{DD} - 0.2 V to V_{DD}	2.5	-	-	Gbps

*1 Excluding the input current, the modulation current and the bias current.

♦ *Block Diagram*



♦ *Pin Descriptions*

Symbol	Description
V_{DDC}	Supply Voltage. V_{DDC} and V_{DDO} are not connected internally.
V_{DDO}	Supply Voltage.
V_{SS}	Supply Voltage.
D_{IN}	Positive data input
D_{INB}	Negative data input
V_{TTD}	Termination data input
CK_{IN}	Positive clock input
CK_{INB}	Negative clock input
V_{TTCK}	Termination for clock input
OUT	Positive modulation output (LD should be connected to this pin.)
OUT_B	Negative modulation output
OUT_{BIAS}	Bias output. (RBM = 5 Ω typ., R_{BMO}=R_{BMOB} = 3 kΩ typ.)
V_{M0}, V_{M1}	Voltage input that sets the LD modulation peak current. V_{M0} and V_{M1} have different control characteristic. If one pin is used, the other must be opened.
V_{B0}, V_{B1}	Voltage input that sets the LD bias current. V_{B0} and V_{B1} have different control characteristic. If one pin is used, the other must be opened.
DIS_{IN}	Voltage input that controls turning on/off modulation current and the bias current
SEL_{IN}	Voltage input that selects clocked or non-clocked operation
BM	Bias current monitor positive output
BM_b	Bias current monitor negative output
V_{REG}	Voltage input that regulate circuit current

♦ *Function Table*

(1) Clocked Operation (V_{IN}@SEL_{IN}=OPEN or V_{SS} to V_{SS}+0.2 V)

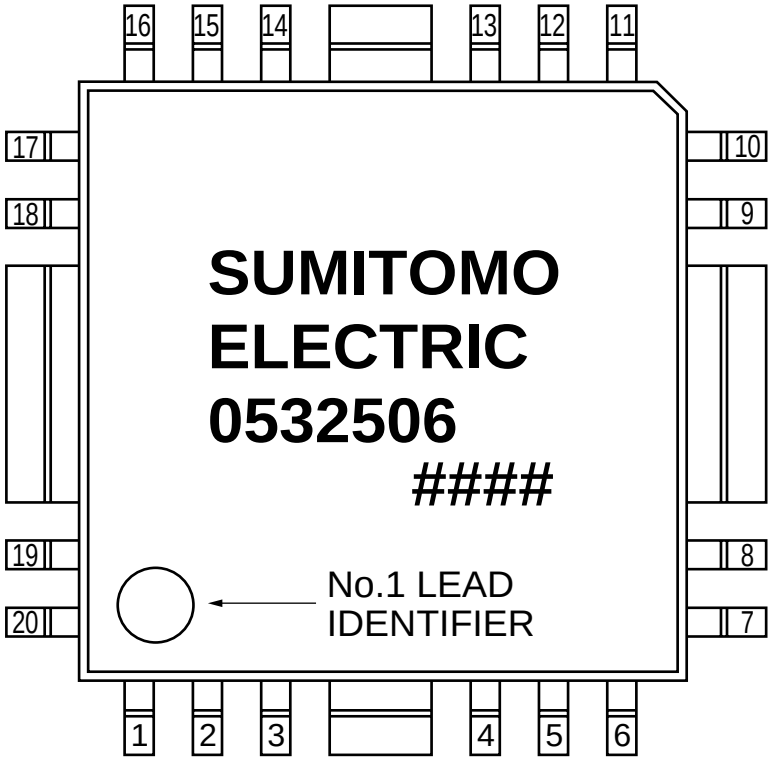
Input		Output	
D_{IN}	CK_{IN}	Current @ OUT	Current @ OUT
H	↑	ON	OFF
L	↑	OFF	ON
Φ	↓	Q_O	Q_{OB}

↓ : Clock transition from high to low
↑ : Clock transition from low to high
Φ : Don't care
Q_O : Previous current output status @ OUT before clock pulse
Q_{OB} : Previous current output status @ OUTB before clock pulse

(2) Non-clocked Operation (V_{IN}@SEL_{IN}=V_{DD}-0.2 V to V_{DD})

Input		Output	
D_{IN}	CK_{IN}	Current @OUT	Current @OUTB
H	Φ	ON	OFF
L	Φ	OFF	ON

♦ *Pin Assignments (Top View)*

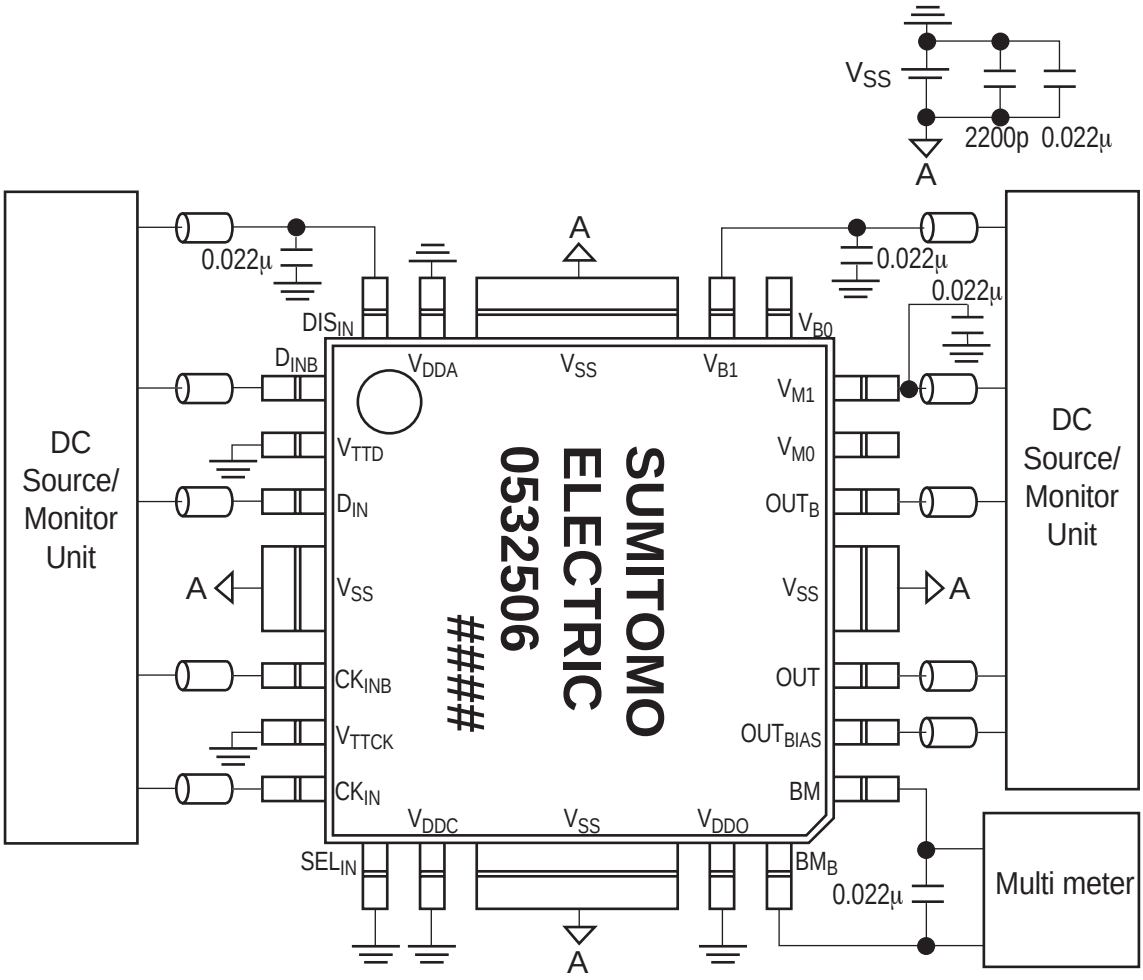


1 :D_{INB}
2 :V_{TTD}
3 :D_{IN}
4 :CK_{IN}
5 :V_{TTCK}
6 :CK_{INB}
7 :SEL_{IN}
8 :V_{DDC}
9 :V_{DDO}
10 :BM_B
11 :BM
12 :OUT_{BIAS}
13 :OUT
14 :OUT_B
15 :V_{M0}
16 :V_{M1}
17 :V_{B0}
18 :V_{B1}
19 :V_{DDA}
20 :DIS_{IN}

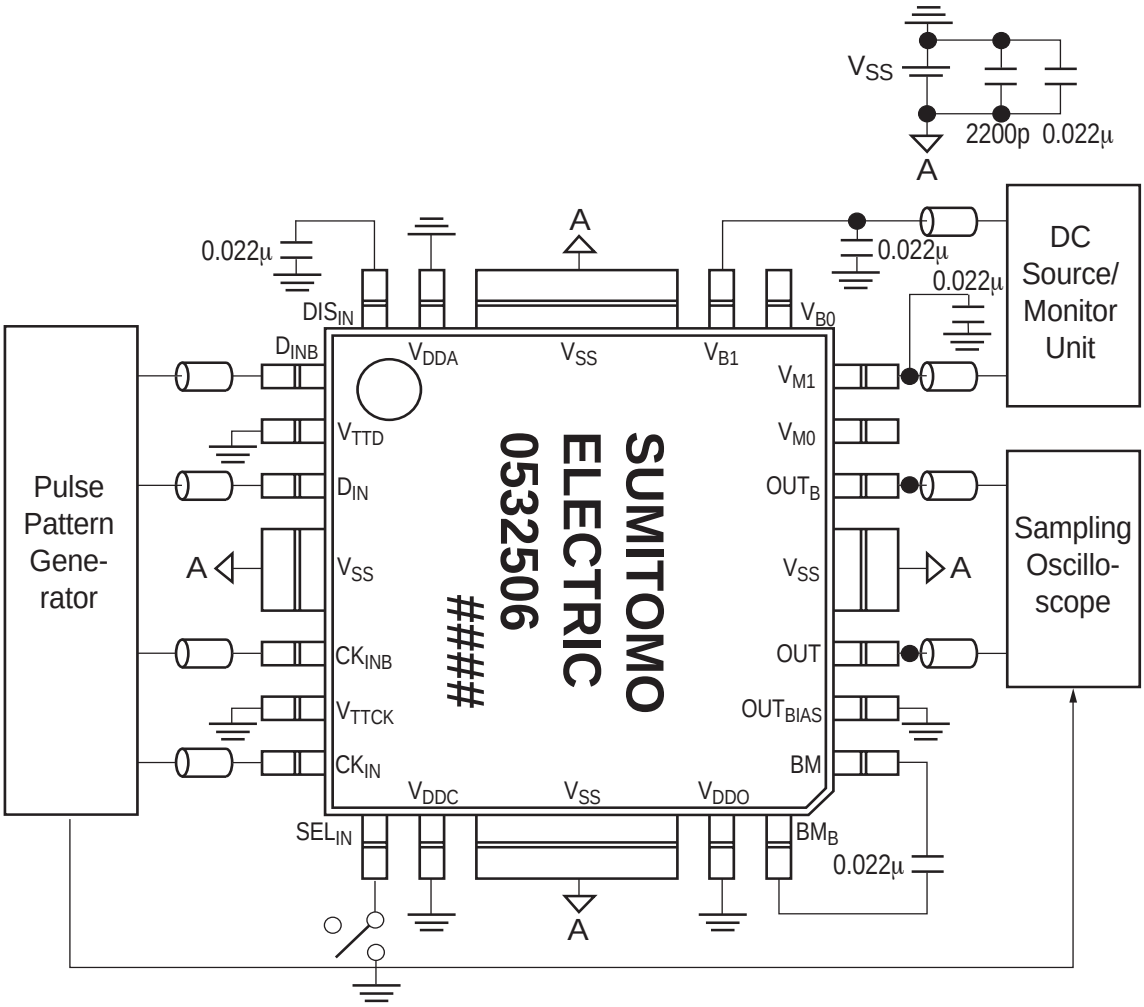
(Note) The pins without numbering should be connected to V_{SS}.
V_{DDA} ,V_{DDC} and V_{DDO} are not connected internally.

♦ *Test Circuits*

(1) DC Characteristics



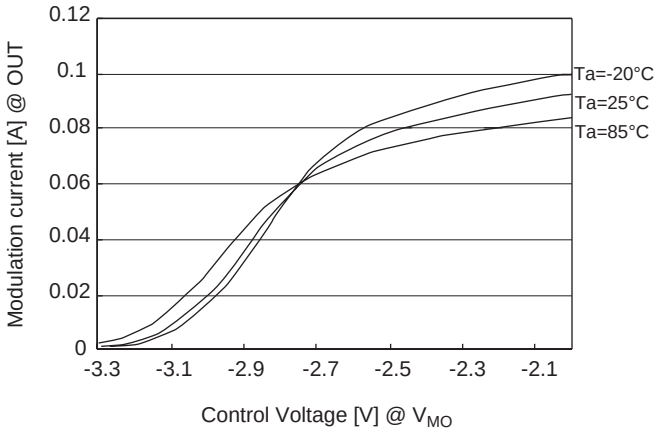
(2) AC Characteristics



♦ *Typical Characteristics*

(1) Modulation Current

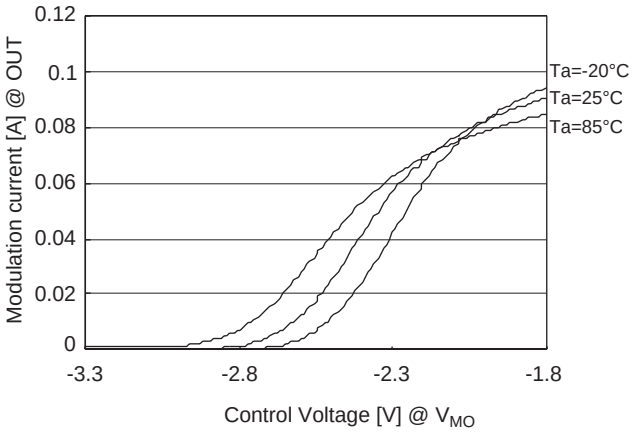
Modulation Current vs VM0



Conditions

V_{OUT}@OUT=GND, V_{DD}=GND, V_{SS}=-3.3V
V_{IN}@D_{IN}=-1.0V, V_{IN}@D_{INB}=-1.6V
V_{OUT}@OUTB, OUT_{BIAS}=GND
V_{M1}=Open

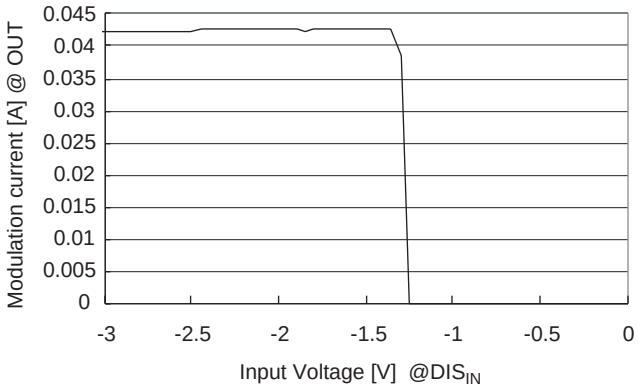
Modulation Current vs VM1



Conditions

V_{OUT}@OUT=GND, V_{DD}=GND, V_{SS}=-3.3V
V_{IN}@D_{IN}=-1.0V, V_{IN}@D_{INB}=-1.6V
V_{OUT}@OUTB, OUT_{BIAS}=GND
V_{M1}=Open

Modulation Current vs DIS_{IN}

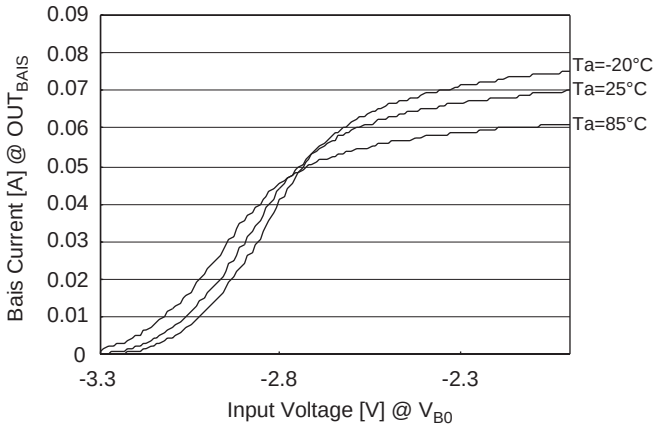


Conditions

V_{OUT}@OUT=GND, V_{DD}=GND, V_{SS}=-3.3V
V_{IN}@D_{IN}=-1.0V, V_{IN}@D_{INB}=-1.6V
V_{OUT}@OUTB, OUT_{BIAS}=GND
Ta=25°C

(2) Bias Current

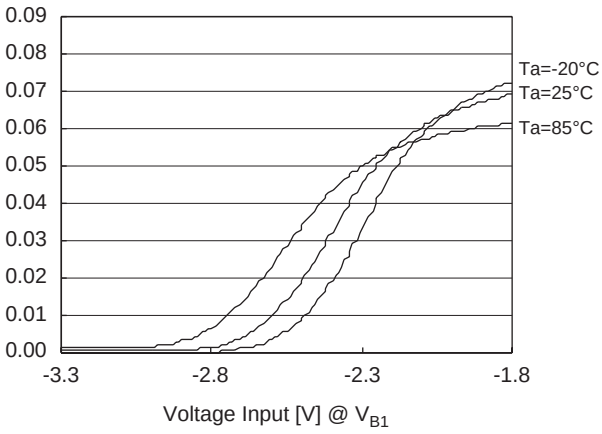
Bias Current vs V_{B0}



Conditions

V_{OUT}@OUT_{BIAS}=GND, V_{DD}=GND, V_{SS}=-3.3V
V_{IN}@D_{IN}=-1.0V, V_{IN}@D_{INB}=-1.6V
V_{OUT}@OUT, OUTB=GND
V_{B1}=Open

Bias Current vs V_{B1}



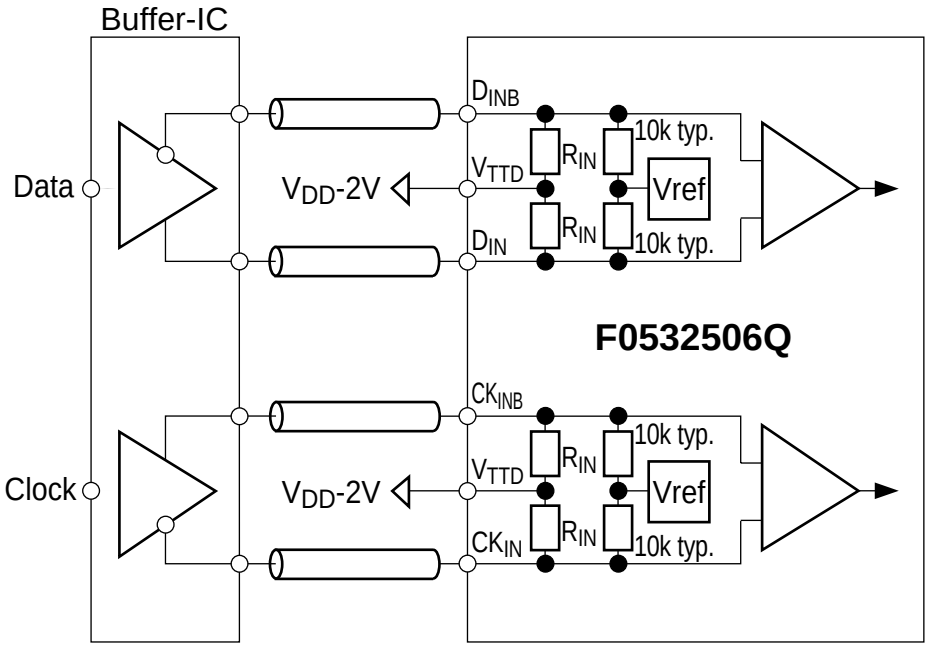
Conditions

V_{OUT}@OUT_{BIAS}=GND, V_{DD}=GND, V_{SS}=-3.3V
V_{IN}@D_{IN}=-1.0V, V_{IN}@D_{INB}=-1.6V
V_{OUT}@OUT, OUTB=GND
V_{B0}=Open

♦ *Application Guide*

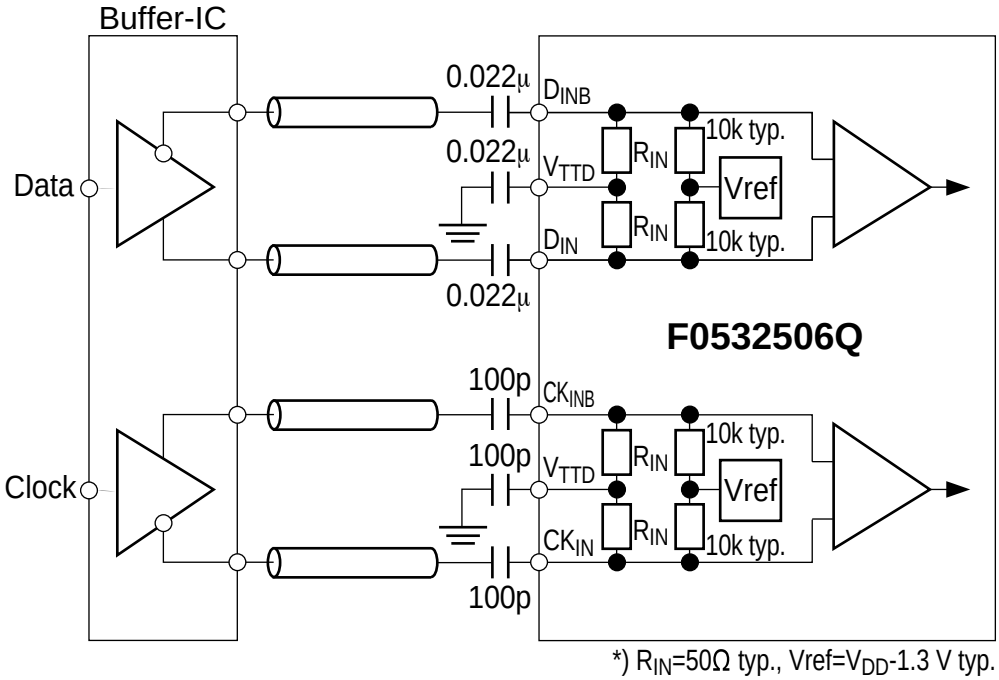
(1) Data and Clock Input Interface

(a) Differential ECL (or PECL) Interface



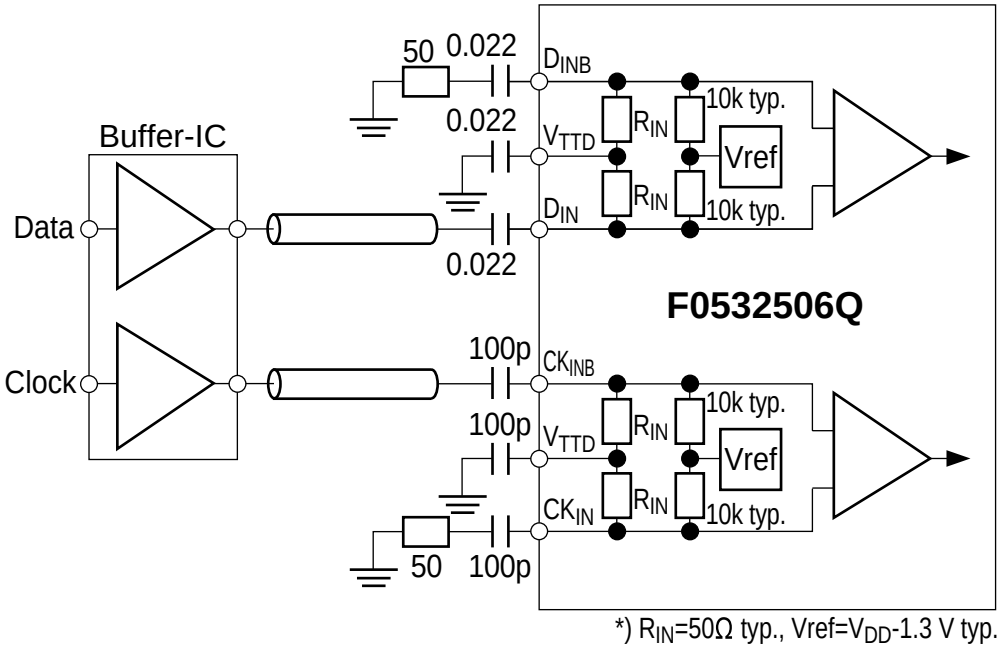
*) R_{IN}=50Ω typ., Vref=V_{DD}-1.3 V typ.

(b) Differential AC Coupled Interface



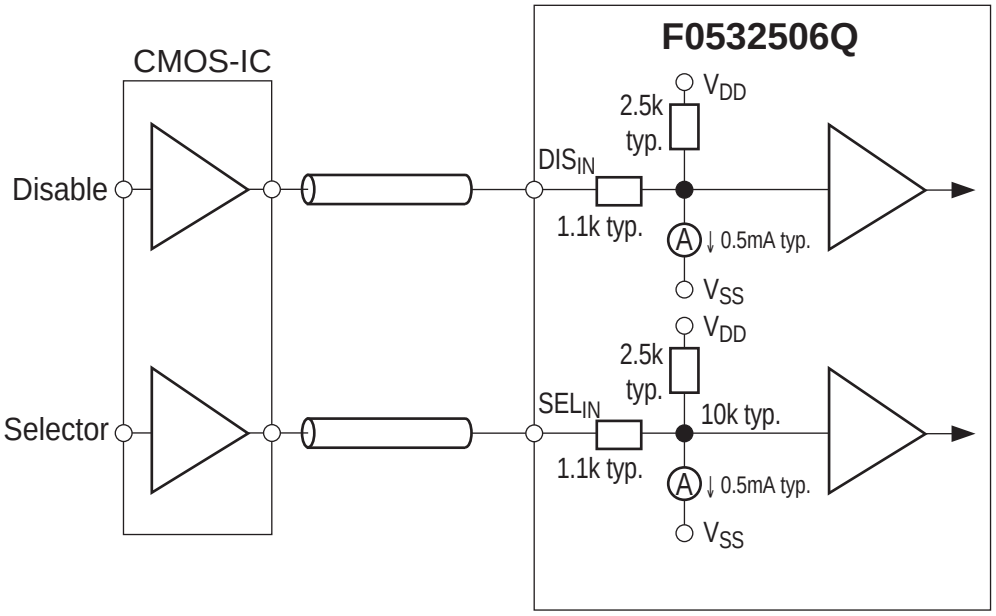
*) R_{IN}=50Ω typ., Vref=V_{DD}-1.3 V typ.

(c) Single-Ended AC Coupled Interface

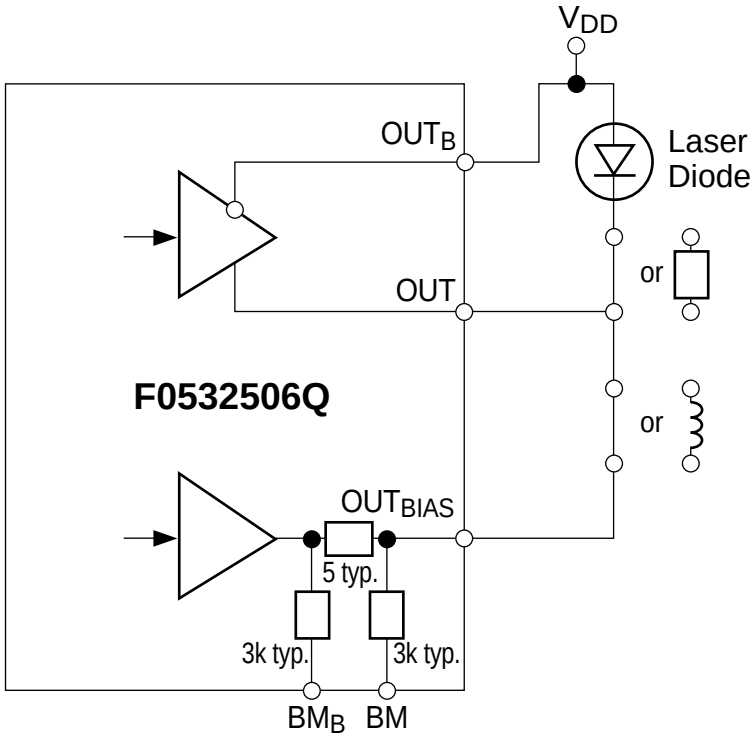


*) R_{IN}=50Ω typ., Vref=V_{DD}-1.3 V typ.

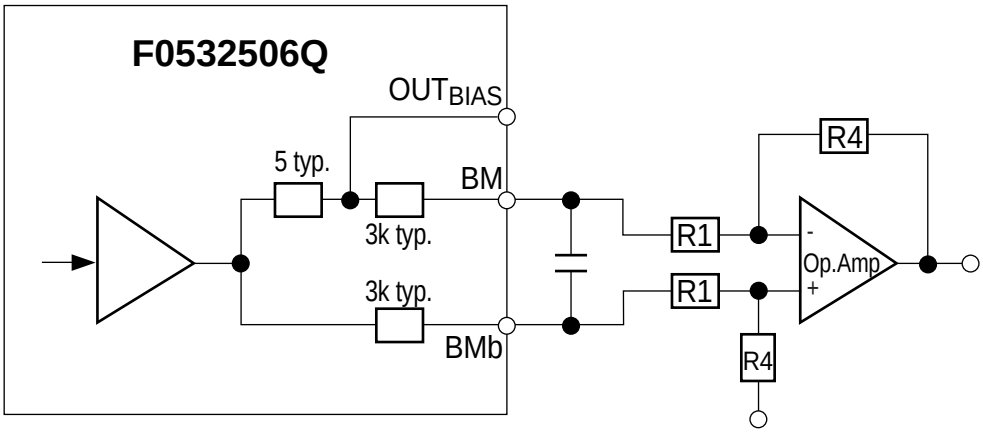
(2) Disable Input and Selector Input Interface



(3) Current Output Interface

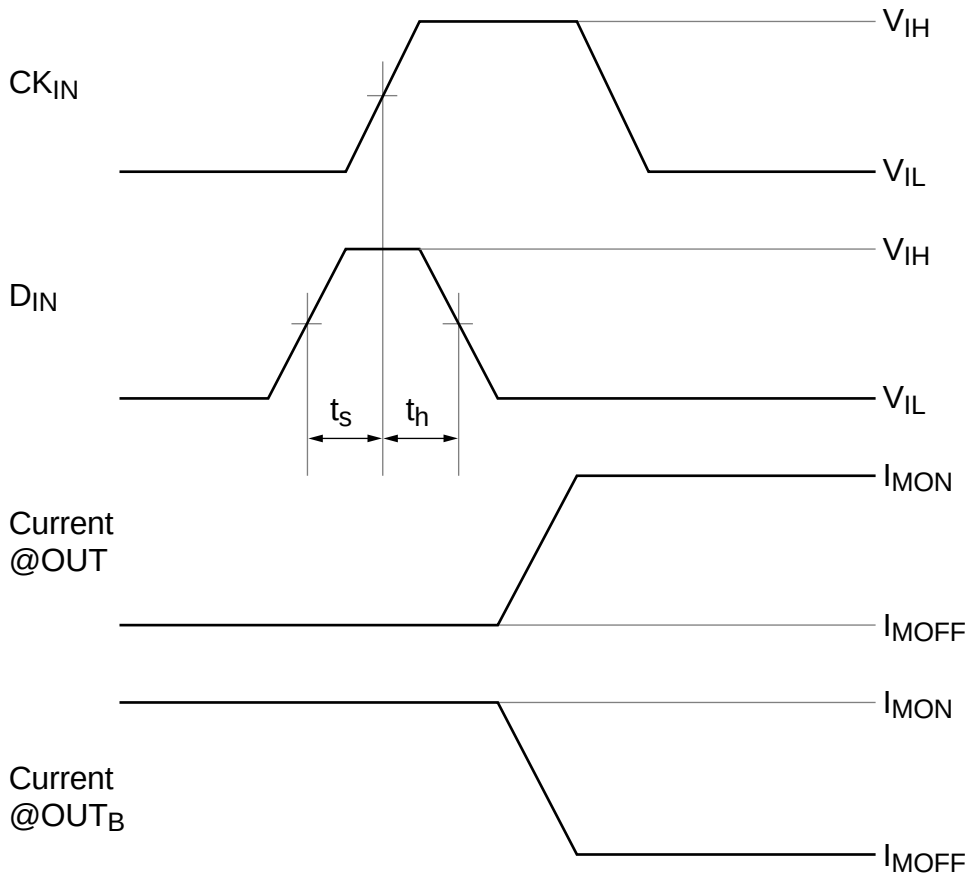


(4) Bias Current Monitor

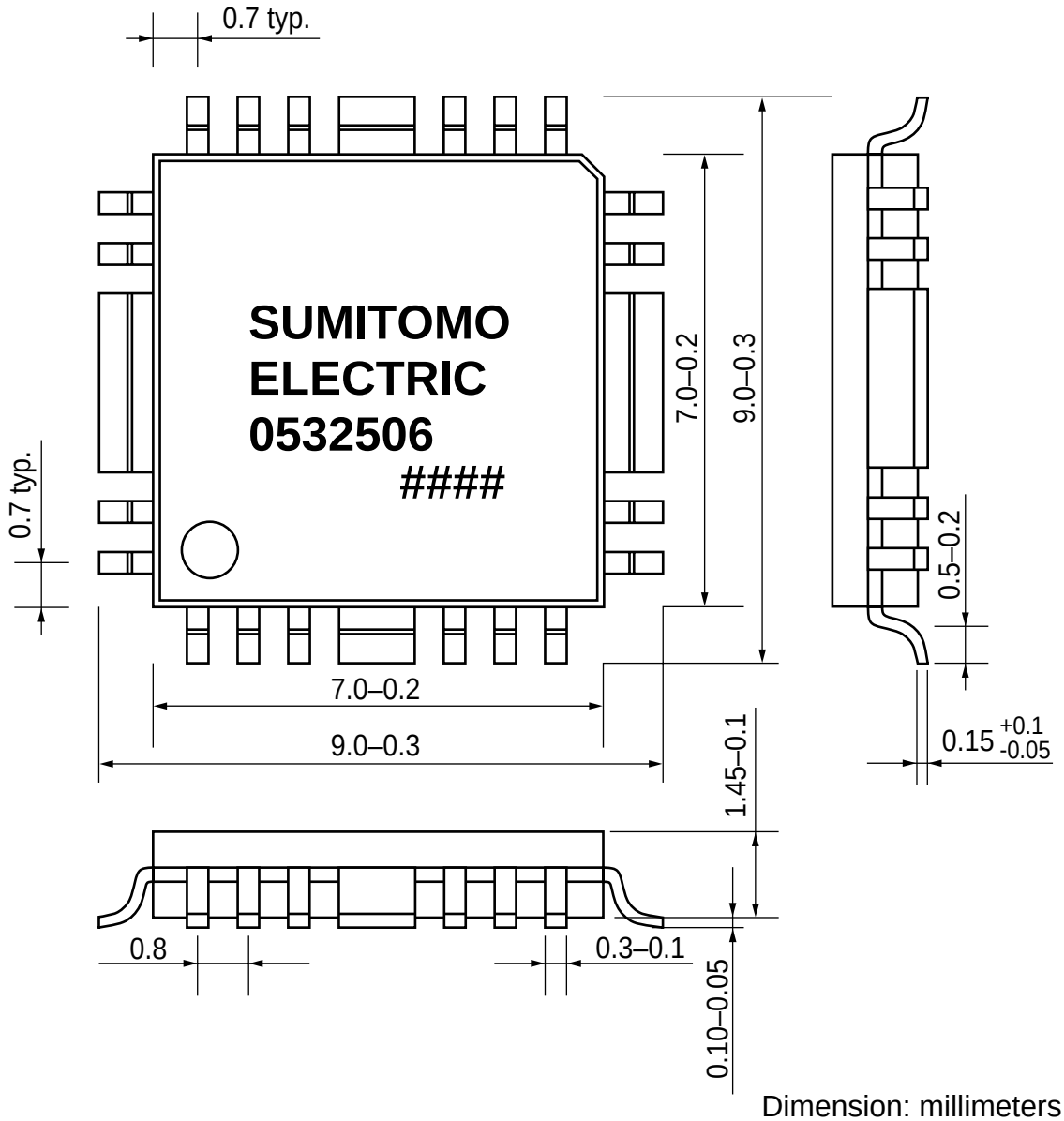


*) Value of R1 to R4 should be enough larger than 25Ω.
Recommended value is 100K to 200 KΩ.

(5) Timing Chart



♦ *Package Drawings*



Dimension: millimeters