

FDJ1027P

P-Channel 1.8V Specified PowerTrench® MOSFET

Features

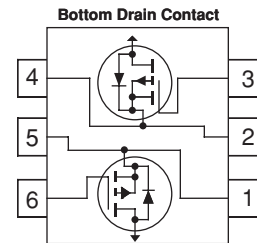
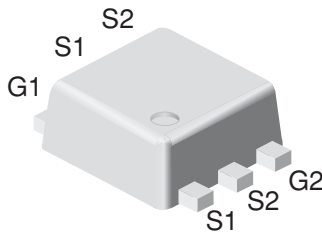
- -2.8 A, -20 V $R_{DS(ON)} = 160\text{ m}\Omega @ V_{GS} = -4.5\text{ V}$
 $R_{DS(ON)} = 230\text{ m}\Omega @ V_{GS} = -2.5\text{ V}$
 $R_{DS(ON)} = 390\text{ m}\Omega @ V_{GS} = -1.8\text{ V}$
- Low gate charge, High Power and Current handling capability
- High performance trench technology for extremely low $R_{DS(ON)}$
- FLMP SC75 package: Enhanced thermal performance in industry-standard package size

General Description

This dual P-Channel 1.8V specified MOSFET uses Fairchild's advanced low voltage PowerTrench process. Packaged in FLMP SC75, the $R_{DS(ON)}$ and thermal properties of the device are optimized for battery power management applications.

Applications

- Battery management/Charger Application
- Load switch



MOSFET Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Ratings | Units |
|--------------------------------|---|-------------|---------------------------|
| V_{DSS} | Drain-Source Voltage | -20 | V |
| V_{GSS} | Gate-Source Voltage | ± 8 | V |
| I_D | Drain Current – Continuous (Note 1a) | -2.8 | A |
| | | – Pulsed | |
| P_D | Power Dissipation for Single Operation (Note 1a) | 1.5 | W |
| | | (Note 1b) | |
| T_J, T_{stg} | Operating and Storage Junction Temperature Range | -55 to +150 | $^\circ\text{C}$ |
| Thermal Characteristics | | | |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient (Note 1a) | 80 | $^\circ\text{C}/\text{W}$ |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | 5 | |

Package Marking and Ordering Information

| | | | | |
|----|----------|----|-----|------------|
| .G | FDJ1027P | 7" | 8mm | 3000 units |
|----|----------|----|-----|------------|

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

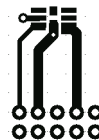
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|------|--------------------------|--------------------------|----------------------|
| Off Characteristics | | | | | | |
| BV_{DSS} | Drain-Source Breakdown Voltage | $V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$ | -20 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = -250\ \mu\text{A}$, Referenced to 25°C | | -13 | | mV/ $^\circ\text{C}$ |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$ | | | -1 | μA |
| I_{GSS} | Gate-Body Leakage | $V_{GS} = \pm 8\text{ V}, V_{DS} = 0\text{ V}$ | | | ± 100 | nA |
| On Characteristics (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$ | -0.4 | -0.8 | -1.5 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D = -250\ \mu\text{A}$, Referenced to 25°C | | 3 | | mV/ $^\circ\text{C}$ |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS} = -4.5\text{ V}, I_D = -2.8\text{ A}$ $V_{GS} = -2.5\text{ V}, I_D = -2.2\text{ A}$ $V_{GS} = -1.8\text{ V}, I_D = -1.7\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -2.8\text{ A}, T_J = 125^\circ\text{C}$ | | 108 163 283 150 | 160 230 390 238 | m Ω |
| g_{FS} | Forward Transconductance | $V_{DS} = -5\text{ V}, I_D = -2.8\text{ A}$ | | 5 | | S |
| Dynamic Characteristics | | | | | | |
| C_{iss} | Input Capacitance | $V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$ | | 290 | | pF |
| C_{oss} | Output Capacitance | | | 55 | | pF |
| C_{rss} | Reverse Transfer Capacitance | | | 29 | | pF |
| R_g | Gate Resistance | $f = 1.0\text{ MHz}$ | | 13 | | Ω |
| Switching Characteristics (Note 2) | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD} = -10\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$ | | 8 | 16 | ns |
| t_r | Turn-On Rise Time | | | 13 | 23 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 13 | 23 | ns |
| t_f | Turn-Off Fall Time | | | 18 | 32 | ns |
| Q_g | Total Gate Charge | $V_{DS} = -10\text{ V}, I_D = -2.8\text{ A},$ $V_{GS} = -4.5\text{ V}$ | | 3 | 4 | nC |
| Q_{gs} | Gate-Source Charge | | | 0.65 | | nC |
| Q_{gd} | Gate-Drain Charge | | | 0.75 | | nC |
| Drain-Source Diode Characteristics and Maximum Ratings | | | | | | |
| I_S | Maximum Continuous Drain-Source Diode Forward Current | | | | -1.25 | A |
| V_{SD} | Drain-Source Diode Forward Voltage | $V_{GS} = 0\text{ V}, I_S = -1.25\text{ A}$ (Note 2) | | -0.8 | -1.2 | V |
| t_{rr} | Diode Reverse Recovery Time | $I_F = -2.8\text{ A},$ $d_{IF}/d_t = 100\text{ A}/\mu\text{s}$ | | 14 | | ns |
| Q_{rr} | Diode Reverse Recovery Charge | | | 4 | | nC |

Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 80°C/W when mounted on a 1 in^2 pad of 2 oz copper (Single Operation).



b) 140°C/W when mounted on a minimum pad of 2 oz copper (Single Operation).

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width < $300\ \mu\text{s}$, Duty Cycle < 2.0%

Typical Characteristics

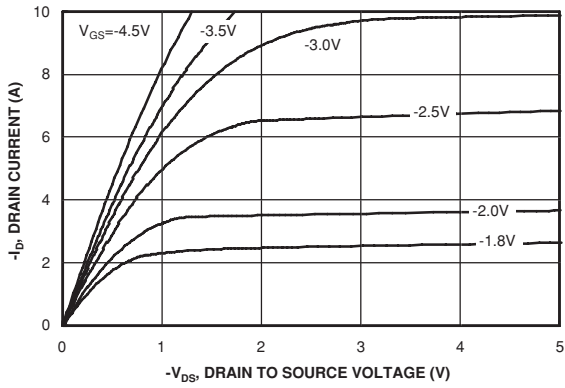


Figure 1. On-Region Characteristics.

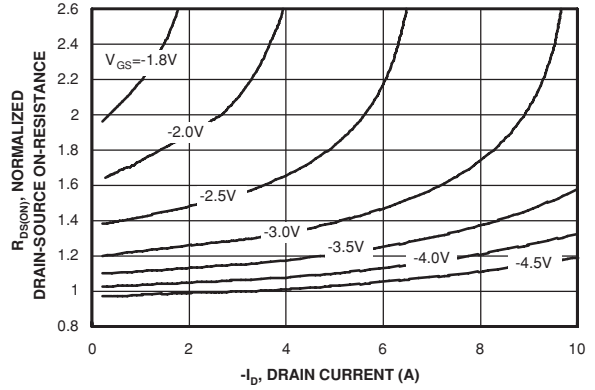


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

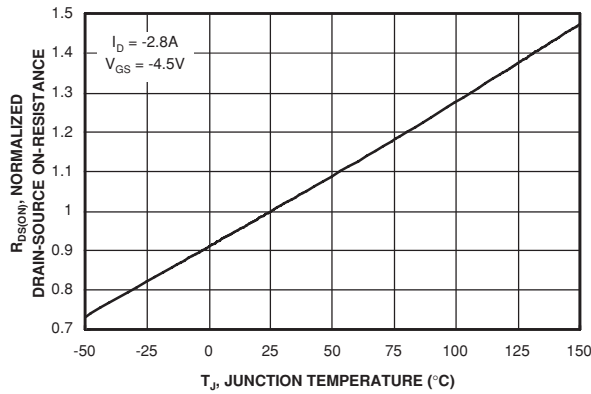


Figure 3. On-Resistance Variation with Temperature.

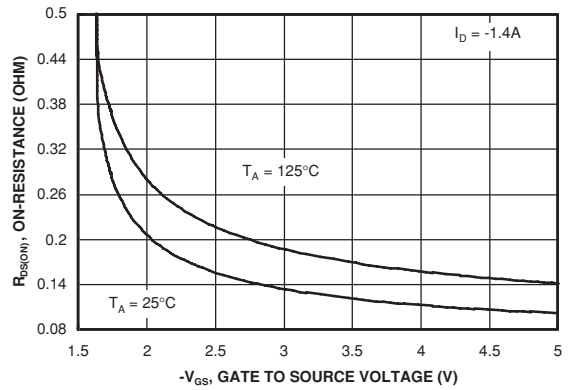


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

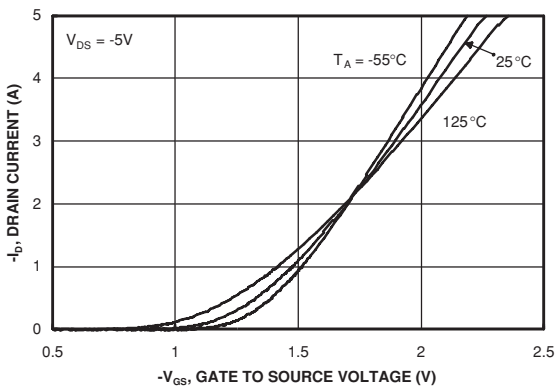


Figure 5. Transfer Characteristics.

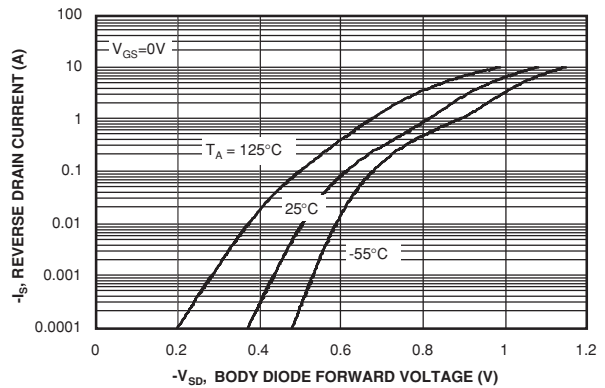


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

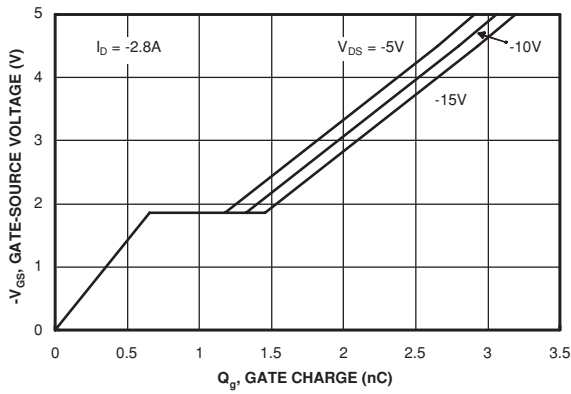


Figure 7. Gate Charge Characteristics.

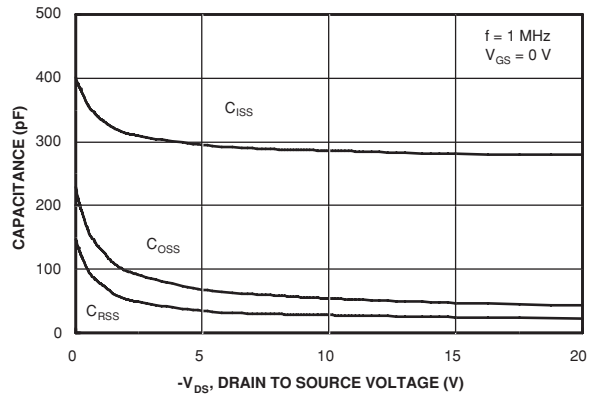


Figure 8. Capacitance Characteristics.

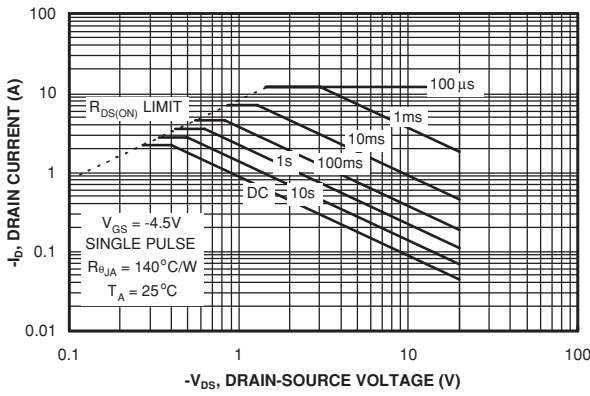


Figure 9. Maximum Safe Operating Area.

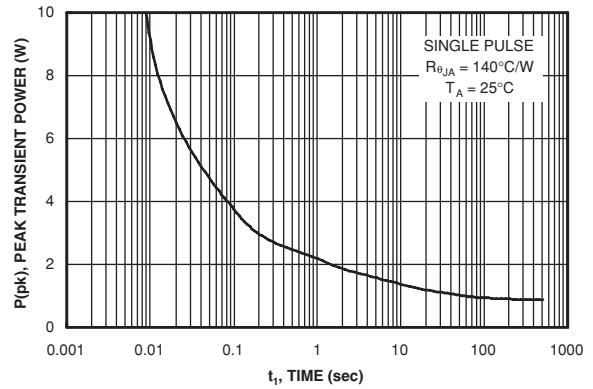


Figure 10. Single Pulse Maximum Power Dissipation.

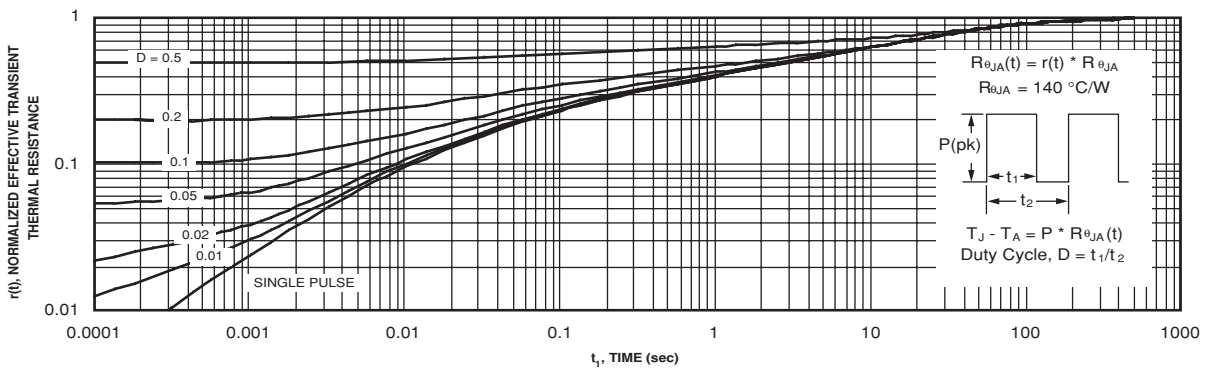
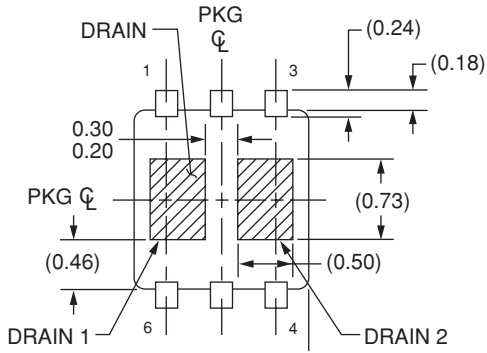


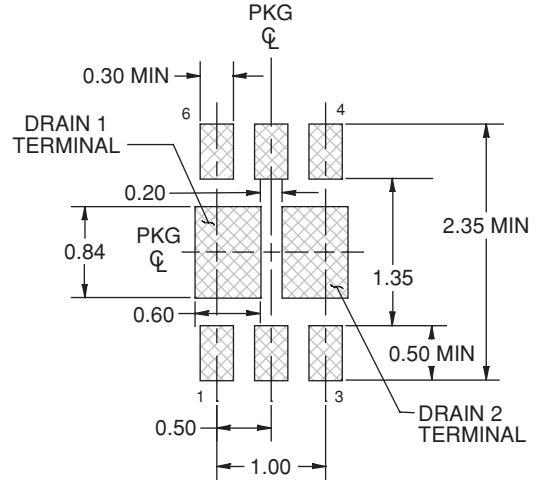
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

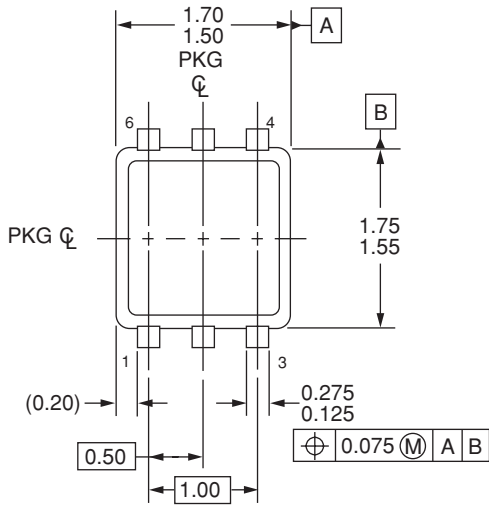
Dimensional Outline and Pad Layout



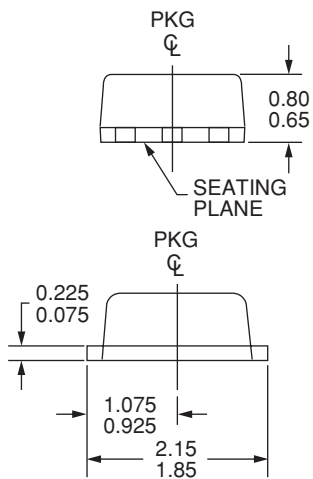
Bottom View



Recommended Landing Pattern



Top View



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