

October 2006

# FDMB3800N Dual N-Channel PowerTrench MOSFET 30V, 4.8A, $40m\Omega$

### **Features**

- Max  $r_{DS(on)}$  = 40m $\Omega$  at  $V_{GS}$  = 10V,  $I_D$  = 4.8A
- Max  $r_{DS(on)}$  = 51m $\Omega$  at  $V_{GS}$  = 4.5V,  $I_D$  = 4.3A
- Fast switching speed
- Low gate Charge
- High performance trench technology for extremely low r<sub>DS(on)</sub>
- High power and current handling capability.
- RoHS Compliant



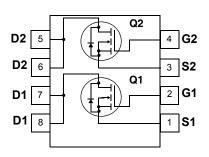
### **General Description**

These N-Channel Logic Level MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.



MicroFET 3X1.9



### MOSFET Maximum Ratings T<sub>A</sub> = 25°C unless otherwise noted

Symbol		Parameter Ratings				
$V_{DS}$	Drain to Source V	oltage			30	V
$V_{GS}$	Gate to Source Vo	Gate to Source Voltage			±20	V
	Drain Current	-Continuous	T <sub>A</sub> = 25°C	(Note 1a)	4.8	^
ID	-Pulsed			9	A	
Б	Power Dissipation		T <sub>A</sub> = 25°C	Note 1a)	1.6	W
$P_{D}$	Power Dissipation		T <sub>A</sub> = 25°C	(Note 1b)	0.75	VV
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range			-55 to +150	°C	

### **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	80	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	165	C/VV

### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
3800	FDMB3800N	MicroFET3X1.9	7"	8mm	3000 units

# **Electrical Characteristics** T<sub>J</sub> = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	acteristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, referenced to 25°C		24		mV/°C
	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 24V,			1	^
DSS	Zero Gate Voltage Drain Current	$V_{GS} = 0V$ $T_J = 55^{\circ}C$			10	μΑ
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V			±100	nA

### **On Characteristics**

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, referenced to 25°C		-4		mV/°C
		$V_{GS} = 10V, I_D = 4.8A$		32	40	
r <sub>DS(on)</sub>	r <sub>DS(on)</sub> Drain to Source On Resistance	$V_{GS} = 4.5V, I_D = 4.3A$		41	51	mΩ
, ,		$V_{GS} = 10V$ , $I_D = 4.8A$ , $T_J = 125$ °C		43	61	
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = 5V, I_{D} = 4.8A$		14		S

### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	\\ -45\\ \\ -0\\	350	465	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> =15V, V <sub>GS</sub> = 0V, f = 1MHz	90	120	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 111112	40	60	pF
$R_g$	Gate Resistance	f = 1MHz	3		Ω

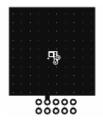
### **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time		8	16	ns
t <sub>r</sub>	Rise Time	$V_{DD}$ = 15V, $I_{D}$ = 1A $V_{GS}$ = 10V, $R_{GEN}$ = 6 $\Omega$	5	10	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	V <sub>GS</sub> = 10V, K <sub>GEN</sub> = 602	21	34	ns
t <sub>f</sub>	Fall Time		2	10	ns
$Q_{g(TOT)}$	Total Gate Charge at 5V	$V_{GS} = 0V \text{ to } 5V$ $V_{DD} = 15V$	4	5.6	nC
$Q_{gs}$	Gate to Source Gate Charge	I <sub>D</sub> = 7.5A	1.0		nC
$Q_{gd}$	Gate to Drain "Miller" Charge		1.5		nC

### **Drain-Source Diode Characteristics**

I <sub>S</sub>	Maximum Continuous Drain - Source Diode Forward Current				1.25	Α
$V_{SD}$	Source to Drain Diode Forward Voltage $V_{GS} = 0V$ , $I_S = 1.25A$ (Note 2)			0.8	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	- I <sub>E</sub> = 4.8A, di/dt = 100A/μs		17		ns
Q <sub>rr</sub>	Reverse Recovery Charge	- I <sub>F</sub> = 4.8A, αι/αι = 100A/μS		7		nC

<sup>1:</sup> R<sub>0JA</sub> is determined with the device mounted on a 1in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R<sub>0JC</sub> is guaranteed by design while R<sub>0CA</sub> is determined by the user's board design.



a. 80°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 165°C/W when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width <  $300\mu$ s, Duty cycle < 2.0%.

### Typical Characteristics T<sub>J</sub> = 25°C unless otherwise noted

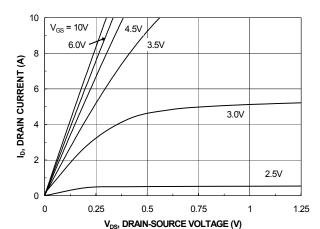


Figure 1. On Region Characteristics

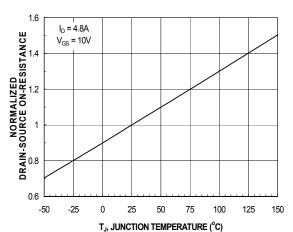


Figure 3. Normalized On - Resistance vs Junction Temperature

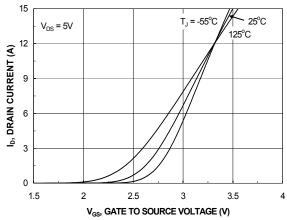
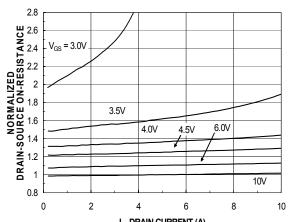


Figure 5. Transfer Characteristics



I<sub>D</sub>, DRAIN CURRENT (A)
Figure 2. Normalized On - Resistance
vs Drain Current and Gate Voltage

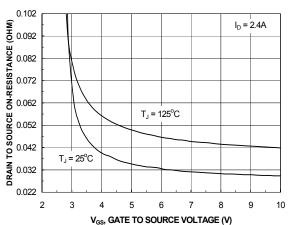


Figure 4. On-Resistance vs Gate to Source Voltage

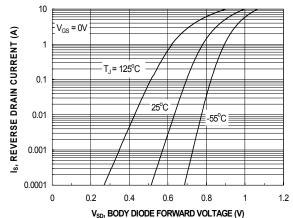


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

## Typical Characteristics T<sub>J</sub> = 25°C unless otherwise noted

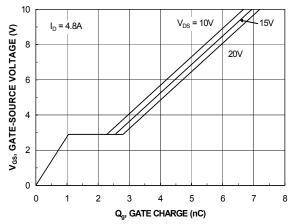


Figure 7. Gate Charge Characteristics

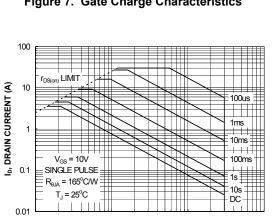
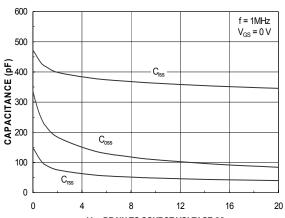


Figure 9. Forward Bias Safe **Operating Area** 

V<sub>DS</sub>, DRAIN-SOURCE VOLTAGE (V)

10

0.1



 $V_{\rm DS}$ , DRAIN TO SOURCE VOLTAGE (V) Figure 8. Capacitance vs Drain to Source Voltage

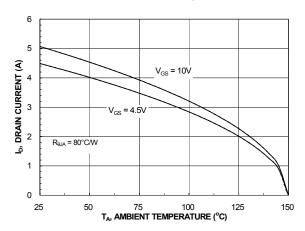
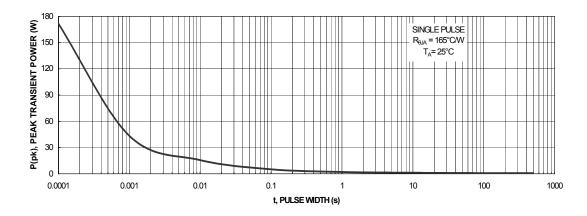


Figure 10. Maximum Continuous Drain **Current vs Ambient Temperature** 



100

Figure 11. Single Pulse Maximum Power Dissipation

# Typical Characteristics T<sub>J</sub> = 25°C unless otherwise noted

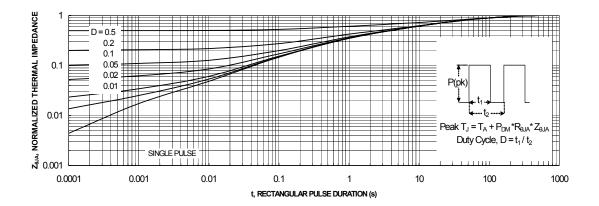
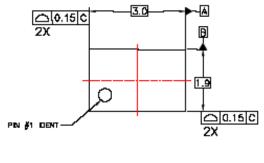
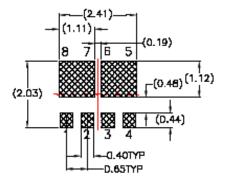


Figure 12. Transient Thermal Response Curve

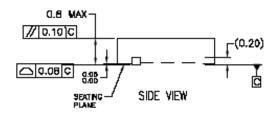
# **Dimensional Outline and Pad Layout**

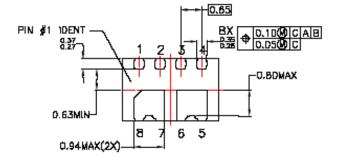


TOP VIEW



RECOMMENDED LAND PATTERN





BOTTOM VIEW

### **TRADEMARKS**

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

FACT Quiet Series™	OCX™	SILENT SWITCHER
GlobalOptoisolator™	OCXPro™	SMART START™
GTO™	OPTOLOGIC <sup>®</sup>	SPM™
HiSeC™	OPTOPLANAR™	Stealth™
I <sup>2</sup> C™	PACMAN™	SuperFET™
i-Lo™	POP™	SuperSOT™-3
ImpliedDisconnect™	Power247™	SuperSOT™-6
IntelliMAX™	PowerEdge™	SuperSOT™-8
ISOPLANAR™	PowerSaver™	SyncFET™
LittleFET™	PowerTrench <sup>®</sup>	TCM™
MICROCOUPLER™	QFET <sup>®</sup>	TinyBoost™
MicroFET™	QS™	TinyBuck™
MicroPak™	QT Optoelectronics™	TinyPWM™
MICROWIRE™	Quiet Series™	TinyPower™
MSX™	RapidConfigure™	TinyLogic <sup>®</sup>
MSXPro™	RapidConnect™	TINYOPTO™
d the world.™	μSerDes™	TruTranslation™
	ScalarPump™	UHC™
	GlobalOptoisolator <sup>TM</sup> GTO <sup>TM</sup> HiSeC <sup>TM</sup> I <sup>2</sup> C <sup>TM</sup> IrLo <sup>TM</sup> ImpliedDisconnect <sup>TM</sup> IntelliMAX <sup>TM</sup> ISOPLANAR <sup>TM</sup> LittleFET <sup>TM</sup> MICROCOUPLER <sup>TM</sup> MicroFET <sup>TM</sup> MICROWIRE <sup>TM</sup> MSX <sup>TM</sup> MSXPro <sup>TM</sup>	GlobalOptoisolator™ OCXPro™ GTO™ OPTOLOGIC® HiSeC™ OPTOPLANAR™ I²C™ PACMAN™ I·Lo™ POP™ ImpliedDisconnect™ Power247™ IntelliMAX™ PowerEdge™ ISOPLANAR™ PowerSaver™ LittleFET™ PowerTrench® MICROCOUPLER™ QFET® MicroFET™ QS™ MicroPak™ QT Optoelectronics™ MICROWIRE™ Quiet Series™ MSX™ RapidConnect™ MSXPro™ RapidConnect™ d the world.™

### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

Programmable Active Droop™

LIFE SUPPORT POLICY
FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

### As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

UniFET™ UltraFET® VCX™ Wire™

### PRODUCT STATUS DEFINITIONS **Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. 120