

FDP7045L/FDB7045L

N-Channel Logic Level PowerTrench[®] MOSFET

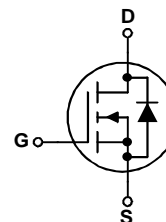
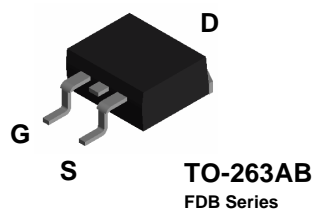
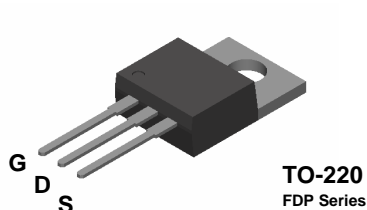
General Description

This N-Channel Logic Level MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable $R_{DS(ON)}$ specifications resulting in DC/DC power supply designs with higher overall efficiency.

Features

- 100 A, 30 V $R_{DS(ON)} = 4.5 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$
 $R_{DS(ON)} = 6.0 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$
- Critical DC electrical parameters specified at elevated temperature
- High performance trench technology for extremely low $R_{DS(ON)}$
- 175°C maximum junction temperature rating



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current – Continuous (Note 1)	100	A
	– Pulsed (Note 1)	300	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	107	W
		0.7	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +175	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.4	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDB7045L	FDB7045L	13"	24mm	800 units
FDP7045L	FDP7045L	Tube	n/a	45

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain-Source Avalanche Ratings (Note 1)						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 15\text{ V}, I_D = 75\text{ A}$			330	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				75	A
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C		25		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate-Body Leakage	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1	1.8	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C		-6		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 50\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 40\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 50\text{ A}, T_J = 125^\circ\text{C}$		3.5 4.0 5.5	4.5 6.0 7.0	m Ω
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 10\text{ V}$	50			A
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 50\text{ A}$		165		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		4357		pF
C_{oss}	Output Capacitance			1092		pF
C_{riss}	Reverse Transfer Capacitance			399		pF
R_G	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$		1.4		Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		16	29	ns
t_r	Turn-On Rise Time			13	24	ns
$t_{d(off)}$	Turn-Off Delay Time			74	119	ns
t_f	Turn-Off Fall Time			41	66	ns
Q_g	Total Gate Charge	$V_{DS} = 15\text{ V}, I_D = 50\text{ A},$ $V_{GS} = 5\text{ V}$		41	58	nC
Q_{gs}	Gate-Source Charge			12		nC
Q_{gd}	Gate-Drain Charge			14		nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current				75	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 50\text{ A}$ (Note 1)		0.91	1.2	V
t_{rr}	Diode Reverse Recovery Time	$I_F = 50\text{ A},$ $dI_F/dt = 100\text{ A}/\mu\text{s}$		48		nS
Q_{rr}	Diode Reverse Recovery Charge			42		nC

Notes:

1. Calculated continuous current based on maximum allowable junction temperature. Actual maximum continuous current limited by package constraints to 75A.
2. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

Typical Characteristics

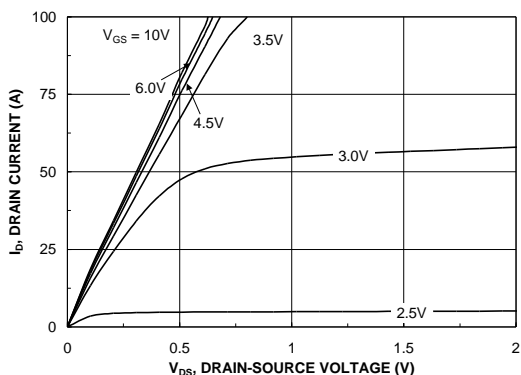


Figure 1. On-Region Characteristics.

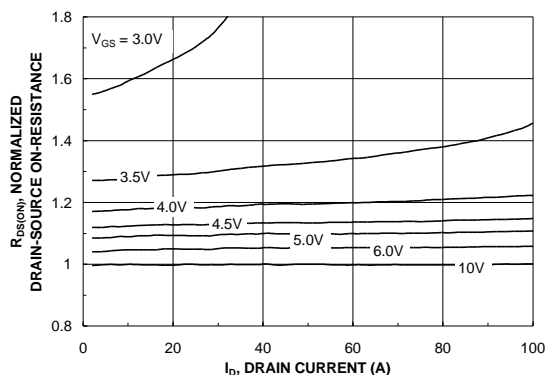


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

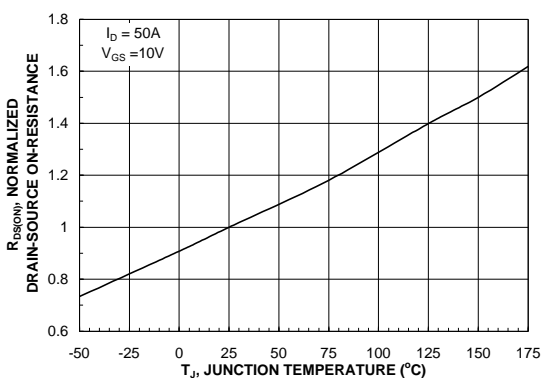


Figure 3. On-Resistance Variation with Temperature.

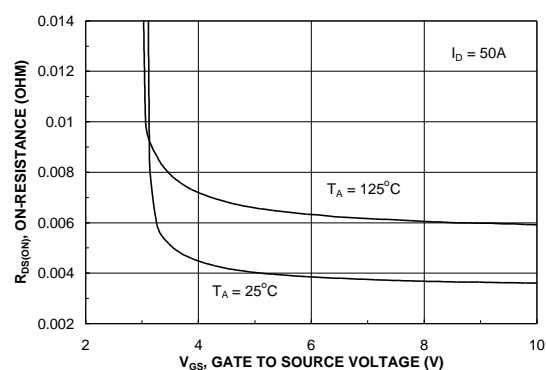


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

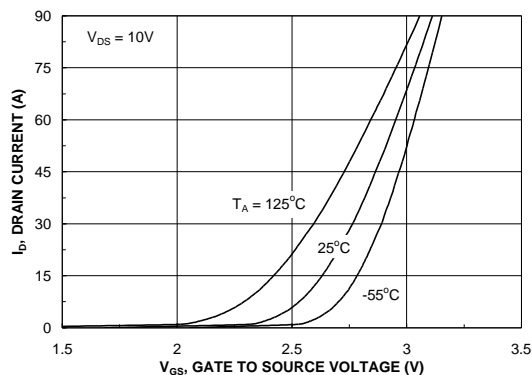


Figure 5. Transfer Characteristics.

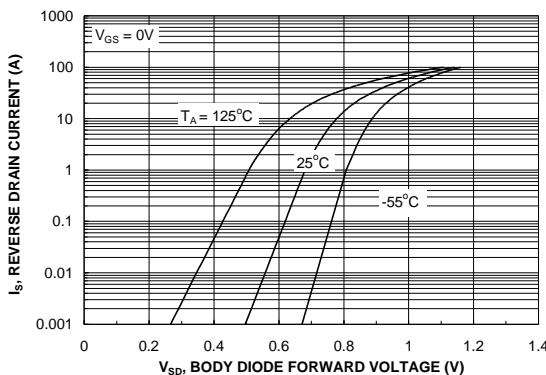


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

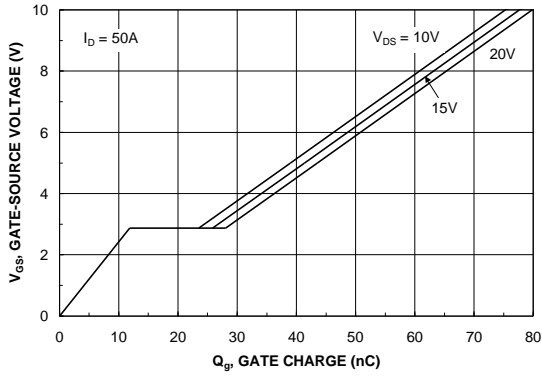


Figure 7. Gate Charge Characteristics.

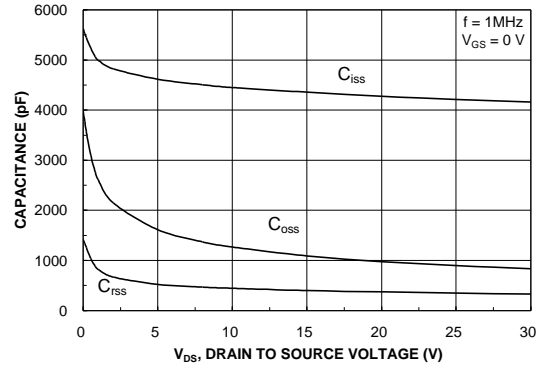


Figure 8. Capacitance Characteristics.

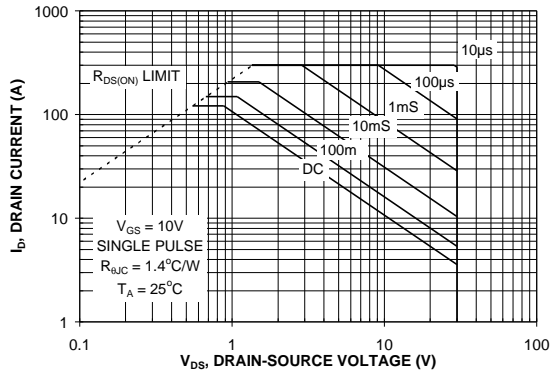


Figure 9. Maximum Safe Operating Area.

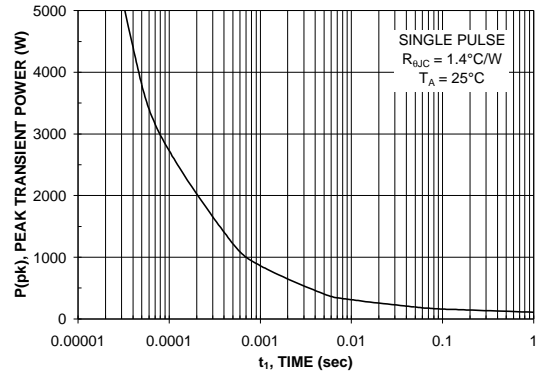


Figure 10. Single Pulse Maximum Power Dissipation.

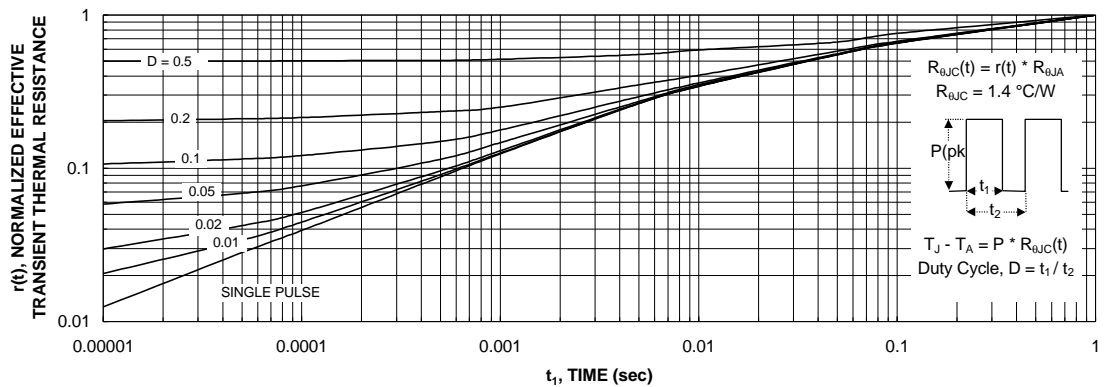


Figure 11. Transient Thermal Response Curve.

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FACT Quiet Series™	ImpliedDisconnect™	PACMAN™	SPM™
ActiveArray™	FAST®	ISOPLANAR™	POP™	Stealth™
Bottomless™	FASTr™	LittleFET™	Power247™	SuperFET™
CoolFET™	FPST™	MICROCOUPLER™	PowerSaver™	SuperSOT™-3
CROSSVOLT™	FRFET™	MicroFET™	PowerTrench®	SuperSOT™-6
DOMET™	GlobalOptoisolator™	MicroPak™	QFET®	SuperSOT™-8
EcoSPARK™	GTO™	MICROWIRE™	QS™	SyncFET™
E ² C MOS™	HiSeC™	MSX™	QT Optoelectronics™	TinyLogic®
EnSigna™	µC™	MSXPro™	Quiet Series™	TINYOPTO™
FACT™	i-Lo™	OCX™	RapidConfigure™	TruTranslation™
Across the board. Around the world.™	OCXPro™	OCXPro™	RapidConnect™	UHC™
The Power Franchise®	OPTOLOGIC®	OPTOLOGIC®	SILENT SWITCHER®	UltraFET®
Programmable Active Droop™	OPTOPLANAR™	OPTOPLANAR™	SMART START™	VCX™

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.