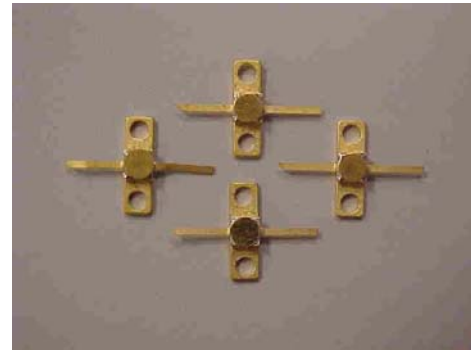


FEATURES

- ◆ 32.5 dBm Linear Output Power
- ◆ 17 dB Power Gain at 2 GHz
- ◆ 9.5 dB Maximum Stable Gain at 10 GHz
- ◆ 42 dBm Output IP3
- ◆ 45% Power-Added Efficiency at 2 GHz


DESCRIPTION AND APPLICATIONS

The FPD3000P100 is a packaged AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (PHEMT), featuring a 0.25 μm by 3000 μm Schottky barrier gate, defined by high-resolution stepper-based photolithography. The recessed and offset Gate structure minimizes parasitics to optimize performance. The epitaxial structure and processing have been optimized for reliable high-power applications. The FPD3000P100 also features Si_3N_4 passivation and is also available in die form and in the low cost plastic SOT89 plastic package.

Typical applications include commercial and other narrowband and broadband high-performance amplifiers, including SATCOM uplink transmitters, PCS/Cellular low-voltage high-efficiency output amplifiers, and medium-haul digital radio transmitters.

ELECTRICAL SPECIFICATIONS AT 22°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
UNLESS OTHERWISE NOTED, RF SPECIFICATIONS MEASURED AT $f = 2$ GHz USING CW SIGNAL						
Power at 1dB Gain Compression	$P_{1\text{dB}}$	$V_{\text{DS}} = 8 \text{ V}; I_{\text{DS}} = 50\% I_{\text{DSS}}$	31.0	32.5		dBm
Power Gain at $P_{1\text{dB}}$	$G_{1\text{dB}}$	$V_{\text{DS}} = 8 \text{ V}; I_{\text{DS}} = 50\% I_{\text{DSS}}$	16.5	17.0		dB
Maximum Stable Gain (S_{21}/S_{12})	SSG	$V_{\text{DS}} = 8 \text{ V}; I_{\text{DS}} = 50\% I_{\text{DSS}}$ $f = 2 \text{ GHz}$	20.5	21.5		dB
			$f = 10 \text{ GHz}$	8.5	9.5	
Power-Added Efficiency	PAE	$V_{\text{DS}} = 8 \text{ V}; I_{\text{DS}} = 50\% I_{\text{DSS}};$ $P_{\text{OUT}} = P_{1\text{dB}}$		45		%
Output Third-Order Intercept Point (from 15 to 5 dB below $P_{1\text{dB}}$)	IP3	$V_{\text{DS}} = 8 \text{ V}; I_{\text{DS}} = 50\% I_{\text{DSS}}$ Matched for optimal power		42		dBm
Saturated Drain-Source Current	I_{DSS}	$V_{\text{DS}} = 1.3 \text{ V}; V_{\text{GS}} = 0 \text{ V}$	750	930	1110	mA
Maximum Drain-Source Current	I_{MAX}	$V_{\text{DS}} = 1.3 \text{ V}; V_{\text{GS}} \cong +1 \text{ V}$		1.5		A
Transconductance	G_{M}	$V_{\text{DS}} = 1.3 \text{ V}; V_{\text{GS}} = 0 \text{ V}$		800		mS
Gate-Source Leakage Current	I_{GSO}	$V_{\text{GS}} = -5 \text{ V}$		2	20	μA
Pinch-Off Voltage	$ V_{\text{P}} $	$V_{\text{DS}} = 1.3 \text{ V}; I_{\text{DS}} = 3 \text{ mA}$	0.7	1.0	1.3	V
Gate-Drain Breakdown Voltage	$ V_{\text{BDGD}} $	$I_{\text{GD}} = 3 \text{ mA}$	14.5	16.0		V
Thermal Resistivity (see Notes)	θ_{JC}	$V_{\text{DS}} > 6 \text{ V}$		24		$^{\circ}\text{C/W}$

• **RECOMMENDED BIAS CONDITIONS:**

Drain-Source Voltage: 5V to 8V Drain-Source Current: 33% to 50% I_{DSS}

• **ABSOLUTE MAXIMUM RATINGS¹**

Parameter	Symbol	Test Conditions	Min	Max	Units
Drain-Source Voltage	V _{DS}	-3V < V _{GS} < +0V		9	V
Gate-Source Voltage	V _{GS}	0V < V _{DS} < +8V		-3	V
Drain-Source Current	I _{DS}	For V _{DS} > 2V		I _{DSS}	mA
Gate Current	I _G	Forward or reverse current		25	mA
RF Input Power ²	P _{IN}	Under any acceptable bias state		600	mW
Channel Operating Temperature	T _{CH}	Under any acceptable bias state		175	°C
Storage Temperature	T _{STG}	Non-Operating Storage	-40	150	°C
Total Power Dissipation	P _{TOT}	See De-Rating Note below		5.3	W
Gain Compression	Comp.	Under any bias conditions		5	dB
Simultaneous Combination of Limits ³		2 or more Max. Limits		80	%

¹T_{Ambient} = 22°C unless otherwise noted ²Max. RF Input Limit must be further limited if input VSWR > 2.5:1

³Users should avoid exceeding 80% of 2 or more Limits simultaneously

Notes:

- Operating conditions that exceed the Absolute Maximum Ratings could result in permanent damage to the device.
- Thermal Resistivity specification assumes a Au/Sn eutectic die attach onto a Au-plated copper heatsink or rib.
- Power Dissipation defined as: P_{TOT} ≡ (P_{DC} + P_{IN}) – P_{OUT}, where
 P_{DC}: DC Bias Power
 P_{IN}: RF Input Power
 P_{OUT}: RF Output Power
- Absolute Maximum Power Dissipation to be de-rated as follows above 22°C:
 P_{TOT} = 5.3W – (0.042W/°C) x T_{HS}
 where T_{HS} = heatsink or ambient temperature above 22°C
 Example: For a 85°C heatsink temperature: P_{TOT} = 5.3W – (0.042 x (85 – 22)) = 2.65

• **HANDLING PRECAUTIONS**

To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 0 (< 250V) per JESD22-A114-B, Human Body Model, and Class A (< 200V) per JESD22-A115-A, Machine Model.

- **APPLICATIONS NOTES & DESIGN DATA**

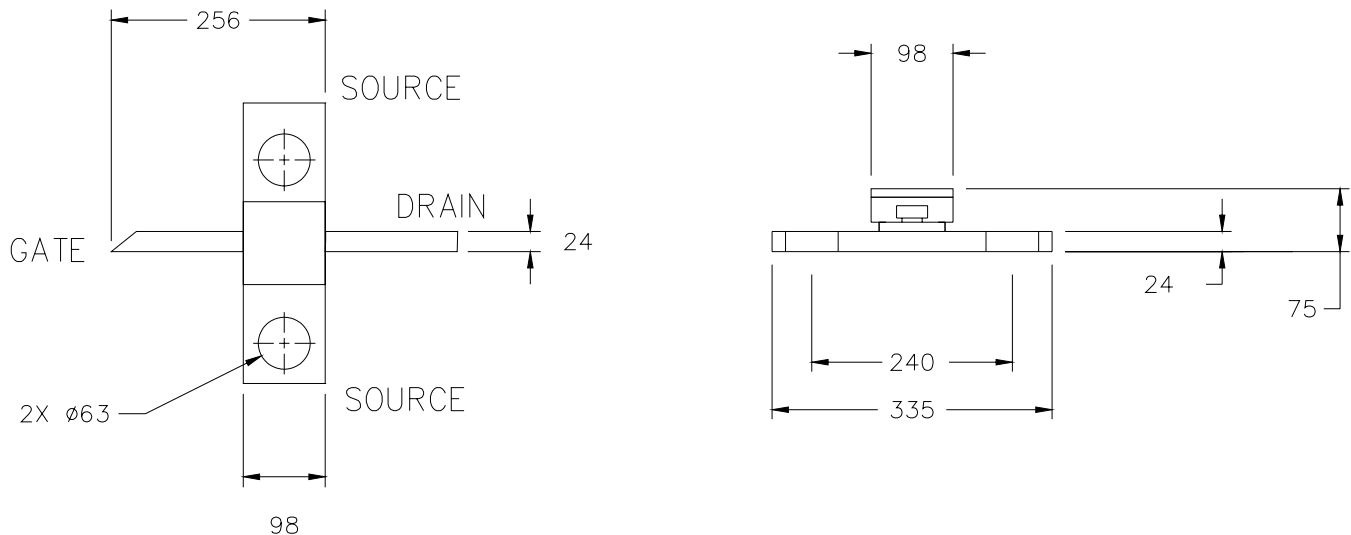
Applications Notes are available from your local Filtronic Sales Representative or directly from the factory. Complete design data, including S-parameters, noise data, and large-signal models are available on the Filtronic web site.

- **RECOMMENDED BIASING GUIDELINES:**

For most applications, a dual-bias circuit is required due to the amount of quiescent current drawn by the FPD3000P100. The Source of the discrete pHEMT device is wire-bonded to the package flange, and therefore self-biasing (using a bypassed Source resistor to set the Gate-Source voltage) is not practical. A dual-bias circuit will require a regulated and filtered negative Gate supply as well as a positive Drain supply. Typical Gate bias voltages will be about -0.4V. Active bias circuits can be employed if the dissipation by a Drain current sense resistor is acceptable, and in these cases the bias voltages must be sequenced so that the negative Gate voltage is established at its final value before the Drain voltage is reached, to prevent device self-oscillation.

PACKAGE OUTLINE

dimensions in mils, tolerance = ± 3 mils



All information and specifications are subject to change without notice.