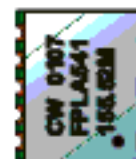


CRYSTAL CONTROLLED OSCILLATORS



SURFACE MOUNT 3.3V LVPECL CLOCK



FPLA541

ABSOLUTE MAXIMUM RATINGS

TABLE 1.0

PARAMETER	UNITS	MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
Storage Temperature		-40	-	85	°C	
Supply Voltage	(V _{cc})	-0.5	-	7.0	V _{dc}	

OPERATING SPECIFICATIONS

TABLE 2.0

PARAMETER		MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
Center Frequency	(F _o)	44.736	-	162	MHz	
Total Frequency Tolerance		-20		20	ppm	1
Operating Temperature Range		0	-	70	°C	
Supply Voltage	(V _{cc})	3.135	3.3	3.465	V _{dc}	
Supply Current	(I _{cc})	-	-	60	mA	
Jitter (BW=10kHz to 20MHz)		-	-	5	pSRMS	
Jitter (BW=12kHz to 20MHz)		-	-	1	pSRMS	

LVPECL OUTPUT CHARACTERISTICS

TABLE 3.0

PARAMETER		MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
LOAD		-	-	50	Ohms	2
Voltage (High)	(V _{oh})	2.275	-	-	V _{dc}	
Voltage (Low)	(V _{ol})	-	-	1.68	V _{dc}	
Duty Cycle		45	50	55	%	3
Rise / Fall Time 20% to 80%		-	-	1	nS	

PACKAGE CHARACTERISTICS

TABLE 4.0

Package	Non-hermetic package consisting of an FR4 substrate with grounded metal cover.
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PROCESS RECOMMENDATIONS

TABLE 5.0

Solder Reflow	The component solder used internal to this device has a melting point of 221°C. The peak temperature inside the device should be less than or equal to 220°C for a maximum of 10 seconds.
Wash	Ultrasonic cleaning is not recommended.

Notes

- Includes initial tolerance, deviation over temperature, supply and load variations, shock, vibration and 10 years aging.
- Output must be terminated into 50 ohms to V_{cc} - 2V or Thevenin equivalent.
- Duty Cycle measured at 1.977V

DESCRIPTION

The Connor-Winfield FPLA541 is a fixed frequency, surface mount Crystal Controlled Oscillator (XO) designed for applications requiring low jitter and a ±20ppm overall stability. Operating at 3.3V supply voltage, the FPLA541 provides LVPECL

FEATURES

- 3.3V OPERATION
- LOW JITTER <1pS RMS
- OVERALL FREQUENCY TOLERANCE ±20PPM
- SURFACE MOUNT PACKAGE
- TAPE AND REEL PACKAGING

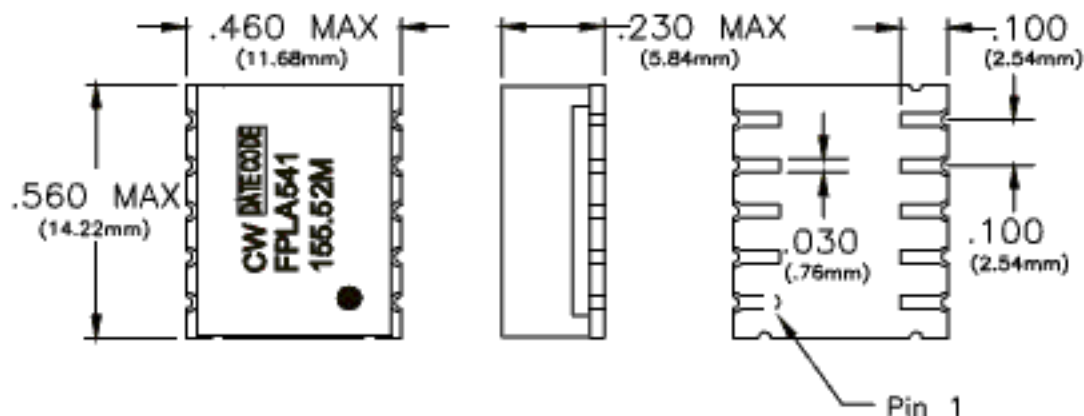
ORDERING INFORMATION

FPLA541 - 155.52MHz

CLOCK SERIES

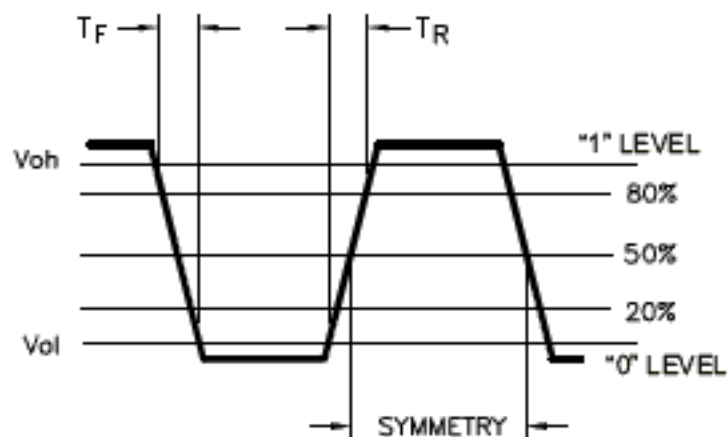
CENTER FREQUENCY

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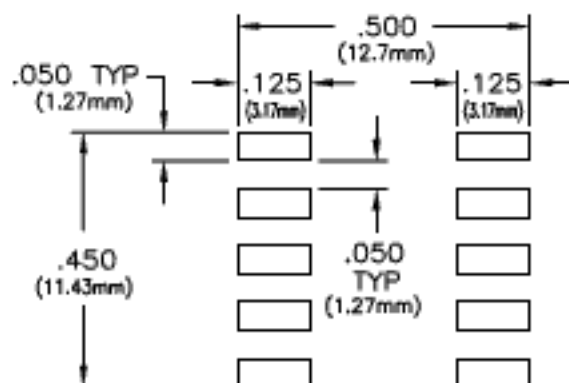


PIN	CONNECTION
1	NC
2	NC
3	NC
4	GROUND
5	NC
6	Q OUTPUT
7	Q OUTPUT
8	NC
9	Vcc
10	NC

OUTPUT WAVEFORM



SUGGESTED PAD LAYOUT



TEST CIRCUIT

