

# FQD3N60C

## 600V N-Channel MOSFET

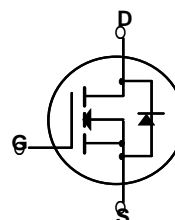
### Features

- 2.4A, 600V,  $R_{DS(on)} = 3.4\Omega @ V_{GS} = 10V$
- Low gate charge ( typical 10.5 nC)
- Low  $C_{rss}$  ( typical 5 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

### Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction, electronic lamp ballasts based on half bridge topology.



### Absolute Maximum Ratings

Symbol	Parameter	FQD3N60C	Unit
$V_{DSS}$	Drain-Source Voltage	600	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ C$ ) - Continuous ( $T_C = 100^\circ C$ )	2.4 1.5	A A
$I_{DM}$	Drain Current - Pulsed (Note 1)	9.6	A
$V_{GSS}$	Gate-Source voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	150	mJ
$I_{AR}$	Avalanche Current (Note 1)	2.4	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	5.0	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ C$ ) - Derate above $25^\circ C$	50 0.4	W W/ $^\circ C$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ C$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ C$

### Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	2.5	$^\circ C/W$
$R_{\theta JA}^*$	Thermal Resistance, Junction-to-Ambient*	--	50	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	110	$^\circ C/W$

\* When mounted on the minimum pad size recommended (PCB Mount)

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQD3N60C	FQD3N60CTM	D-PAK	380mm	16mm	2500
FQD3N60C	FQD3N60CTF	D-PAK	380mm	16mm	2000

## Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	600	--	--	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, Referenced to 25°C	--	0.6	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 600V, V <sub>GS</sub> = 0V V <sub>DS</sub> = 480V, T <sub>C</sub> = 125°C	--	--	1 10	μA μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30V, V <sub>DS</sub> = 0V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30V, V <sub>DS</sub> = 0V	--	--	-100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	2.0	--	4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 1.2A	--	2.8	3.4	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40V, I <sub>D</sub> = 1.2A (Note 4)	--	3.5	--	S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f = 1.0MHz	--	435	565	pF
C <sub>oss</sub>	Output Capacitance		--	45	60	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	5	8	pF
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 300V, I <sub>D</sub> = 3A R <sub>G</sub> = 25Ω  (Note 4, 5)	--	12	34	ns
t <sub>r</sub>	Turn-On Rise Time		--	30	70	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	35	80	ns
t <sub>f</sub>	Turn-Off Fall Time		--	35	80	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 480V, I <sub>D</sub> = 3A V <sub>GS</sub> = 10V  (Note 4, 5)	--	10.5	14	nC
Q <sub>gs</sub>	Gate-Source Charge		--	2.1	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	4.5	--	nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	3	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	12	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> = 2.4A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>S</sub> = 3A di <sub>F</sub> /dt = 100A/μs  (Note 4)	--	260	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	1.6	--	μC

### NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. I<sub>AS</sub> = 2.4A, V<sub>DD</sub> = 50V, L = 47mH, R<sub>G</sub> = 25Ω, Starting T<sub>J</sub> = 25°C
3. I<sub>SD</sub> ≤ 3A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, Starting T<sub>J</sub> = 25°C
4. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

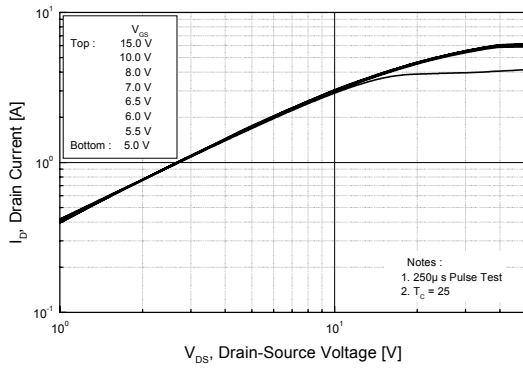


Figure 2. Transfer Characteristics

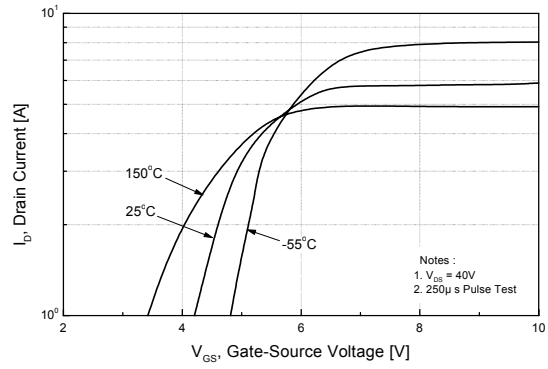


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

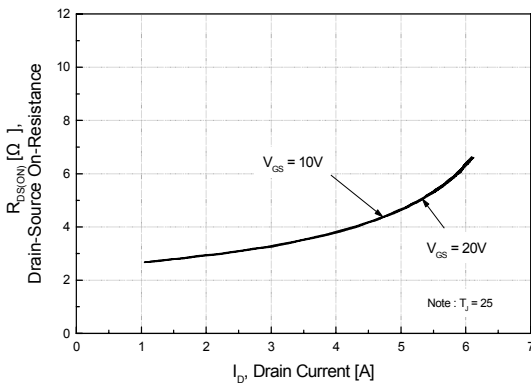


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

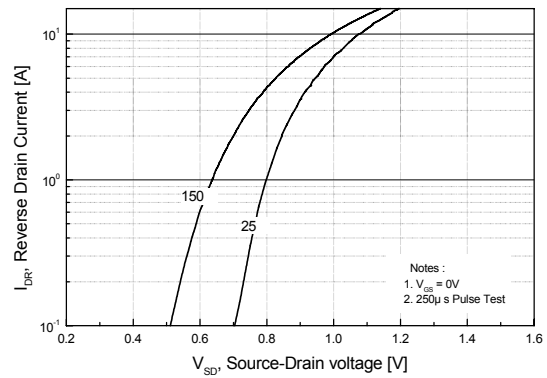


Figure 5. Capacitance Characteristics

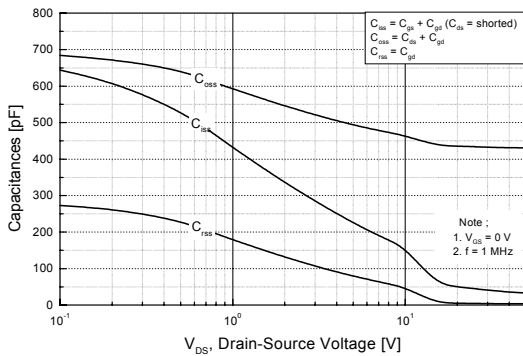
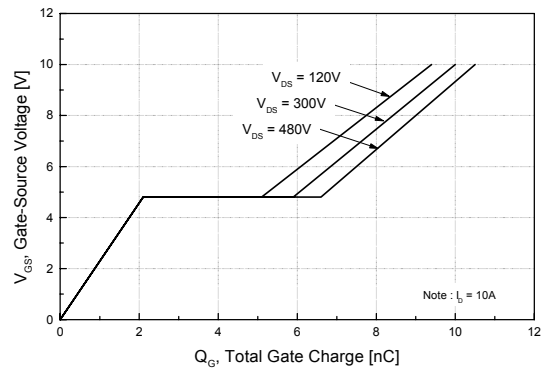


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

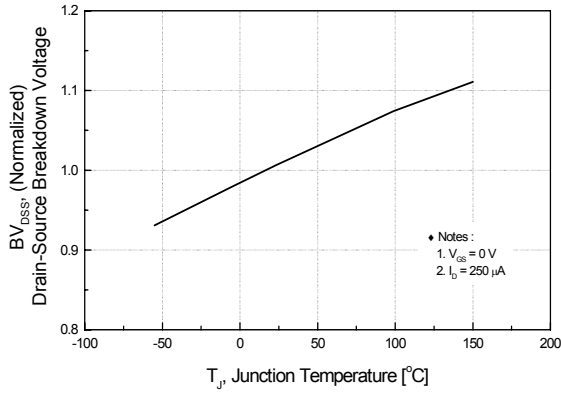


Figure 8. On-Resistance Variation vs. Temperature

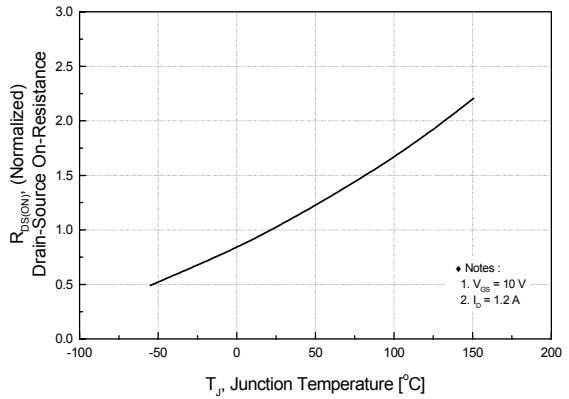


Figure 9. Maximum Safe Operating Area

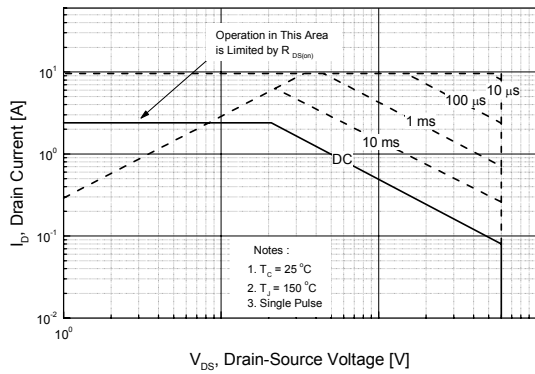


Figure 10. Maximum Drain Current vs. Case Temperature

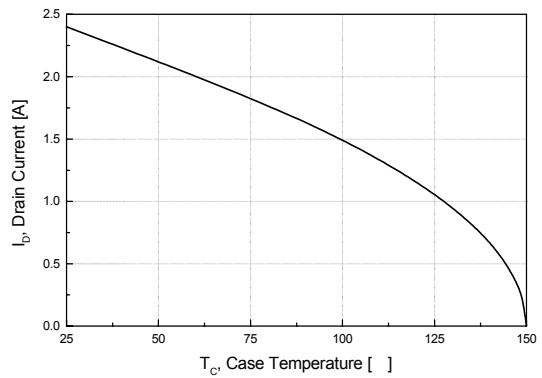
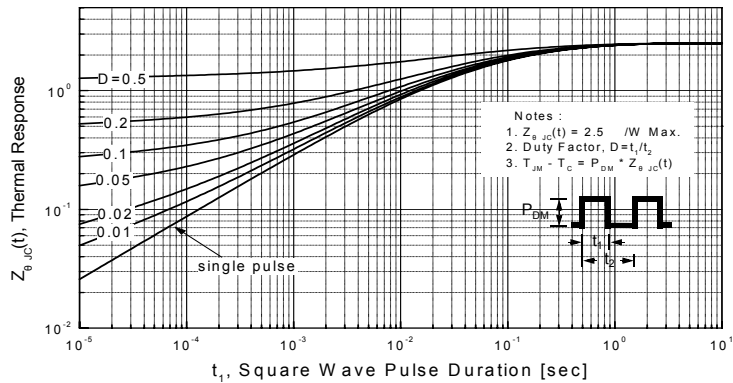
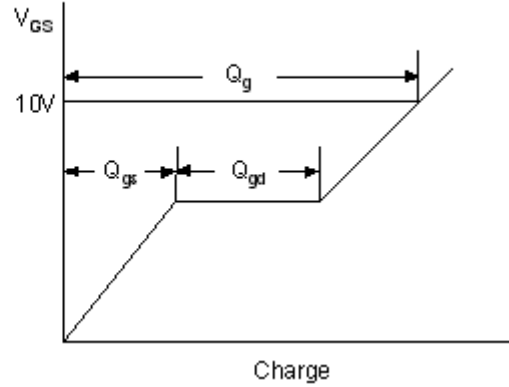
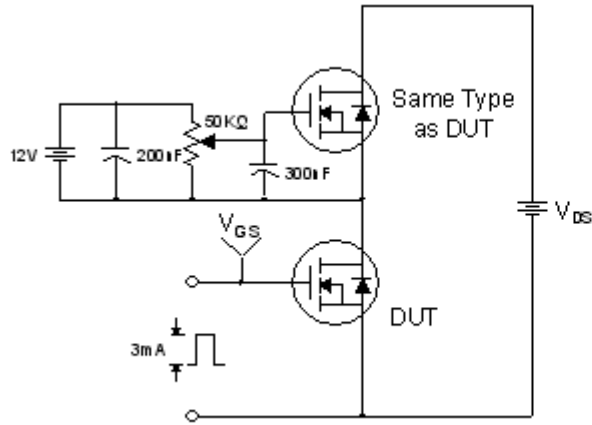


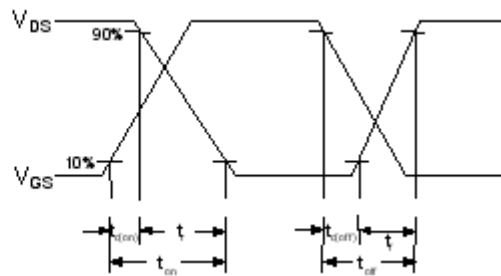
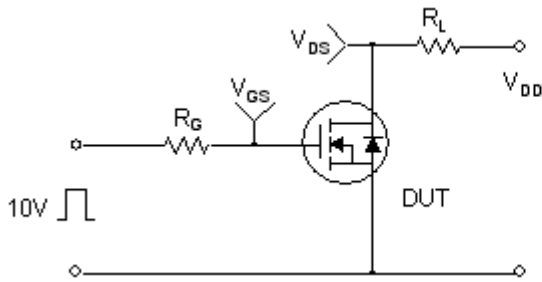
Figure 11. Transient Thermal Response Curve



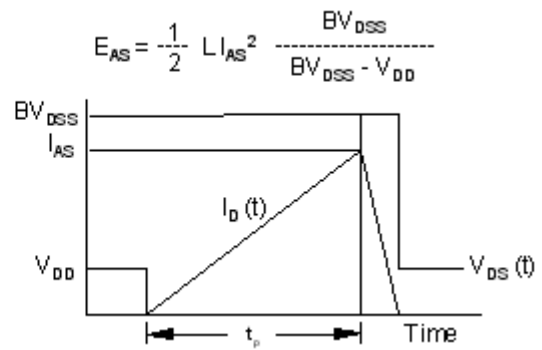
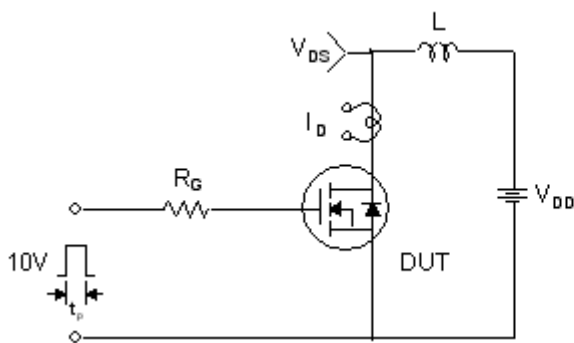
**Gate Charge Test Circuit & Waveform**



**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**

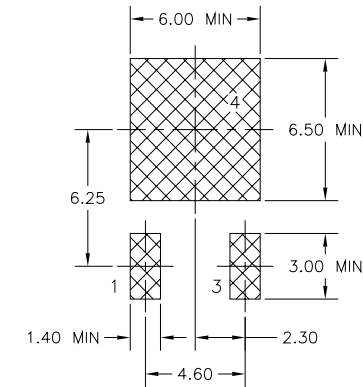
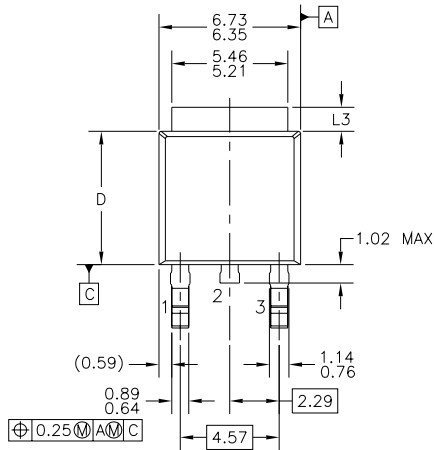


Peak Diode Recovery dv/dt Test Circuit & Waveforms

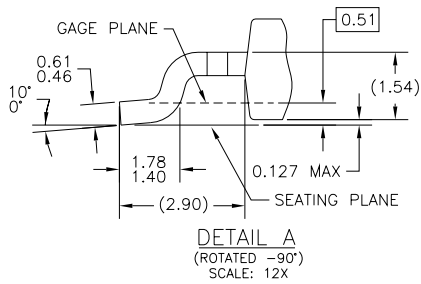
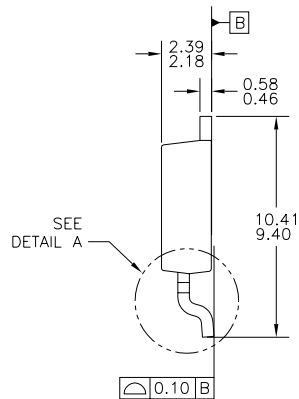
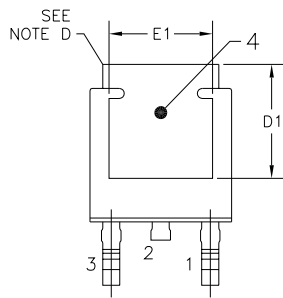


Mechanical Dimensions

D-PAK



LAND PATTERN RECOMMENDATION



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
  - B) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.
  - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
  - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
  - E) DIMENSIONS L3,D,E1&D1 TABLE:
- |    | OPTION AA | OPTION AB |
|----|-----------|-----------|
| L3 | 0.89-1.27 | 1.52-2.03 |
| D  | 5.97-6.22 | 5.33-5.59 |
| E1 | 4.32 MIN  | 3.81 MIN  |
| D1 | 5.21 MIN  | 4.57 MIN  |
- F) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

Dimensions in Millimeters

## TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FAST®	ISOPLANAR™	PowerSaver™	SuperSOT™-6
ActiveArray™	FASTr™	LittleFET™	PowerTrench®	SuperSOT™-8
Bottomless™	FPST™	MICROCOUPLER™	QFET®	SyncFET™
Build it Now™	FRFET™	MicroFET™	QS™	TCM™
CoolFET™	GlobalOptoisolator™	MicroPak™	QT Optoelectronics™	TinyLogic®
CROSSVOLT™	GTO™	MICROWIRE™	Quiet Series™	TINYOPTO™
DOME™	HiSeC™	MSX™	RapidConfigure™	TruTranslation™
EcoSPARK™	I <sup>2</sup> C™	MSXPro™	RapidConnect™	UHC™
E <sup>2</sup> C MOS™	i-Lo™	OCX™	μSerDes™	UltraFET®
EnSigna™	ImpliedDisconnect™	OCXPro™	ScalarPump™	UniFET™
FACT™	IntelliMAX™	OPTOLOGIC®	SILENT SWITCHER®	VCX™
FACT Quiet Series™		OPTOPLANAR™	SMART START™	Wire™
Across the board. Around the world.™		PACMAN™	SPM™	
The Power Franchise®		POP™	Stealth™	
Programmable Active Droop™		Power247™	SuperFET™	
		PowerEdge™	SuperSOT™-3	

## DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.