CML Semiconductor Products

PRODUCT INFORMATION

FX489 GMSK Modem

Obsolete Product - For Information Only

Features

- Full-Duplex Gaussian Minimum Shift Keying
- Selectable BT (0.3 or 0.5)
- Meets RAM - MOBITEX Specification
- Data Rates From 4000bits/s to 19200bits/s
- Serial Rx and Tx Data Interfaces
- Rx and Tx Data Clock Generation
- Rx Signal Tracking Controls
- Rx S/N Indication
- Separate Rx and Tx Powersave Inputs
- Wireless Modem, Radio Telemetry and Data Terminal Applications

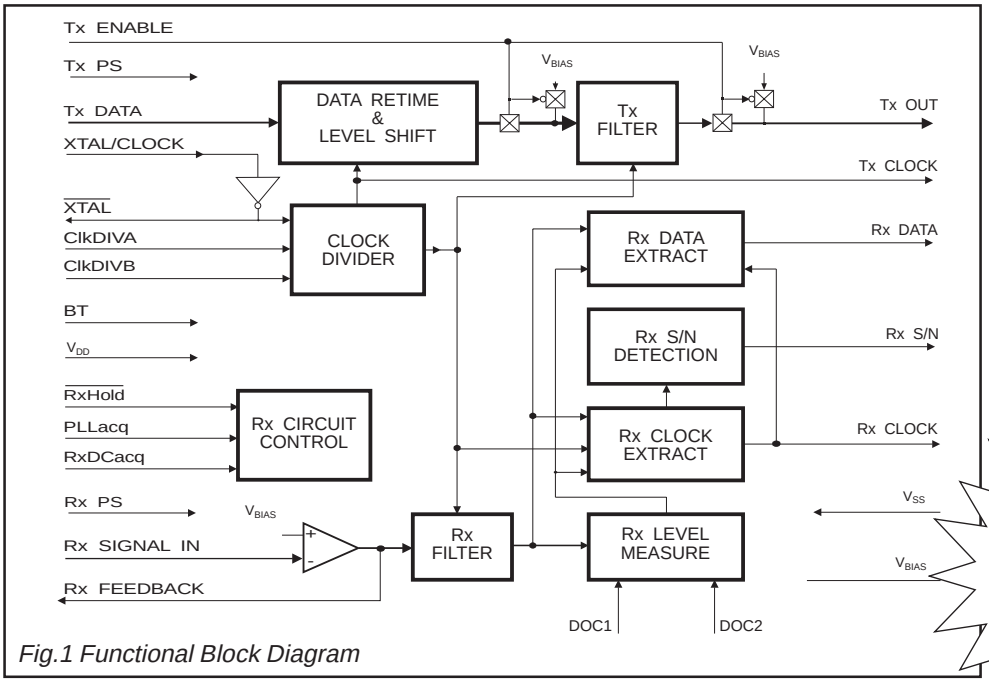


Fig.1 Functional Block Diagram

FX489

NEW 40kbps Modem **FX589** Pin/Function Compatible

Brief Description

The FX489 is a single-chip modem employing Gaussian Minimum Shift Keying (GMSK) modulation. Having a pin selectable BT of 0.3 or 0.5, the FX489 may be employed at data rates of between 4,000bits/s and 19,200bits/s; for use in FM radio-data links and data communication systems conforming to DOC and FCC spectrum limitations for 12.5kHz and 8,000 baud at a BT of 0.3, and 12.5, 25.0, and 50.kHz channel spacing and data rates of 4800, 9600 and 19,200 baud respectively at a BT of 0.5.

The Rx and Tx digital data interfaces are bit-serial and synchronised to Rx and Tx data clocks generated by the modem. Separate Rx and Tx Powersave/ Enable inputs allow for full- or half-duplex operation.

Rx input levels can be set by a suitable a.c. and d.c. level adjusting circuit built, with external components, around an on-chip Rx input amplifier.

Acquisition, lock and hold of Rx data signals is made easier and faster by the use of Rx Control Inputs to clamp, detect and/or hold input data levels and can be set by the µProcessor as required.

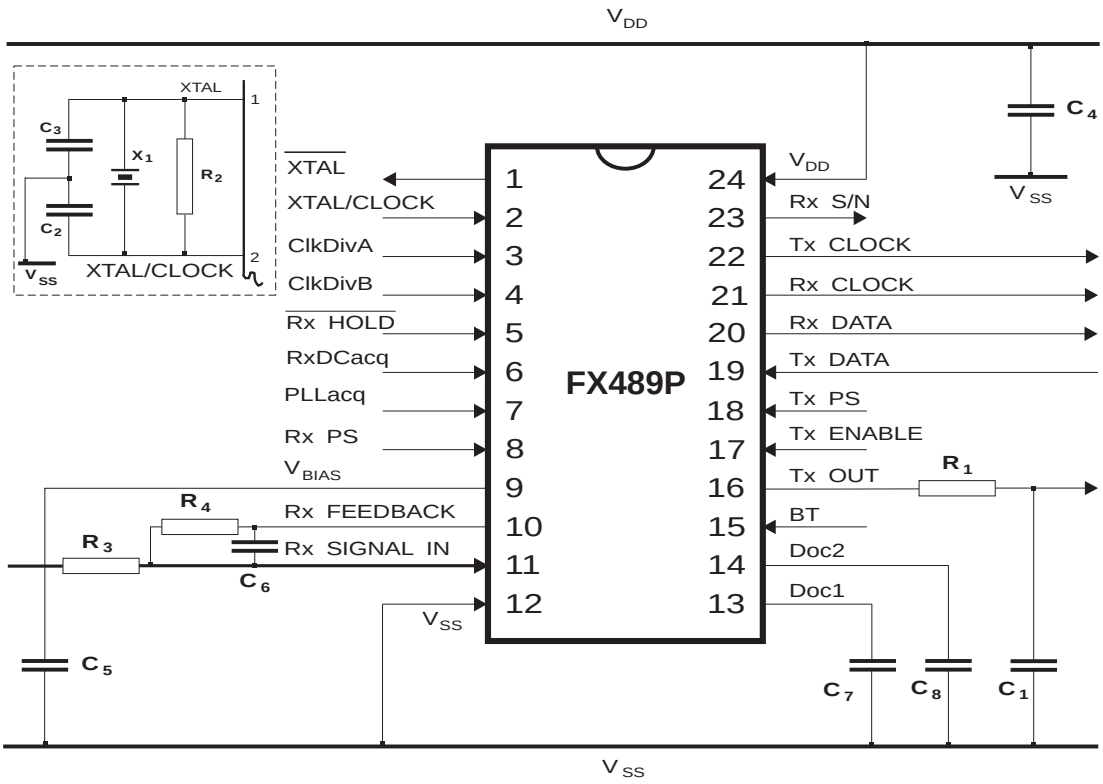
Indication is available, from the Rx S/N output, as to the quality of the received signal.

The FX489, a low-power CMOS microcircuit, is available in both 24-pin plastic Small Outline (S.O.I.C) and DIL packages.

Pin Number FX489DW FX489P	Function
1	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator.
2	**Xtal/Clock:** The input to the on-chip Xtal oscillator. A Xtal, or externally derived clock (f_{XTAL}) pulse input should be connected here. If an externally generated clock is to be used, it should be connected to this pin and the "$\overline{\text{Xtal}}$" pin left unconnected. Note that operation of the FX489 without a suitable Xtal or clock input may cause device damage.
3	**ClkDivA:** Two logic level inputs that control the internal clock divider and hence the transmit and receive data rate. See Table 1.
4	**ClkDivB:**
5	**$\overline{\text{Rx Hold}}$:** A logic "0" applied to this input will 'freeze' the Clock Extraction and Level Measurement circuits unless they are in 'acquire' mode.
6	**RXDCacq:** A logic "1" applied to this input will set the Rx Level Measurement circuitry to the 'acquire' mode.
7	**PLLacq:** A logic "1" applied to this input will set the Rx Clock Extraction circuitry to 'acquire' mode (see Table 2).
8	**Rx PS:** A logic "1" applied to this input will powersave all receive circuits except for "Rx Clock " output (which will continue at the set bit-rate) and cause the "Rx Data" and "Rx S/N" outputs to go to a logic "0".
9	**V_{BIAS}:** The internal circuitry bias line, held at $V_{DD}/2$, this pin must be decoupled to V_{SS} by a capacitor mounted close to the pin.
10	**Rx Feedback:** The output of the Rx Input Amplifier/The input to the Rx Filter.
11	**Rx Signal In:** The input to Rx input amplifier.
12	**V_{SS}:** Negative supply rail. Signal ground.

Pin Number FX489DW FX489P	Function
13	**Doc1:** Connections to the Rx Level Measurement Circuitry. A capacitor should be connected from each pin to V_{SS}.
14	**Doc2:**
15	**BT:** A logic level to select the modem 'BT' (the ratio of the Tx Filter's -3dB frequency to the Bit-Rate). A logic "1" sets the modem to a BT of 0.5, a logic "0" to a BT of 0.3.
16	**Tx Out:** The Tx signal output from the FX489 GMSK Modem.
17	**Tx Enable:** A logic "1" applied to this input enables the transmit data path through the Tx Filter to the "Tx Out pin". A logic "0" will put the "Tx Out" pin to V_{BIAS} via a high impedance.
18	**Tx PS:** A logic "1" applied to this input will powersave all transmit circuits except for the Tx Clock.
19	**Tx Data:** The logic level input for the data to be transmitted. This data should be synchronous with the "Tx Clock".
20	**Rx Data:** A logic level output carrying the received data, synchronous with the "Rx Clock".
21	**Rx Clock:** A logic level clock output at the received data bit-rate.
22	**Tx Clock:** A logic level clock output at the transmit-data rate.
23	**Rx S/N:** A logic level output which may be used as an indication of the quality of the received signal.
24	**V_{DD}:** Positive supply rail. A single +5 volt power supply is required. Levels and voltages within this modem are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor mounted close to the pin.

Application Information



External Components

Component	Value	Tolerance			
R_1	Note 1	±5%	C_4	100nF	±20%
R_2	1.0MΩ	±10%	C_5	1.0µF	±20%
R_3	Note 2	±10%	C_6	22.0pF	±20%
R_4	100kΩ	±10%	C_7	15.0nF	±20%
C_1	Note 1	±10%	C_8	15.0nF	±20%
C_2	33.0pF	±20%	X_1	Note 3	
C_3	33.0pF	±20%			

Fig.2 External Components

Notes

1. The RC network formed by R_1 and C_1 is required between the Tx Out pin and the input to the modulator. This network, which can form part of any d.c. level shifting and gain adjustment circuitry, forms an important part of the transmit signal filtering. The ground connection to the capacitor C_1 should be positioned to give maximum attenuation of high-frequency noise into the modulator.
   The component values should be chosen so that the product of the resistance (Ohms) and the capacitance (Farads) is:
   BT of 0.3 = 0.34/bit rate (bits/second)
   BT of 0.5 = 0.22/bit rate (bits/second)
   - with suitable values for common bit rates being:

		R_1	C_1
8000 bits/sec	BT = 0.3	91.0kΩ	470pF
4800 bits/sec	BT = 0.5	100kΩ	470pF
9600 bits/sec	BT = 0.5	47.0kΩ	470pF

   NOTE that in all cases, the value of R_1 should be not less than 47.0kΩ and the calculated value of C_1 includes calculated parasitic (circuit) capacitances.
2. R_3, R_4 and C_6 form the gain components for the Rx Input signal.
   R_3 should be chosen as required by the signal input level.
3. The FX489 can operate correctly with Xtal/Clock frequencies as detailed in Table 1.
   Operation of this device without a Xtal or Clock input may cause device damage.

Application Information .....

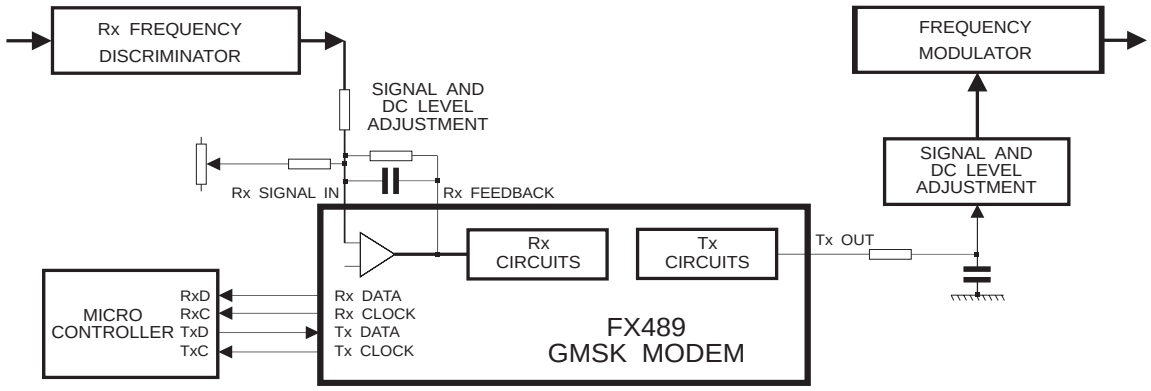


Fig.3 External Signal Paths

Clock Oscillator and Dividers

The Tx and (nominal) Rx data rates are determined by division of the frequency present at the Xtal pin, which may be generated by the on-chip Xtal oscillator or be derived from an external source.

The division ratio is controlled by the logic level inputs on the ClkDivA/B pins, and is shown in the table below - together with an indication of how various 'standard' data rates may be derived from common µP Xtal frequencies.

Note *that device operation is not guaranteed or specified above 19,200 bits/s or below 4,000 bits/s.*			**Xtal/Clock Frequency (MHz)**			
			4.096 [12.288/3]	4.9152	2.048 [6.144/3]	2.4576 [12.288/5]
ClkDiv A	**ClkDiv B**	**Division ratio Xtal Freq/ Data Rate**	**Data Rate (bps)**			
0	0	128			16000	19200
0	1	256	16000	19200	8000	9600
1	0	512	8000	9600	4000	4800
1	1	1024	4000	4800		

Table 1 Clock/Data Rates

Radio Channel Requirements

To achieve legal adjacent channel performance at high bit-rates, a radio with an accurate carrier frequency and an accurate modulation index will be required.

To achieve optimum channel utilization, (eg. low BER and high data-rates) attention must be paid to the phase and frequency response of both the IF and baseband circuitry.

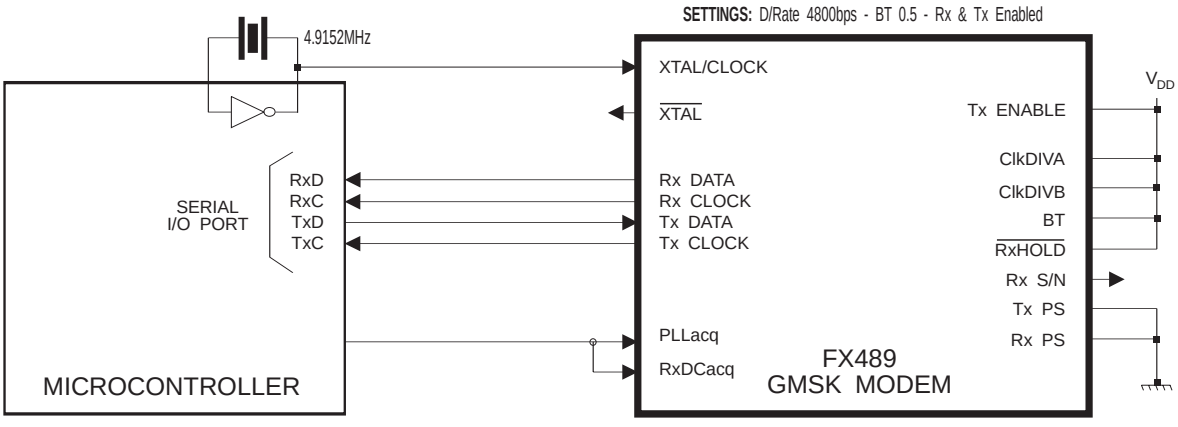


Fig.4 Minimum µController System Connections

Application Information .....

Rx Signal Path Description

The function of the Rx circuitry is to:

1. Set the incoming signal to a usable level.
2. Clean the signal by filtering.
3. Provide d.c. level thresholds for clock and data extraction.
4. Provide clock timing information for data extraction and external circuits.
5. Provide Rx data in a binary form.
6. Assess signal quality and provide Signal-to-Noise information.

The output of the radio receiver's Frequency Discriminator should be fed to the FX489's Rx Filter via a suitable gain and d.c. level adjusting circuit. This gain circuit can be built, with external components, around the on-chip Rx Input Amplifier, with the gain set so that the signal level at the Rx Feedback pin is nominally 1-volt peak-to-peak centred around V_{BIAS} when receiving a continuous "1111000011110000 .." data pattern.

Positive going signal excursions at Rx Feedback pin will produce a logic "0" at the Rx Data Output. Negative going excursions will produce a logic "1."

The received signal is fed through the lowpass Rx Filter, which has a -3dB corner frequency of 0.56 times the data bit-rate, before being applied to the Level Measure and Clock and Data extraction blocks.

The Level Measuring block consists of two voltage detectors. One of which measures the amplitude of the 'positive' parts of the received signal; The other measures the amplitude of the 'negative' portions. External capacitors are used by these detectors, via the Doc 1/2 pins, to form voltage- 'hold' or 'integrator' circuits. Results of the two measurements are then processed to establish the optimum d.c. level decision-thresholds for the Clock and Data extraction, depending upon the Rx signal amplitude, BT and any d.c. offset present.

Rx Circuit Control Modes

The operating characteristics of the Rx Level Measurement and Clock Extraction circuits are controlled, as shown in Table 2, by logic level inputs applied to the 'PLLacq,' 'Rx Hold' and 'RxDCacq' pins to suit a particular application, or to cope with changing reception conditions.

With reference to Figure 5, the Rx Mode Control diagram. In general, a data transmission will begin with a preamble of, for example, "1100110011001100," to allow the receive modem to establish timing- and level-lock as quickly as possible. After the Rx carrier has been detected, and during the time that the preamble is expected, the 'RxDCacq' and 'PLLacq' inputs should be switched from a logic "0 to 1" so that the Level Measuring and Clock Extraction modes are operated and sequenced as shown.

The 'Rx Hold' input should normally be held at a logic "1" while data is being received, but may be driven to a logic "0" to freeze the Level Measuring and Clock Extraction circuits during a fade. If the fade lasts for less than 200 bit periods, normal operation can be resumed by returning the 'Rx Hold' input to a logic "1" at the end of the fade. For longer fades, it may be better to reset the Level Measuring circuits by placing the 'RxDCacq' to a logic "1" for 10 to 20 bit periods.

'Rx Hold' has no effect on the Level Measuring circuits while 'RxDCacq' is at a logic "1," and has no effect on the PLL while 'PLLacq' is at a logic "1."

A logic "0" on 'Rx Hold' does not disable the 'Rx Clock' output, and the Rx Data Extraction and S/N Detector circuits will continue to operate.

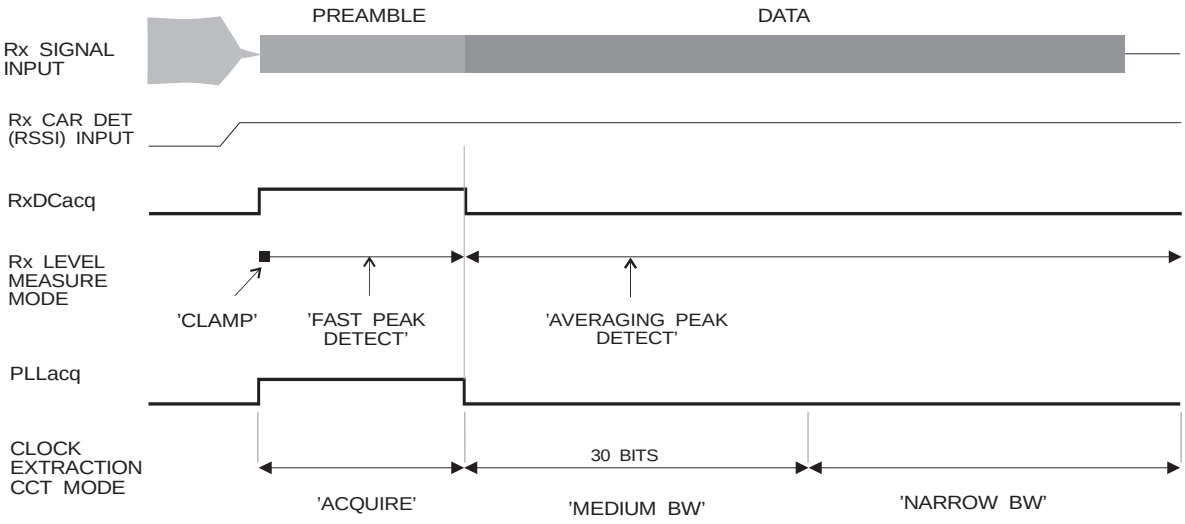


Fig.5 Rx Mode Control Diagram

Application Information .....

PLLacq	$\overline{\text{Rx Hold}}$	PLL Action
"1"	X	**Acquire:** Sets the PLL bandwidth wide enough to allow a lock to the received signal in less than 8 zero crossings. The Acquire mode will operate as long as PLLacq is a logic "1".
"1" to "0"	"1"	**Medium Bandwidth:** The correction applied to the extracted clock is limited to a maximum of ±1/16th bit-period for every two received zero-crossings. The PLL operates in this mode for a period of about 30 bits immediately following a "1" to "0" transition of the PLLacq input, provided that the Rx Hold input is a logic "1".
"0"	"1"	**Narrow Bandwidth:** The correction applied to the extracted clock is limited to a maximum of ±1/64th bit-period for every two received zero-crossings. The PLL operates in this mode whenever the Rx Hold Input is a logic "1" and PLLacq has been a logic "0" for at least 30 bit periods (after Medium Bandwidth operation for instance).
"0"	"0"	**Hold:** The PLL feedback loop is broken, allowing the Rx Clock to freewheel during signal fade periods.
RxDCacq	**$\overline{\text{Rx Hold}}$**	**Rx Level Measure Action**
"0" to "1"	X	**Clamp:** Operates for one bit-time after a "0" to "1" transition of the RxDCacq input. The external capacitors are rapidly charged towards a voltage mid-way between the received signal input level and V_{BIAS}, with the charge time-constant being of the order of 0.5bit-time.
"1"	X	**Fast Peak Detect:** The voltage detectors act as peak-detectors, one capacitor is used to capture the 'positive'-going signal peaks of the Rx Filter output signal and the other capturing the 'negative'-going peaks. The detectors operate in this mode whenever the RxDCacq input is at a logic "1," except for the initial 1-bit Clamp-mode time.
"0"	"1"	**Averaging Peak Detect:** Provides a slower but more accurate measurement of the signal peak amplitudes.
"0"	"0"	**Hold:** The capacitor charging circuits are disabled so that the outputs of the voltage detectors remain substantially at the last readings (discharging very slowly [time-constant approx. 2,000bits] towards V_{BIAS}).

Table 2 PLL and Rx Level Measurement Operational Modes

Rx Clock Extraction

Synchronized by a phased locked loop (PLL) circuit to zero-crossings of the incoming data, the 'Rx Clock Extraction' circuitry controls the 'Rx Clock' output. The Rx Clock is also used internally by the Data Extraction circuitry. The PLL parameters can be varied by the 'Rx Circuit Control' inputs PLLacq and Rx Hold to operate in one of four PLL modes as described in Table 2.

Rx Data Extraction

The 'Rx Data Extraction' circuit decides whether each received bit is a "1" or "0" by sampling the output of the Rx Filter in the middle of each bit-period, and comparing the sampled voltage against a threshold derived from the 'Level Measuring' circuit. This threshold is varied on a bit-by-bit basis to compensate for intersymbol interference depending on the chosen BT. The extracted data is output from the 'Rx Data' pin, and should be sampled externally on the rising edge of the 'Rx Clock.'

Rx S/N Detection

The 'Rx S/N Detector' system classifies the incoming zero-crossings as GOOD or BAD depending upon the time when each crossing actually occurs with respect to its expected time as determined by the Clock Extraction PLL. This information is then processed to provide a logic level output at the 'Rx S/N' pin.

By monitoring, and averaging, this output it is possible to derive a measure of the Signal-to-Noise-Ratio and hence the Bit-Error-Rate of the received signal.

Application Information .....

Bit Error Rate Performance

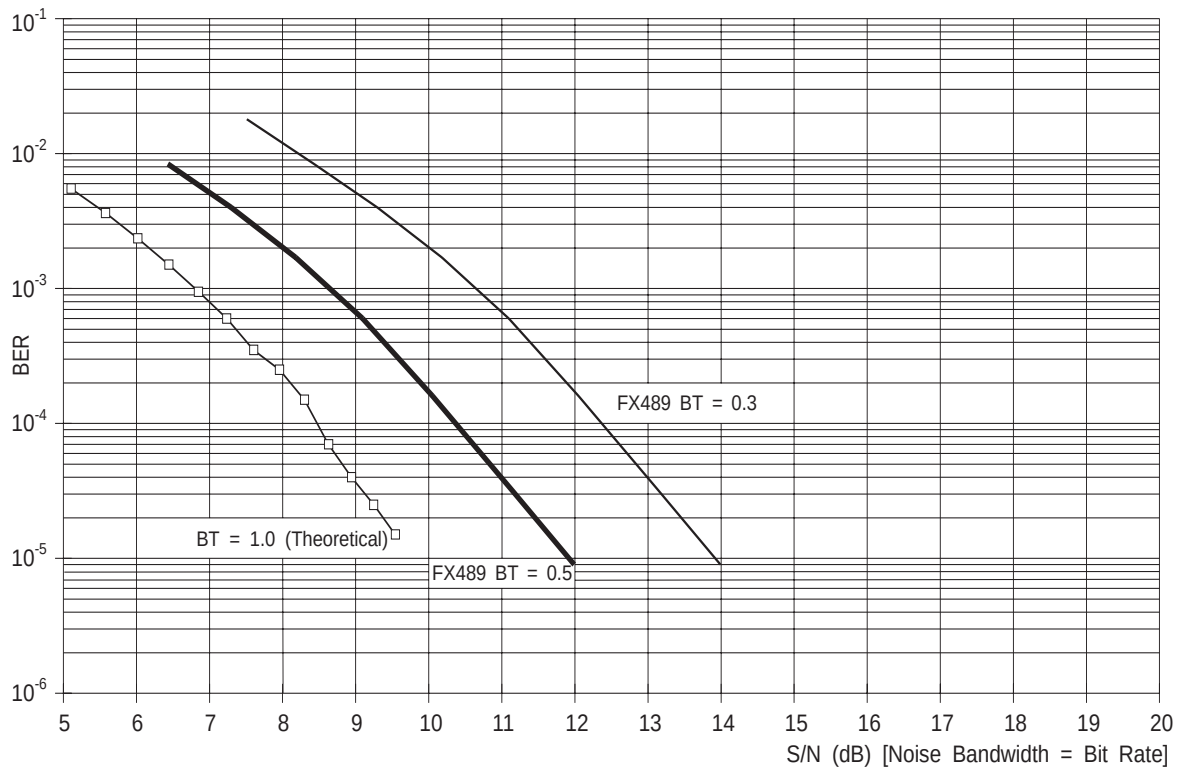


Fig. 6 Typical Bit-Error-Rate Performance

Rx Signal Quality

Figure 7 shows, diagramatically, the effect of input Rx signal quality on the “Rx S/N” output.

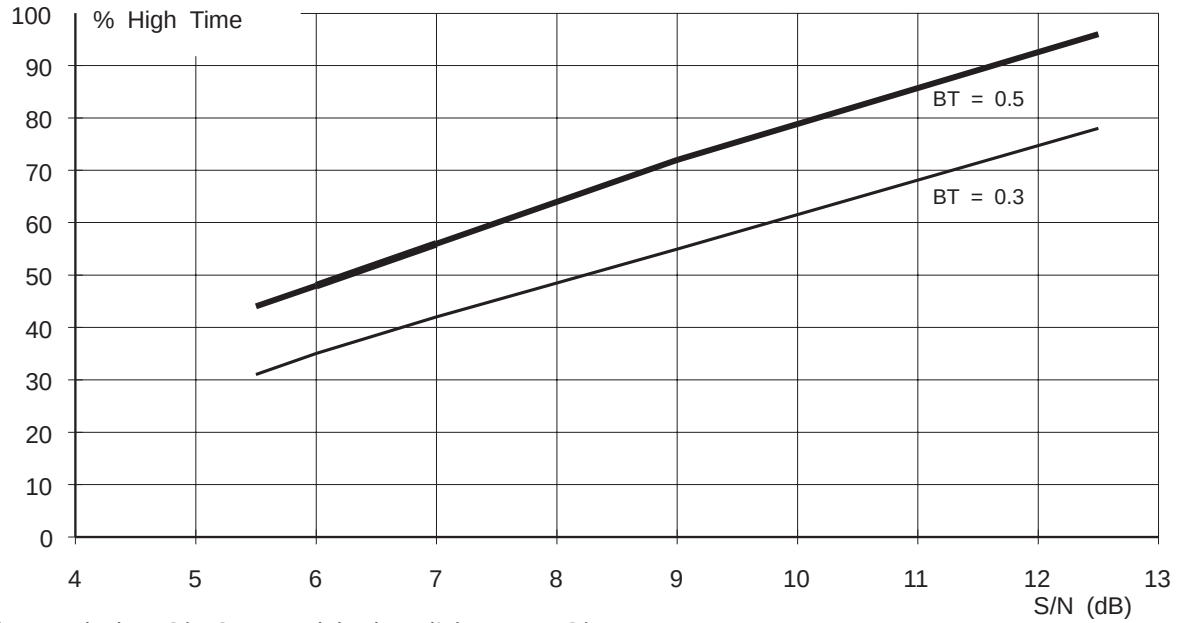


Fig.7 Typical Rx S/N Output ‘High-Time’ (%) vs Input S/N

Application Information .....

Tx Signal Path Description

The binary data applied to the 'Tx Data' input is retimed within the chip on each rising edge of the 'Tx Clock' and then converted to a 1-volt peak-to-peak binary signal centred about V_{BIAS}.

If the 'Tx Enable' input is 'high,' then this internal binary signal will be connected to the input of the lowpass Tx Filter, and the output of the filter connected to the 'Tx Out' pin.

Tx Enable	Tx Filter Input	Tx Out Pin
'1' (high)	1 volt p-p Data In	Filtered Data
"0" (low)	V_{BIAS}	V_{BIAS} via 500kΩ

A 'low' input to the 'Tx Enable' will connect the input of the Tx Filter to V_{BIAS}, and disconnect the 'Tx Out' pin from the filter, connecting it instead to V_{BIAS} through a high resistance (nominally 500kΩ).

The Tx Filter has a lowpass frequency response, which is approximately gaussian in shape as shown in Figure 9, to minimise amplitude and phase distortion of the binary signal while providing sufficient attenuation of the high frequency-components which would otherwise cause interference into adjacent radio channels. The actual filter bandwidth to be used in any particular application will be determined by the overall system requirements. The attenuation-vs-frequency response of the transmit filtering provided by the FX489 have been designed to meet the specifications for most GMSK modem systems, having a -3dB bandwidth switchable between 0.3 and 0.5 times the data bit-rate (BT).

Note that an external RC network is required between the 'Tx Out' pin and the input to the Frequency Modulator (see Figures 2 and 3). This network, which can form part of any d.c. level shifting and gain adjustment circuitry, forms an important part of the transmit signal filtering, and the ground connection to the capacitor C_1 should be positioned to give maximum attenuation of high-frequency noise into the modulator.

The component values should be chosen so that the product of the resistance (Ohms) and the capacitance (Farads) is:

BT of 0.3 = 0.34/bit rate (bits/second)

BT of 0.5 = 0.22/bit rate (bits/second)

with suitable values for common bit rates being:

	R	C
8000 bits/sec, BT = 0.3	91.0kΩ	470pF
4800 bits/sec, BT = 0.5	100kΩ	470pF
9600 bits/sec, BT = 0.5	47.0kΩ	470pF

The signal at 'Tx Out' is centred around V_{BIAS}, going positive for logic "1" (high) level inputs to the 'Tx Data' input and negative for logic "0" (low) inputs.

When the transmit circuits are put into a 'powersave' mode (by a logic "1" to the 'Tx PS' pin) the output voltage of the Tx Filter will go to V_{SS}. When power is subsequently restored to the Tx Filter, its output will take several bit-times to settle. The 'Tx Enable' input can be used to prevent these abnormal voltages from appearing at the 'Tx Out' pin.

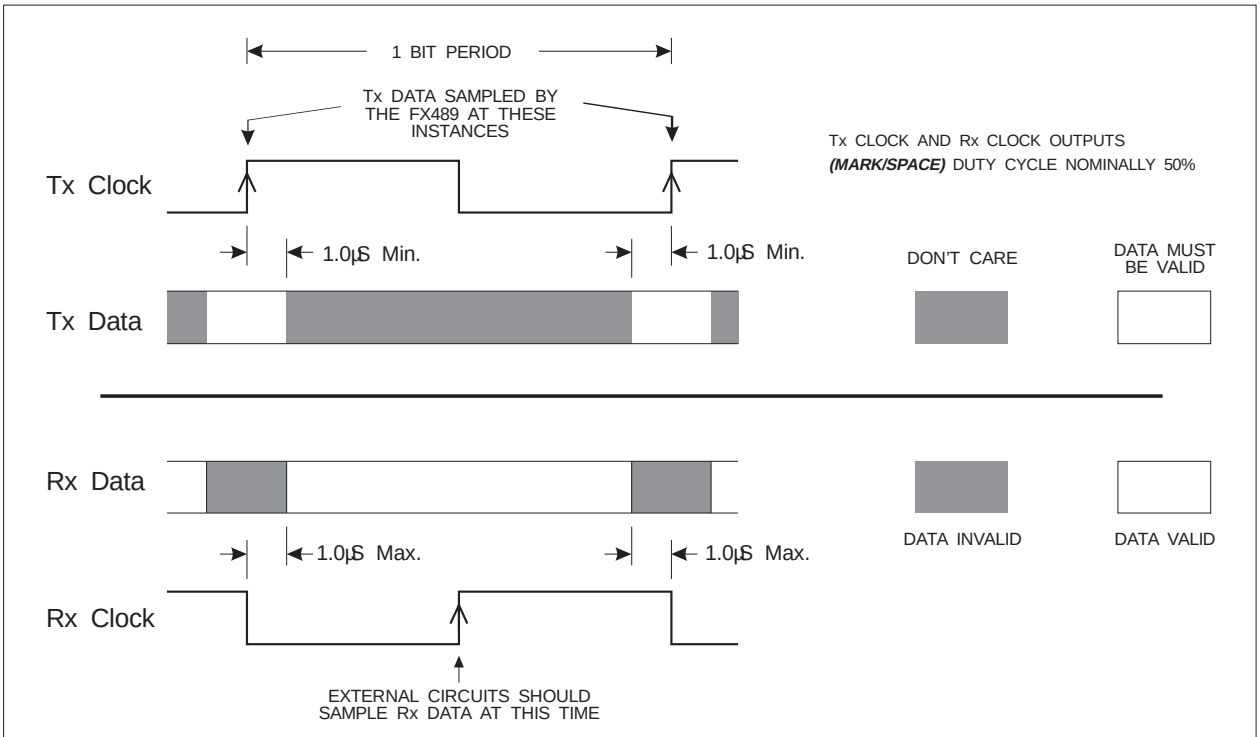


Fig.8 Rx and Tx Clock Data Timings

Application Information .....

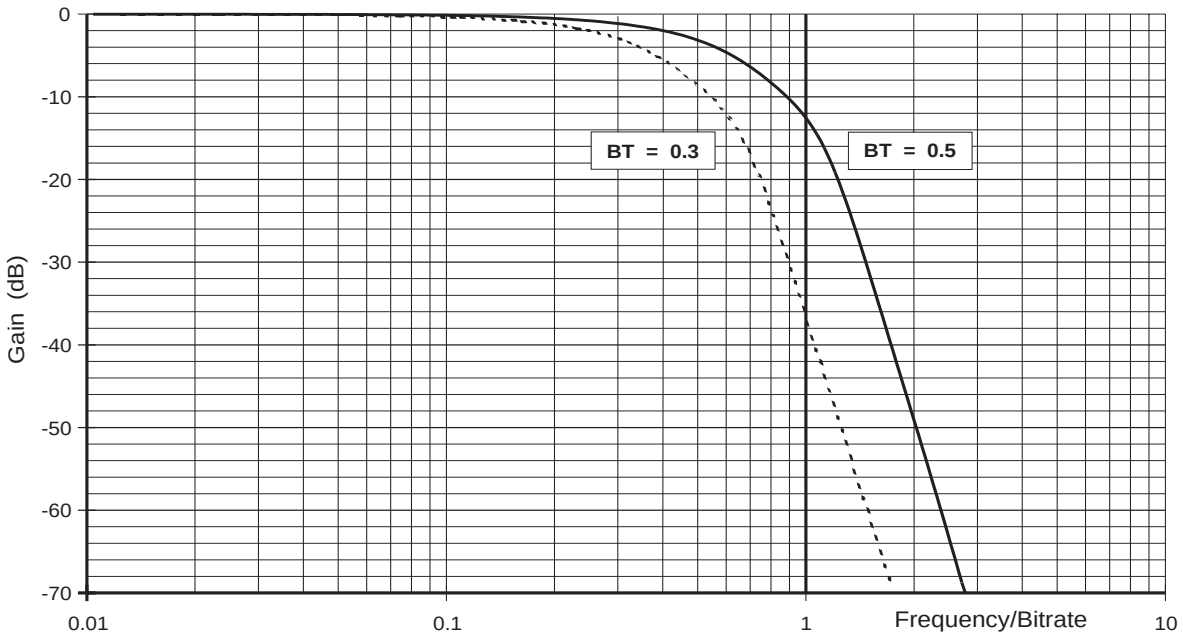


Fig.9 Tx Filter Response

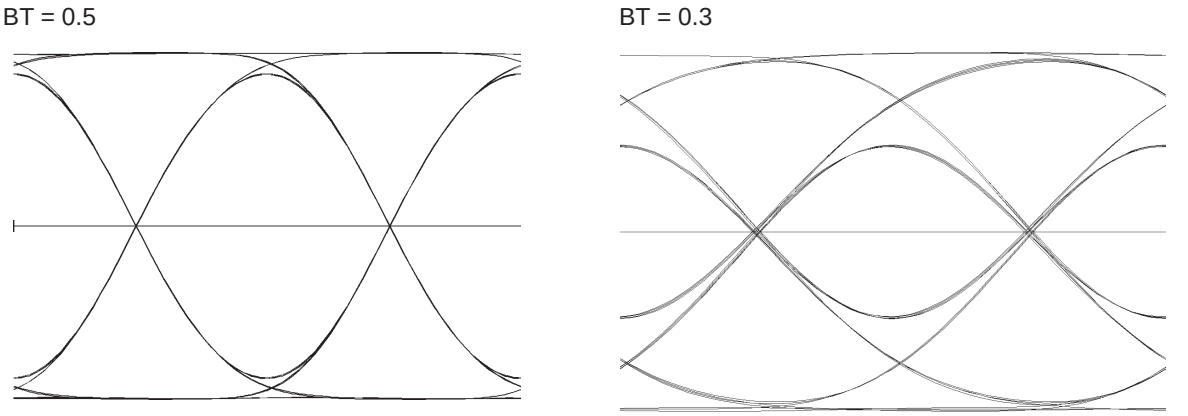


Fig.10 Typical Transmit Eye Patterns

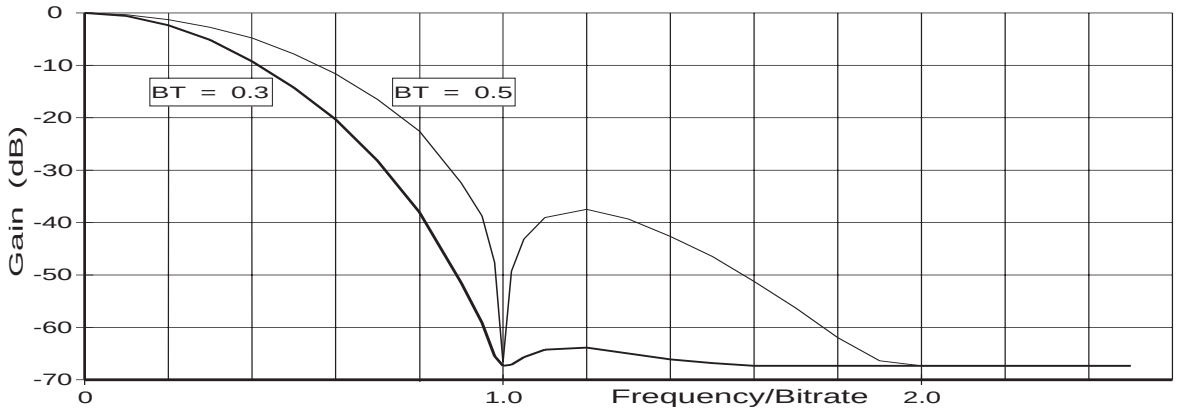


Fig.11 Tx Output Spectrum (Random Data)

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)		+/- 30mA
(other pins)		+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX489DW/P**	-40°C to +85°C
Storage temperature range:	**FX489DW/P**	-40°C to +85°C

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V, T_{AMB} = 25°C. Xtal/Clock Frequency = 4.096MHz. Data Rate = 8000 bits/sec.
Noise Bandwidth = Bit Rate

Characteristics	Tx PS	Rx PS	See Note	Min.	Typ.	Max.	Unit
Static Values							
Supply Voltage (V_{DD})				4.5	5.0	5.5	V
Supply Current	**Tx PS**	**Rx PS**	1				
	1	1		-	1.0	-	mA
	0	1		-	3.0	-	mA
	1	0		-	4.0	-	mA
	0	0		-	7.0	-	mA
Input Logic Levels							
Logic “1”				3.5	-	-	V
Logic “0”				-	-	1.5	V
Logic Input Current			2	-5.0	-	5.0	µA
Logic “1”Output Level at IOH = -120µA				4.6	-	-	V
Logic “0”Output Level at IOL = 120µA				-	-	0.4	V
Rx, Tx Data Rate				4000		19200	bits/sec
Transmit Parameters							
Tx OUT, Output Impedance			3	-	1.0	-	kΩ
Tx OUT, Level			4	0.8	1.0	1.2	V p-p
Tx Data Delay (BT = 0.3)			5	-	2.0	2.5	bit-periods
(BT = 0.5)			5	-	1.5	2.0	bit-periods
Tx PS to Output-Stable Time			6	-	4.0	-	bit-periods
Receive Parameters							
Rx Amplifier -							
Input Impedance				1.0	-	-	MΩ
Output Impedance			7	-	10.0	-	kΩ
Voltage Gain				-	50.0	-	dB
Rx Filter Signal Input Level			8	0.7	1.0	1.3	V p-p
Rx Time Delay			9	-	-	3.0	bit-periods
On-Chip Xtal Oscillator							
R_{IN}				10.0	-	-	MΩ
R_{OUT}				5.0	-	15.0	kΩ
Voltage Gain				-	15.0	-	dB
Xtal/Clock Frequency				1.0	–	5.0	MHz
“High” Pulse Width			10	80.0	-	-	ns
“Low” Pulse Width			10	80.0	-	-	ns

Notes

1. Not including current drawn from the FX489 pins by external circuitry. See Absolute Maximum Ratings.
2. For V_{IN} in the range V_{SS} to V_{DD}.
3 For a load of 10kΩ or greater. Tx PS input at logic “0”; Tx Enable = “1”.
4. Data pattern of “1111000011110000 ..”
5. Measured between the rising edge of ‘Tx Clock’ and the centre of the corresponding bit at ‘Tx Out.’
6. Time between the falling edge of ‘Tx PS’ and the ‘Tx Out’ voltage stabilising to normal output levels.
7. For a load of 10kΩ or greater. Rx PS input at logic “0”.
8. For optimum performance, measured at the ‘Rx Feedback’ pin for a “1111000011110000 ...” pattern.
9. Measured between the centre of bit at ‘Rx Signal In’ and corresponding rising edge of the ‘Rx Clock’.
10. Timing for an external clock input to the Xtal/Clock pin.

Package Outlines

The FX489DW, the Small Outline Integrated Circuit (S.O.I.C.) package is shown in Figure 12 and the 'P' plastic version in Figure 13.
Pin 1 identification marking is shown on the relevant diagram and pins on both package styles number anti-clockwise when viewed from the top (marked side).

Handling Precautions

The FX489 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

Fig.12 ***FX489DW 24-pin S.O.I.C. Package***

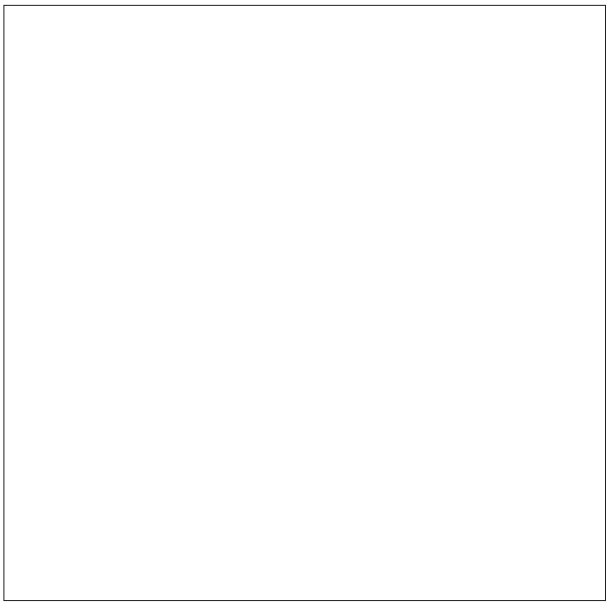
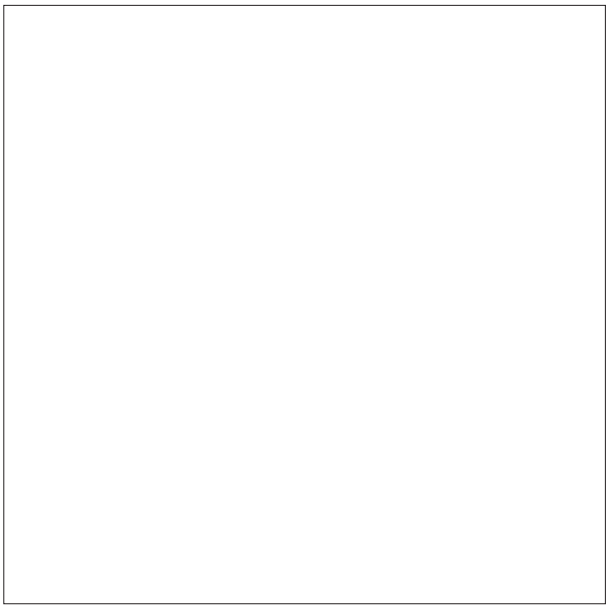


Fig.13 ***FX489P 24-pin plastic Package***



Ordering Information

FX489DW 24-pin plastic S.O.I.C.

FX489P 24-pin plastic DIL