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GC4116

MULTI-STANDARD QUAD DUC CHIP

DATA SHEET

REV 1.0

APRIL 27, 2001

This datasheet may be changed without notice.

REVISION HISTORY

Revision	Date	Description
0.1	Feruary 8, 2000	Original
0.2	March 22, 2000	Corrected typos, and miscellaneous errors.
0.3	October 31, 2000	Rewritten throughout to reflect new modes, final design changes
1.0	April 27, 2001	Modified to reflect Production specifications. Changes throughout.

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1.0 KEY FEATURES

- Output rates up to 100 MSPS
- Four identical up-convert channels
- 16 bit real or complex inputs
- Four bit serial input ports, or memory mapped input registers
- Serial interface controller simplifies interfacing with ASICs or DSP chips
- Resampler circuit filters, pulse shapes and resamples data to allow arbitrary input to output sample rate conversion
- Interpolation factors of
  32 to 5,792 in each channel
  16 to 32 by combining two channels
- Independent frequency, phase and gain controls
- User programmable 63 tap input filter
- 0.02 Hz tuning resolution
- 115 dB Spur Free Dynamic Range
- 90 dB or more image rejection
- 0.07 dB gain resolution
- 0.05 dB peak to peak passband ripple
- The four channels are summed into a single output signal
- 22 bit sum I/O path to merge outputs from multiple GC4116 chips
- 8 to 22 bit 2's complement or offset binary output samples
- Accepts QPSK or QAM symbol data directly, performs transmit (pulse shape) filtering
- Performs pulse shaping and phase equalization for IS95 and CDMA2000
- Exceeds Damps, GSM, & IS95 requirements
- Supports up to two 4 Mbaud channels.
- Microprocessor interface for control
- Built in diagnostics
- Each GC4116 chip upconverts:
  Four GSM, DAMPS, or 1X CDMA carriers, or
  Two 3X CDMA2000 carriers, or
  Two 3.84MB UMTS carriers
- Power consumption at 70 MHz, 2.5 volts:
  84 mW per DAMPS channel
  107 mW per GSM channel
  305mW per 3.84MB UMTS channel
- Industrial temperature range (-40C to +85C)
- GC4016-PB 160 ball PBGA
  (15mm by 15mm) package
- 3.3volt I/O voltage, 2.5volt core voltage
- JTAG Boundary Scan

2.0 BLOCK DIAGRAM

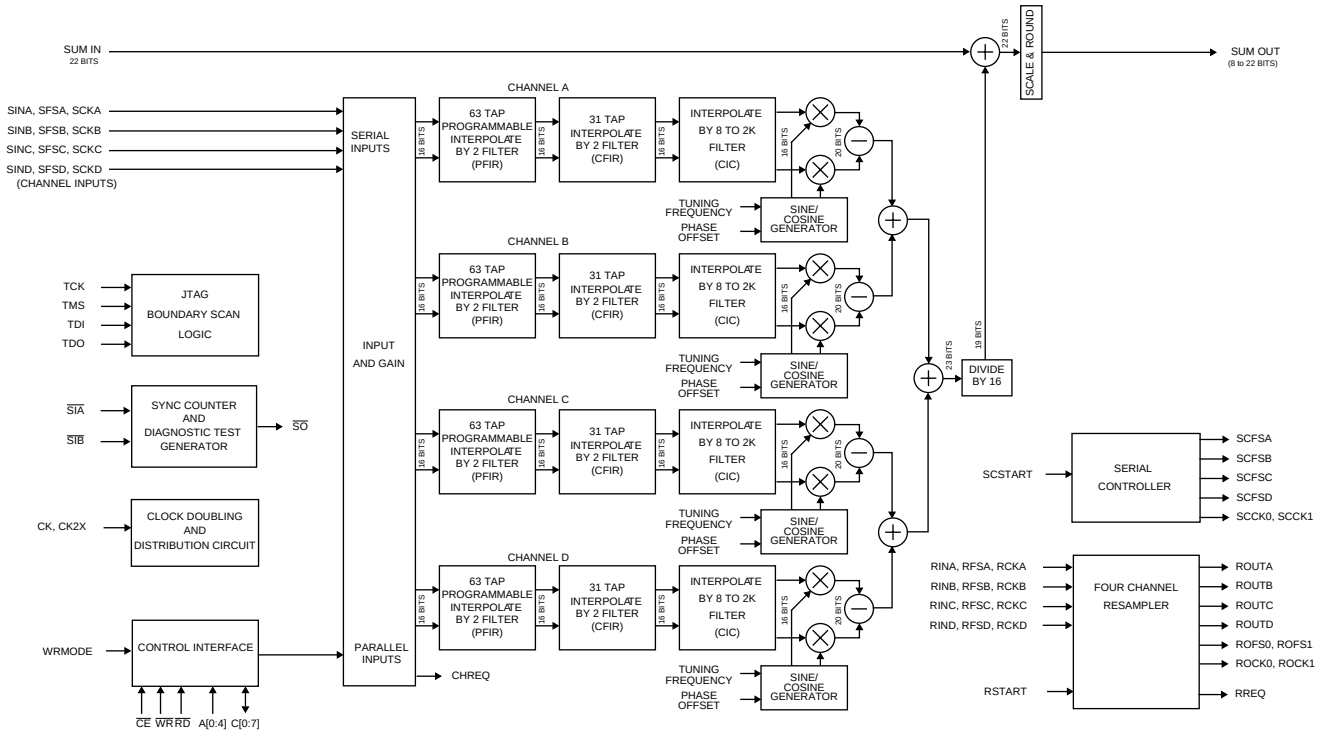


Figure 1. GC4116 Block Diagram

3.0 FUNCTIONAL DESCRIPTION

The GC4116 quad transmit chip contains four identical up-conversion channels. The up-convert channels accept real or complex signals, interpolate them by programmable amounts ranging from 32 to 5,792, and modulates them up to selected center frequencies. The modulated signals are then summed together and optionally summed with modulated signals from other GC4116 chips. Channels can be used in pairs to reduce the interpolation ratio down to 16 in order to process wider band input signals.

Each channel contains a user programmable input filter (PFIR) which can be used to shape the transmitted signal's spectrum, or can be used as a Nyquist transmit filter for shaping digital data such as QPSK, GMSK or QAM symbols (See Section 7 for example applications).

The up-converter channels are designed to maintain over 115 dB of spur free dynamic range. Each up-convert channel accepts 16 bit inputs (bit serial) and produces 20 bit outputs. The up-converter outputs are summed with an external 22 bit input to produce a single 22 bit output. The chip can output either real or complex data. The frequencies and phase offsets of the four sine/cosine sequence generators can be independently specified, as can the gain of each circuit. Each channel interpolates by the same amount, but can be programmed with independent PFIR coefficients. Channels can be synchronized to support beamformed or frequency hopped systems.

An independent resampler block performs resampling on up to 4 signals. The resampler has its own input and output pins so that it can be used independently from the up-convert channels. The resampler engine is identical to the one in the gc4016. It provides a user programmable filter up to 512 taps long and allows for sampling by arbitrary amounts with delay resolutions up to 64 time phases.

A serial controller block is used to generate serial clocks and frame strobes for the channel and resampler input ports. This block simplifies interfacing the GC4116 to other devices.

On chip diagnostic circuits are provided to simplify system debug and maintenance.

The chip receives configuration and control information over a microprocessor compatible bus consisting of an 8 bit data I/O port, a 5 bit address port, a chip enable strobe, a read strobe and a write strobe. The chip's 110 control registers (8 bits each) and five coefficient RAM's are memory mapped into the 5 bit address space of the control port using an internal page register.

3.1 CONTROL INTERFACE

The chip is configured by writing control information into control registers within the chip. The control registers are grouped into 8 global registers and 64 pages of registers, each page containing up to 16 registers. The global registers are accessed as addresses 0 through 15. Address 15 is the page register which selects which page is accessed by addresses 16 through 31. The contents of these control registers and how to use them are described in Section 5.

The registers are written to or read from using the **C[0:7]**, **A[0:4]**, $\overline{\textbf{CE}}$, $\overline{\textbf{RD}}$ and $\overline{\textbf{WR}}$ pins. Each control register has been assigned a unique address within the chip. This interface is designed to allow the GC4116 chip to appear to an external processor as a memory mapped peripheral (the pin $\overline{\textbf{RD}}$ is equivalent to a memory chip's $\overline{\textbf{OE}}$ pin).

An external processor (a microprocessor, computer, or DSP chip) can write into a register by setting **A[0:4]** to the desired register address, selecting the chip using the $\overline{\textbf{CE}}$ pin, setting **C[0:7]** to the desired value and then pulsing $\overline{\textbf{WR}}$ low. The data will be written into the selected register when both $\overline{\textbf{WR}}$ and $\overline{\textbf{CE}}$ are low and will be held when either signal goes high. An alternate "edge write" mode can be used to strobe the data into the selected register when either $\overline{\textbf{WR}}$ or $\overline{\textbf{CE}}$ goes high. This is useful for processors that do not guarantee valid data when the write strobe goes active, but guarantee that the data will be stable for the required set up time before the write strobe goes inactive. The edge write is necessary for these processors, as some control registers (such as most sync registers) are sensitive to transient values on the **C[0:7]** data bus.

To read from a control register the processor must set **A[0:4]** to the desired address, select the chip with the $\overline{\textbf{CE}}$ pin, and then set $\overline{\textbf{RD}}$ low. The chip will then drive **C[0:7]** with the contents of the selected register. After the processor has read the value from **C[0:7]** it should set $\overline{\textbf{RD}}$ and $\overline{\textbf{CE}}$ high. The **C[0:7]** pins are turned off (high impedance) whenever $\overline{\textbf{CE}}$ or $\overline{\textbf{RD}}$ are high or when $\overline{\textbf{WR}}$ is low. The chip will only drive these pins when both $\overline{\textbf{CE}}$ and $\overline{\textbf{RD}}$ are low and $\overline{\textbf{WR}}$ is high.

One can also ground the $\overline{\textbf{RD}}$ pin and use the $\overline{\textbf{WR}}$ pin as a read/write direction control and use the $\overline{\textbf{CE}}$ pin as a control I/O strobe. Figure 2 shows timing diagrams illustrating both I/O modes.

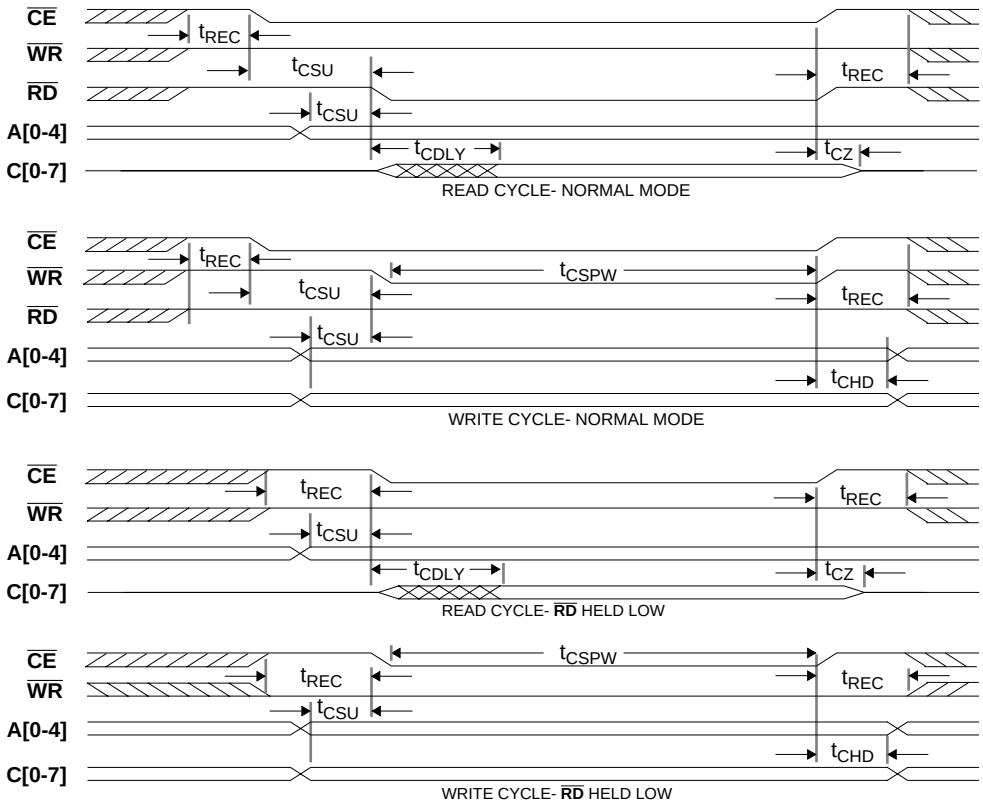


Figure 2. Normal Control I/O Timing

The edge write mode, enabled by the **WRMODE** input pin, allows for rising edge write cycles. In this mode the data on the **C[0:7]** pins only need to be stable for a small setup time before the rising edge of the write strobe, and held for a small hold time afterwards. This mode is appropriate for processors that do not provide stable data before the start of the write pulse. Figure 3 shows the timing for this mode.

The setup, hold and pulse width requirements for control read or write operations are given in Section 6.0.

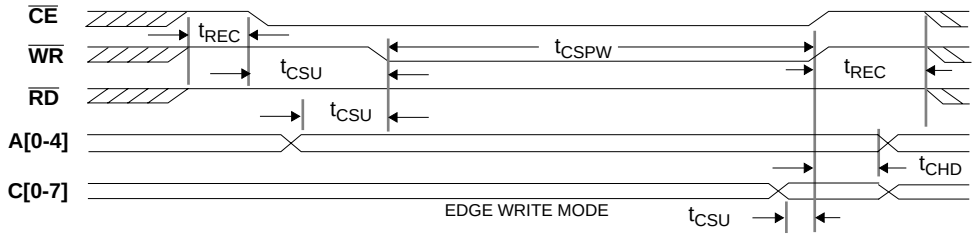


Figure 3. Edge Write Control Timing

3.2 CHANNEL INPUT FORMAT

The input samples are 16 bits, either real or complex. The samples are input to the chip either through the bit-serial input ports, or through memory mapped control registers. The channel data request signal (CHREQ) is output from the chip to identify when the GC4116 is ready for another complex input sample or pair of real samples.

3.2.1 Bit Serial Interface

The bit serial format consists of a data input pin (SIN), a bit clock pin (SCK), and a frame strobe pin (SFS) for each of the four channels (A,B,C and D), and a channel data request pin (CHREQ) which is common to all channels.

The serial channel inputs can come directly from the Four Channel Resampler by connecting the resampler's serial output ports to the channel's serial input ports, and connecting the CHREQ pin to the resampler's RSTART pin. The Resampler and its I/O interface is described in Section 3.7.

If the Resampler is not being used, then the Serial Controller can be used to generate the proper serial clocks and frame strobes fro the channel inputs. In this case CHREQ is tied to SCSTART, and then SCCK and the SCFS strobes are used to drive the serial clock and frame strobes for both the channel inputs and the channel data source (typically a DSP chip, FPGA, or ASIC).

The bit serial samples are always entered MSB first. Complex values are entered I-half first followed by the Q-half. Real values are entered as pairs of samples, with the first sample in the I-half and the second sample in the Q-half. The input accepts either pairs of 16 bit words each with its own frame strobe (the unpacked mode), or as a single 32 bit transfer with a single frame strobe (the packed mode). The bit serial input formats are shown in Figure 4

Figure 4a shows the unpacked input mode (PACKED in the input control register is low). The user provides a bit serial clock (SCK), a frame strobe (SFS) and a data bit line (SIN). The chip clocks SFS and SIN into the chip on the rising edge of SCK (or falling edge if the SCK_POL bit in the input control register is set). The user sends a 16 bit serial input word to the GC4116 by setting SFS high (or low if SFS_POL in the input control register is set) for one SCK clock cycle, and then transmitting the data, MSB first, on the next 16 SCK clocks. The SFS may remain high during the transfer, but must go low for one SCK cycle before the next serial word is sent. The serial sample is transferred to a parallel register on the next SCK clock. Additional SCK clocks are acceptable but are ignored. The data can be transmitted "back to back" as shown in Figure 4b as long as the SFS signal toggles low and then high as shown. If the PACKED control bit is high, then the I and Q samples (or I0 then I1 for real data) are sent as a single 32 bit word with only one SFS strobe as shown in Figure 4c.:

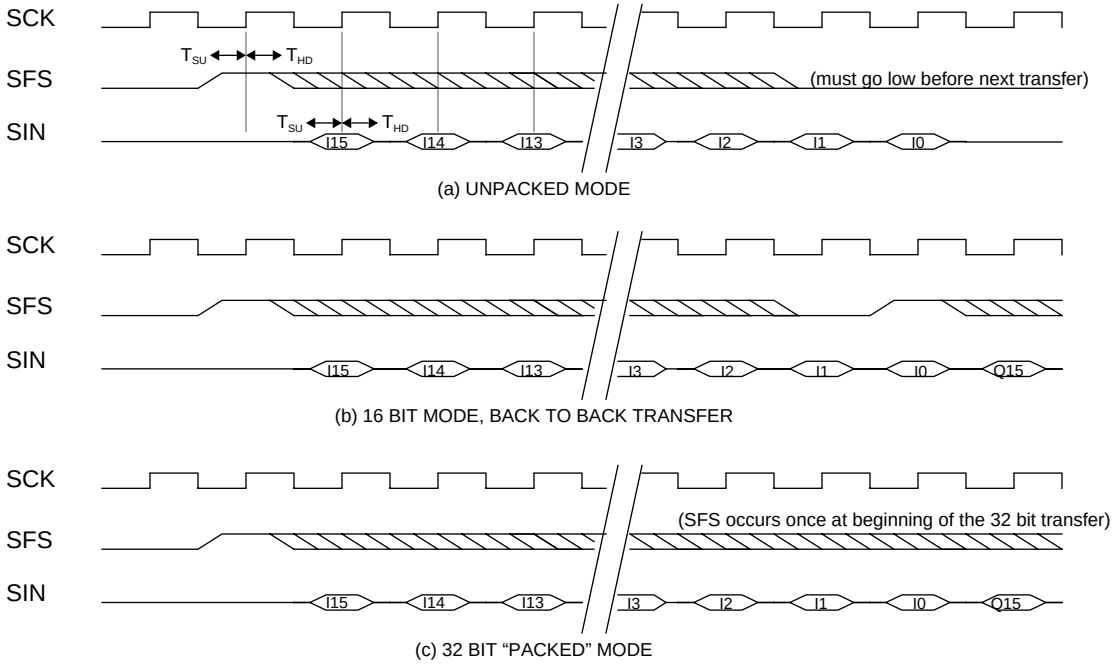


Figure 4. Serial Input Formats

The GC4116 input interface sends a channel data request strobe (CHREQ) when a new input sample is required for the up-converter channels. The CHREQ strobe is output from the chip every 4N clocks, where N is the interpolation ratio in the CIC filter. The pulse width of the CHREQ strobe is one CK period. The polarity of CHREQ is user programmable. The CHREQ strobe is typically connected to SCSTART of the serial request controller, or to RSTART of the resampler (See Section 3.7.9). CHREQ can also be used as an interrupt to an external device to tell it to send another input sample. The GC4116 chip must receive the last data bit at least one bit clock (SCK) period before the next CHREQ strobe.

The frame sync can be sent up to 7 bit clocks before CHREQ. This is normally used when the serial interface timing is tight, i.e., the CHREQ rate is less than 34 SCK cycles, so that there is not time between CHREQ strobes to send SFS, then 32 bits and then have an SCK cycle before the next CHREQ.

Very Important Note: The chip requires that SCK be active when frame sync occurs, and be active for one cycle after the last bit is sent. Serial data can be sent using only 32 SCK clocks per CHREQ period if the frame sync for the 16 bit I word (or the 32 bit I/Q word in the PACKED mode) is coincident with the last bit of the previous transfer. The Serial Controller block described in Section 3.8 can provide appropriately timed frame strobes and serial clocks.

3.2.2 Memory Mapped Interfaced

Input samples can be entered into the chip using the control interface. Addresses 16 through 31 on page 3 are the input data registers. Note that these registers can be written to in a DMA burst, 8 bits at a time. Note that some DMA formats write samples most significant byte first. If this is the case then the DMA should write from address 31 down to address 16. The CHREQ strobe from the GC4116 chip defines when the DMA transfer can start. The transfer must be done before the next CHREQ strobe is received. See global address 14 for handshake details.

3.3 THE UP-CONVERTERS

Each up-converter channel uses a two stage interpolate by four filter and a 5 stage cascaded integrate-comb (CIC) filter to increase the sample rate of the input data up to the chip's clock rate. An NCO and mixer circuit modulates the signal up to the desired center frequency.

A block diagram of each up-convert channel is shown in Figure 5. Each input sample is multiplied by an 8 bit 2's complement gain word. The gain adjustment is GAIN/128, where the gain word (GAIN) ranges from -128 to +127. This gives a 42 dB gain adjustment range. Setting G to zero clears the channel input. A different gain can be specified for each channel. The gain values are double buffered and may be transferred to the active register on a sync. The transfer is delayed so that the new values take effect on the same sample for all channels. Gain is described in more detail in Section 3.6.

After the gain has been applied, the input samples are interpolated by a factor of 2 in a 63 tap filter with programmable coefficients (PFIR). A typical use of the PFIR is to implement matched (root-raised-cosine) transmit filters.

The PFIR will also, if desired, convert real input data to single-sideband complex data. In this mode the PFIR does not interpolate by a factor of 2. Instead it down-converts the input data by $F_S/4$, where F_S is the input sample rate, and low pass filters the result.

The second interpolate by 2 filter is a 31 tap compensating filter (CFIR) which both interpolates by 2 and pre-compensates for the droop associated with the CIC filter that follows it.

The CIC filter interpolates by another factor of N=(8 to 1,448) to give an overall interpolation factor of 32 to 5,792 (16 to 2,896 in the real input mode).

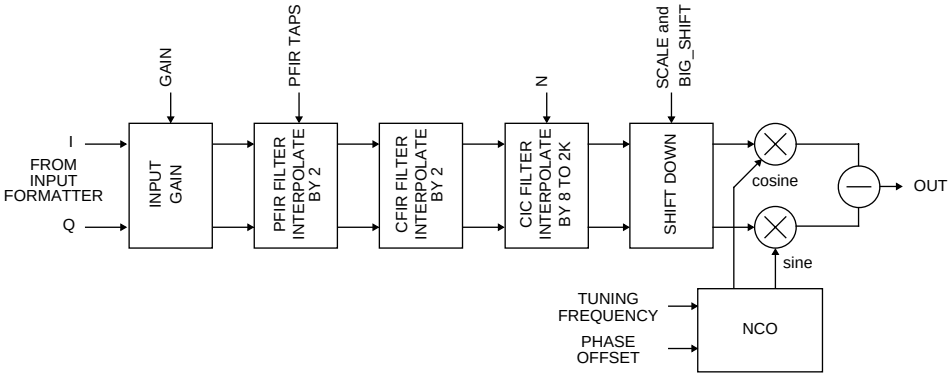


Figure 5. The Up-converter Channel

The interpolated signal is modulated by a sine/cosine sequence generated by the NCO. In the real output mode the real part (I-half) of the complex result is saved as the channel output.

In the complex output mode the CIC interpolation is cut in half and the NCO/mixer calculates both the I-half and Q-half of the complex result. In this mode the complex output sample rate is one-half the clock rate, with the I and Q halves multiplexed together onto the same output bus.

3.3.1 The Programmable Interpolate By 2 Filter (PFIR)

The input samples are filtered by two stages of interpolate by 2 filtering before they are interpolated by the CIC filter. The first stage interpolate by two filter is a 63 tap filter with programmable 16 bit coefficients. The PFIR will accept either complex or real input data. If the input samples are complex, the filter doubles the input rate by inserting zeroes between each sample, and then low pass filters the result. If the input samples are real (REAL in address 1 is set), the filter translates the real samples down by $F_{IN}/4$, where F_{IN} is the input sample rate, by multiplying them by the complex sequence +1, -j, -1, +j, …, and then lowpass filters the result. This generates a single-sideband modulation of the real input. Note that in the real input mode the data is entered as pairs of samples packed into the complex input word format (see Section 3.2). If double sideband real upconversion is desired, then the chip should be operated in the complex mode with the Q-half of each complex pair set to zero.

The PFIR filter passband must be flat in the region of the signal of interest, and have the desired out of band rejection in the region that will contain the interpolation image. Figure 6 illustrates the passband and stopband requirements of the filter. F_{IN} is the input sample rate to the channel. $2F_{IN}$ is the output sample rate of the PFIR. A common use of the PFIR is to pulse shape digital data. The PFIR will accept QPSK, O-QPSK, PSK, PAM, OOK, π/4-QPSK, or QAM symbols and then filter them by the desired pulse shaping filter, which is commonlt a root-raised-cosine (RRC) filter. The symbols can be entered directly into the chip at the desired symbol (baud) rate. The application notes in Section 7 describes sample filter coefficients sets for common standards (DAMPS, GSM, IS95, UMTS).

Each channel has its own PFIR coefficient memory, so the same filter, or a different filter, can be used in each channel.

The user downloaded filter coefficients are 16 bit 2's complement numbers. Unity gain will be achieved through

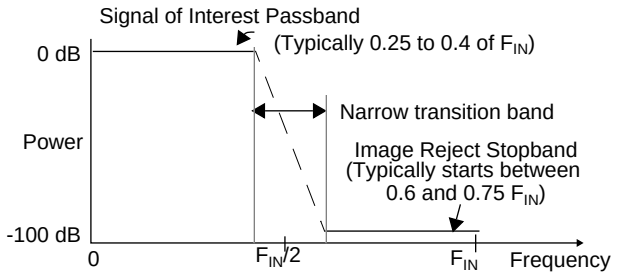


Figure 6. Typical PFIR Specifications

the filter if the sum of the 63 coefficients is equal to 65536. If the sum is not 65536, then PFIR will introduce a gain equal to: $\text{PFIR\_GAIN} = \frac{\text{PFIR\_SUM}}{65536}$, where PFIR_SUM is the sum of the 63 coefficients.

The 63 coefficients are identified as coefficients h_0 through h_{62}, where h_{31} is the center tap. The coefficients are assumed to be symmetric, so only the first 32 coefficients (h_0 through h_{31}) are loaded into the chip. A non-symmetric mode (NO_SYM_PFIR in address 26) allows the user to download a 32 tap non-symmetric filter as taps h_0 through h_{31}. The newest sample is multiplied by h31 and the oldest is multiplied by h_{01}.

3.3.2 The Compensating Interpolate by 2 Filter (CFIR)

The second stage filter is a fixed coefficient 31 tap interpolate by 2 filter. The second stage filter always interpolates by a factor of two. The second filter has a passband which is flat (0.01 dB ripple) out to $0.6F_{IN}$ and provides over 90dB of image rejection beyond $1.4F_{IN}$. The second filter also compensates for the droop associated with the CIC interpolation filter described in the next section. The 16 unique coefficients of the symmetric filter are:

```
-34, -171, -166, 403, 837, -317, -1983, -790,
2820, 3328, -1667, -6589, -4024, 7232, 20602,
26577
```

The passband of this filter is wide enough to upconvert digital symbol data with excess bandwidths up to 0.35.

The CFIR output is scaled to have unity gain.

The output rate of the CFIR filter is $4F_{IN}$ in the complex input mode and is $2F_{IN}$ in the real input mode. The CFIR output rate relative to the clock rate is F_{CK}/N

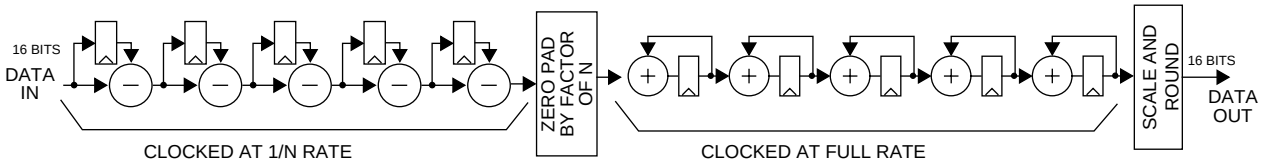


Figure 7. Five Stage CIC Interpolate by N Filter

3.3.3 The CIC Interpolate by N Filter

The CFIR output is interpolated by a factor of N in the CIC[1] filter, where N is any integer between 8 and 1,448. The filter is a 5 stage CIC filter. A block diagram of the CIC filter is shown in Figure 7.The output of the CIC interpolation filter is equal to the clock rate. The CIC filter has a gain equal to N^4 which must be removed by the "SCALE AND ROUND" circuit shown in Figure 7. This circuit has a gain equal to $2^{-(3+SCALE+12*BIG\_SHIFT)}$, where SCALE ranges from 0 to 15 and BIG_SHIFT ranges from 0 to 2. The value chosen for BIG_SHIFT must also satisfy: $2^{(12*BIG\_SHIFT+18)} \geq N^4$. Overflows due to improper gain settings will go undetected if this relationship is violated. This restriction means that N must be less than 23 for BIG_SHIFT = 0, N must be less than 182 for BIG_SHIFT = 1, and N must be less than 1449 for BIG_SHIFT = 2. Larger interpolation amounts can be achieved by using the resampler to perform interpolation. Larger interpolation amounts using the CIC can be accomplished only by reducing the signal amplitude feeding the CIC.

The CIC filter must be initialized when the chip is first configured or whenever the interpolation value N or the shift value BIG_SHIFT are changed. The CIC filter is initialized using the flush controls described in Section 5.8. If the CIC is disturbed during processing due to noise, radiation particles, or due to changing N or BIG_SHIFT, then the CIC will generate wideband white noise in the output. This property is inherent in the mathematics of a CIC filter used for interpolation. This instability can be prevented by using the "auto flush" capability of the chip[2] (See DISABLE_AUTO_FLUSH in control register 13). The auto flush mode detects CIC instability and automatically re-initializes the CIC. The auto flush mode requires that the gain up to the output of the CIC filter is less than or equal to unity.

1. Hogenhauer, Eugene V., An Economical Class of Digital Filters for Decimation and Interpolation, IEEE transactions on Acoustics, Speech and Signal Processing, April 1981.
2. The auto flush mode is a patented feature of the chip. Use of the auto flush mode is highly recommended. CIC instability in cellular basestation chips without the auto flush feature can cause full power white noise to be transmitted on ALL frequencies, interfering with cell users in all nearby cells.

3.3.4 Wideband Input Mode

The overall interpolation factor of an up convert channel is 4N. The minimum value of N is 8, which limits the maximum input sample rate to be $F_{CK}/32$. If the clock rate is 100 MHz, then the maximum single channel input bandwidth is between 2 and 3 MHz. Wider input bandwidths can be handled by combining two channels into a single wideband channel using the SplitIQ mode (SPLITIQ in register 1). In the split IQ mode the complex input data is split between two channels. One channel up converts the I-half and the other channel up converts the Q-half. This allows the channels to process data at twice the rate so the minimum CIC interpolation is N=4 (rather than the previous N=8).

The input data is entered as two samples per CHREQ cycle. The I-half inputs are packed into complex words (I0 with I1, for example) and input into the first channel. The Q-half inputs are packed into complex words (Q0 with Q1, for example) and input into the second channel. The channel processing the imaginary data is programmed with a phase offset of 90 degrees from the channel processing the real channel (PHASE=0x4000).

In this mode, the chip can support two channels of 3.84 Mbaud UMTS signals.

NOTE: The resampler can not be used in the split IQ mode since it cannot provide data in the two samples per CHREQ format.

3.3.5 Complex Output Mode

The chip may be configured to generate complex rather than real output. In this case the output is the I word followed by the Q word at half the clock rate. The QFLG signal is used to identify the Q half of the output. Complex output applies to all channels on a chip. Likewise, if any chip in a sum path is using complex output, then all chips in the sum path must do so also. The CIC in the complex mode interpolates by N, but only outputs every other sample. This means that the effective CIC interpolation is N/2 in the complex output mode. Note, however, that the CIC gain will still be a function of N, not N/2.

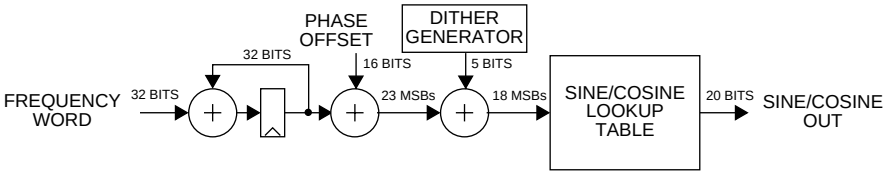


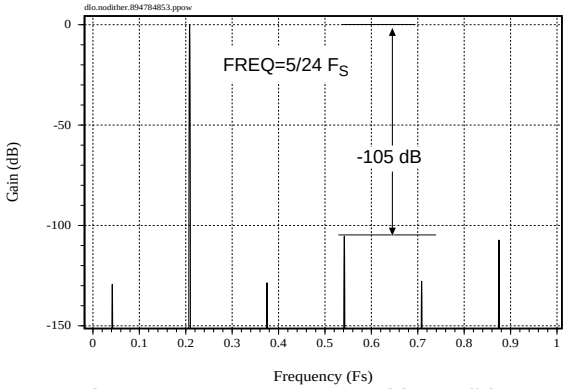
Figure 8. NCO Circuit

3.3.6 The Numerically Controlled Oscillator (NCO)

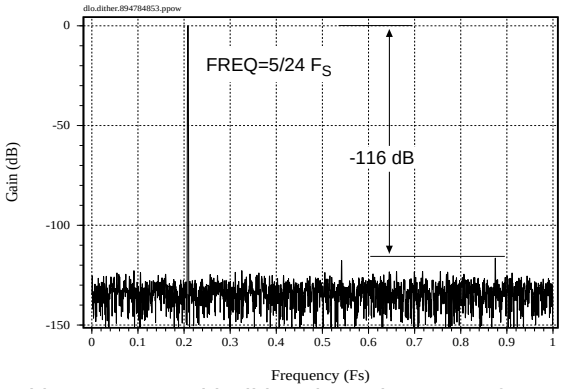
The tuning frequency of each down converter is specified as a 32 bit word and the phase offset is specified as a 16 bit word. The NCOs can be synchronized with NCOs on other chips. This allows multiple down converter outputs to be coherently combined, each with a unique phase and amplitude. A block diagram of the NCO circuit is shown in Figure 8.

The tuning frequency is set to FREQ according to the formula $FREQ = 2^{32}F/F_{CK}$, where F is the desired tuning frequency and F_{CK} is the chip's clock rate. The 16 bit phase offset setting is $PHASE = 2^{16}P/2\pi$, where P is the desired phase in radians ranging between 0 and 2π. Note that a positive tuning frequency should be used to upconvert the signal. A negative tuning frequency can be used to spectrally flip the spectrum of the desired signal. FREQ and PHASE are set in addresses 16 through 31 of the frequency and phase pages.

The NCO's frequency, phase and accumulator can be initialized and synchronized with other channels using the FREQ_SYNC, PHASE_SYNC, and NCO_SYNC controls in addresses 8 through 11. The FREQ_SYNC and PHASE_SYNC controls determine when new frequency and phase settings become active. Normally these are set to "always" so that they take effect immediately, but can be used to synchronize frequency hopping or beam forming systems. The NCO_SYNC control is usually set to never, but can be used to synchronize the LOs of multiple channels.

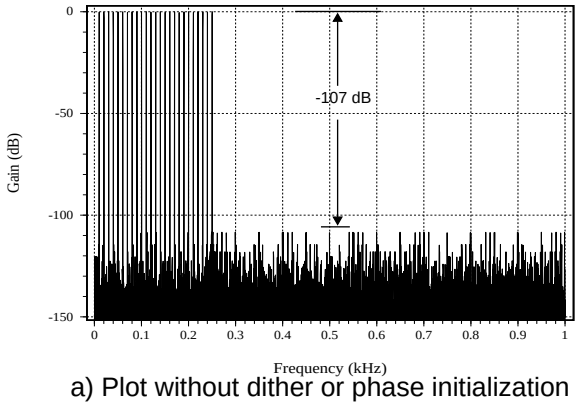


a) Worst case spectrum without dither

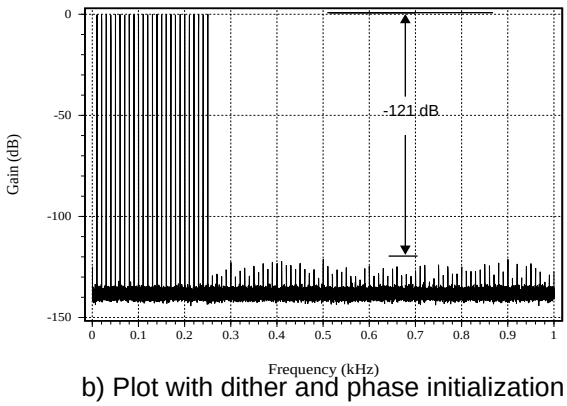


b) Spectrum with dither (tuned to same frequency)

Figure 9. Example NCO Spurs



a) Plot without dither or phase initialization



b) Plot with dither and phase initialization

Figure 10. NCO Peak Spur Plot

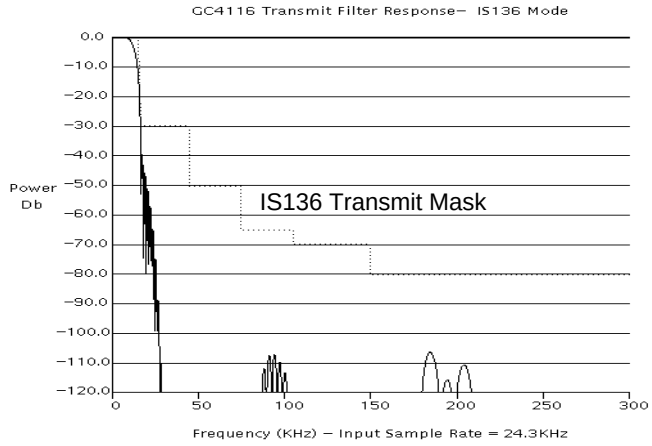
The NCO's spur level is reduced to below -113 dB through the use of phase dithering. The spectrums in Figure 9 show the NCO spurs for a worst case tuning frequency before and after dithering has been turned on. Notice that the spur level decreases from -105 dB to -116 dB. Dithering is turned on or off using the DITHER_SYNC controls in addresses 8 through 11.

The worst case NCO spurs at -113 to -116dB, such as the one shown in Figure 9(b), are due to a few frequencies that are related to the sampling frequency by multiples of $F_{CK}/96$ and $F_{CK}/124$. In these cases the rounding errors in the sine/cosine lookup table repeat in a regular fashion, thereby concentrating the error power into a single frequency, rather than spreading it across the spectrum. These worst case spurs can be eliminated by selecting an initial phase that minimizes the errors or by changing the tuning frequency by a small amount (50 Hz). Setting the initial phase to 4 for multiples of $F_{CK}/96$ or $F_{CK}/124$ (and to 0 for other frequencies) will result in spurs below -115 for all frequencies.

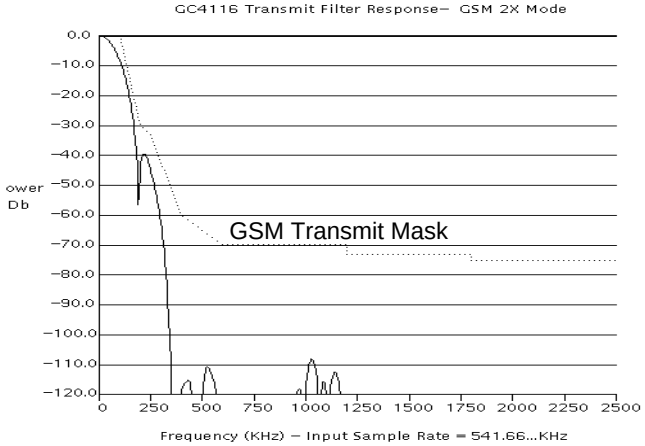
Figure 10 shows the maximum spur levels as the tuning frequency is scanned over a portion of the frequency range with the peak hold function of the spectrum analyzer turned on. Notice that the peak spur level is -107 dB before dithering and is -121 dB after dithering has been turned on and the phase initialization described above has been used.

3.4 THE OVERALL INTERPOLATION FILTER RESPONSE

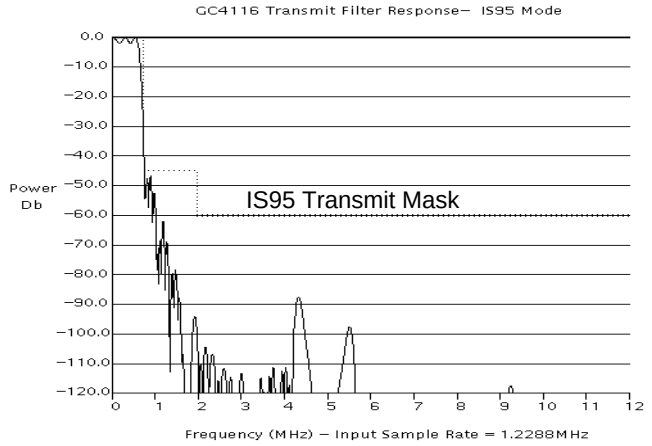
The image rejection of the up-convert channel is equal to the stop band rejection of the overall interpolation filter response. The overall response is obtained by convolving the interpolated responses of the PFIR and CFIR filters and CIC filter response. The overall response and appropriate transmit masks are shown in Figure 11 for four common standards. Figure 11a shows the overall response for IS136 (also referred to as DAMPS). Figure 11b shows the response for GSM (input at 2 samples per bit). Figures 11c & d shows the response for IS95 and 3.84 MB UMTS.



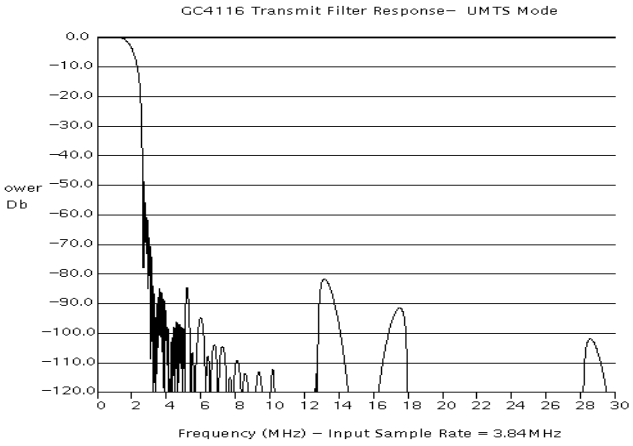
(a) IS136



(b) GSM



(c) IS95



(d) 3.84 MB UMTS

Figure 11. Overall Filter Response

3.5 THE SUM TREE

As shown in Figure 1, the mixer outputs are rounded to 20 bits and put into the LSBs of a 23 bit sum tree. The sum tree adds all four up-convert channels together. The 23 bit sum tree output is shifted down by four bits and rounded to 19 bits before being added into the LSBs of the external 22 bit sum input. The final 23 bit sum is either saturated to 22 bits (the MSB is checked for overflow) and output from the chip as 22 bits, or is scaled up by 0 to 7bits, rounded into the 8, 10, 12, 14, 16, 18, 20, or 22 MSBs and then output from the chip.

The sum tree gain is equal to $2^{SUM\_SCALE-7}$, where SUM_SCALE is 0 to 7 (See address 19 of the IO control page). Overflows in the sum tree are saturated to plus or minus full scale.

The latency from SUMI[0:21] to SUMO[0:21] is eight clock cycles.

3.6 OVERALL GAIN

The overall gain of the chip is a function of the input gain setting (G), the sum of the programmable filter coefficients (PFIR_SUM described in Section 3.3.1), the amount of interpolation in the CIC filters (N described in Section 3.3.3), the scale circuit settings in the CIC filter (SCALE and BIG_SHIFT described in Section 3.3.3), and the sum tree scale factor (SUM_SCALE described in Section 3.5). The overall gain, excluding any resampler gain, is:

$$\text{GAIN} = \left\{\frac{G}{128}\right\}\left\{\frac{PFIR\_SUM}{65536}\right\}\left\{N^4 2^{-(SCALE + 12 \times BIG\_SHIFT + 3)}\right\}\left\{2^{SUM\_SCALE-7}\right\}$$

where G and PFIR_SUM can be different for each channel, but N, SCALE, BIG_SHIFT, and SUM_SCALE are common to all channels. The resamplers gain, which precedes the input gain, is discussed in Section 3.7.6.

The optimal gain setting is one which will keep the amplitude of the data within the channel as high as possible without causing overflow. For random amplitude data the recommended gain target is to keep the root-mean-squared amplitude of the data close to one-fifth (0.2) full scale (a 14 dB crest factor). This level should be maintained throughout the channel computations. This means that the products

$$\left\{\frac{RMS}{32768}\right\}\left\{\frac{G}{128}\right\}\left\{\frac{PFIR\_SUM}{65536}\right\}$$

and

$$\left\{\frac{RMS}{32768}\right\}\left\{\frac{G}{128}\right\}\left\{\frac{PFIR\_SUM}{65536}\right\}\left\{N^4 2^{-(SCALE + 12 \times BIG\_SHIFT + 3)}\right\}$$

should both be less than or equal to 0.2, where “RMS” is the root-mean-squared level of the input data. Other crest factors can be used depending upon the application. For example, a crest factor of 12 dB is adequate if the final number of bits going to a DAC is 12 bits. In most cases the input data will already have the correct crest factor for the application, in which case the ratio $\left\{\frac{RMS}{32768}\right\}$ will be equal to the crest factor (e.g., 0.2) and the gain settings in the channel should be set to unity.

In some applications the input amplitude is far from random. For example, QPSK data has constant amplitude. In such cases the largest gain that guarantees no overflow can be calculated from the PFIR coefficients and normally allows a substantially higher gain than the optimal gain for random data of similar power.

Note that the resampler’s gain can be used to increase or decrease the RMS input level to the channels.

The sum tree adds the four channels within a single GC4116 together and then adds in sums from other chips using the sum I/O ports. The 22 bit sum I/O path guarantees that no overflow will occur for systems with 8 chips (32 channels) or less. The final chip in the chain should then shift and round the result to optimize the performance of the D/A. Since this represents the sum of many channels the gain should be set with a 14 dB crest factor.

The 14 dB crest factor assumes that the channels can be treated as uncorrelated signals which will result in a random, uniform amplitude distribution. If M signals are correlated, however, the amplitude gain can be M and the sum tree gain should be set to $\frac{1}{M}$. Examples of correlated signals are pure tones or modem signals that have been synchronized so that they might peak at the same time. These signals, however, require a much smaller crest factor, such as 3 dB for pure tones and 6 dB for modem signals. In this case the crest factor of 14 dB will absorb much of the difference in gain between $\sqrt{M}$ and M.

If overflow does occur, then the samples are saturated to plus or minus full scale. Overflow can be monitored using the status register (address 14).

The values of N and BIG_SHIFT must also satisfy $2^{(12*BIG\_SHIFT+18)} \geq N^4$ (see Section 3.3.3 for details). If N and BIG_SHIFT do not satisfy this relationship, then an overflow may occur which may not be detected.

If the auto flush mode is used, then the gain in the CIC must be less than or equal to unity. This means that the values of N, SCALE and BIG_SHIFT must satisfy $2^{(SCALE+12*BIG\_SHIFT+3)} \geq N^4$ (see Section 3.3.3 for details).

If attenuation is necessary, for example when multiple channel outputs are to be added together, then the attenuation should be added as close to the output of the chip as is possible - preferably only at the end of the sumtree just prior to going to the D/A.

3.7 FOUR CHANNEL RESAMPLER

The GC4116 contains a resampler which can be used to feed the up-converter channels in the chip, or can be used as a general resampling resource for a signal processing system. The resampler shares the clock to the chip, but its input, output and control circuitry are independent from the rest of the chip. The resampler in the GC4116 chip is very similar to the one in the GC4016 chip.

The resampler requires the use of the Serial Controller block described in Section 8.

Note that the resampler only works on complex data so the up converter's real or split IQ modes, which require two real samples per complex word, can not use the resampler. Also, the maximum output sample rate from the resampler is CK/44 when it is connected to the GC4116's upconvert channels. This means the upconvert channels must interpolate by at least a factor of 44 (N>=11) when using the resampler.

3.7.1 Resampler Input Format

The resampler inputs are complex samples, 16 bits per I or Q word. The samples are input to the resampler through bit-serial input ports, or through memory mapped registers. A resampler data request signal (RREQ) is output from the chip to identify when the resampler is ready for another complex input sample. The request (RREQ) signal may not be periodic, depending upon the resampling ratio being used.

The bit serial interface to the resampler functions the same as the serial interface to the channels (see Section 2) except the resampler does not support real input mode and the maximum input complex word rate is CK/34.

The Serial Controller is used to tell the resampler input buffer when the next set of serial samples is ready. The Serial Controller can also be used to generate the serial clock and frame strobes for the resampler's input ports (see Section 3.8).

3.7.2 Functional Description

The resampler consists of an input buffer, an interpolation filter, and an output buffer. A functional block diagram of the resampler is shown in Figure 12.

The resampler's sampling rate change is the ratio NDELAY/NDEC where NDELAY and NDEC are the interpolation and decimation factors shown in Figure 12. The decimation amount NDEC is a mixed integer/fractional number. When NDEC is an integer, then the exact sampling instance is computed and there is no phase jitter. If NDEC is fractional, then the desired sampling instance will not be one of the possible NDELAY interpolated values. Instead the nearest interpolated sample is used. This introduces a timing error (jitter) of no more than 1/(2*NDELAY) times the input sample period.

The input buffer accepts 16 bit data from the serial input ports or the memory mapped input registers. The input buffer serves both as a FIFO between the input and the resampler, and as a data delay line for the interpolation filter. The 64 complex word input buffer can be configured as four segments of 16 complex words each to support 4 resampler channels, or as two segments of 32 complex words each to support 2 resampler channels, or as a single segment of 64 complex words to support a single resampler channel. The number of segments is set by NCHAN in address 16 of the resampler control page.

The interpolation filter zero pads the input data by a factor of NDELAY and then filters the zero padded data using a QTAP length filter. The output of the QTAP filter is then decimated by a factor of NDEC.

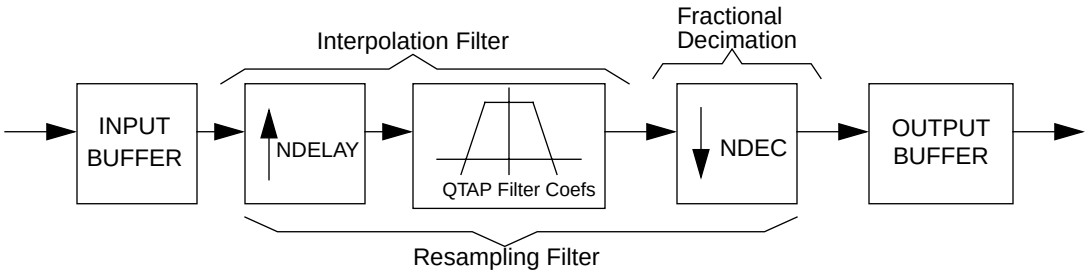


Figure 12. Resampler Channel Block Diagram

The resampling ratio for each channel is determined by setting the 32 bit RATIO control in addresses 16 through 31 of the resampler ratio page. The value of RATIO is defined as:

$$RATIO = 2^{26}\left(\frac{NDEC}{NDELAY}\right) = 2^{26}\left(\frac{INPUT\ SAMPLE\ RATE}{OUTPUT\ SAMPLE\ RATE}\right)$$

Up to four ratios can be stored within the chip. A ratio map register (address 23) selects which ratio is used by each channel.

The three spectral plots shown in Figure 13 illustrate the steps required to resample the channel data. The first spectral plot shows the data just after zero padding. The sample rate after zero padding is NDELAY*F_S, where F_S is the sample rate into the resampler. The second spectrum shows the shape of the QTAP filter which must be applied to the zero padded data in order to suppress the interpolation images. The last spectrum shows the final result after decimating by NDEC.

3.7.3 The Resampler Filter

Figure 13(b) illustrates the spectral shape requirements of the QTAP filter. If the desired signal bandwidth is B, then the filter's passband must be flat out to B/2 and the filter's stop band must start before F_S-B/2. The user designs this filter assuming a sample rate equal to NDELAY*F_S. Section 7.6 contains example resampler filters coefficient sets. Other passband and stopband responses can be used, such as root raised cosine receive filters, as desired. The resampler filter can also be used to augment the CIC, CFIR and PFIR filters' spectral response.

The number of filter coefficients, QTAP, is equal to NMULT*NDELAY, where NMULT is the number of multiplies available to compute each resampler output, and NDELAY is either 4, 8, 16, 32 or 64 as will be described later. The maximum filter length is 512. The user specifies NMULT in address 17 of the resampler control page.

The filter can be symmetric, or non-symmetric, as selected by the NO_SYM_RES control in address 17 of the resampler control page. The symmetric filter is of even length which means the center tap repeats.

The 12 bit filter coefficients are stored in a 256 word memory which can be divided into one, two, or four equal blocks. This allows the user to store one symmetric filter of up to 512 taps, two symmetric filters of up to 256 taps each, or four symmetric filters of up to 128 taps each. The number of filters is set by NFILTER in address 16 of the resampler control page. The filter used by each channel is selected

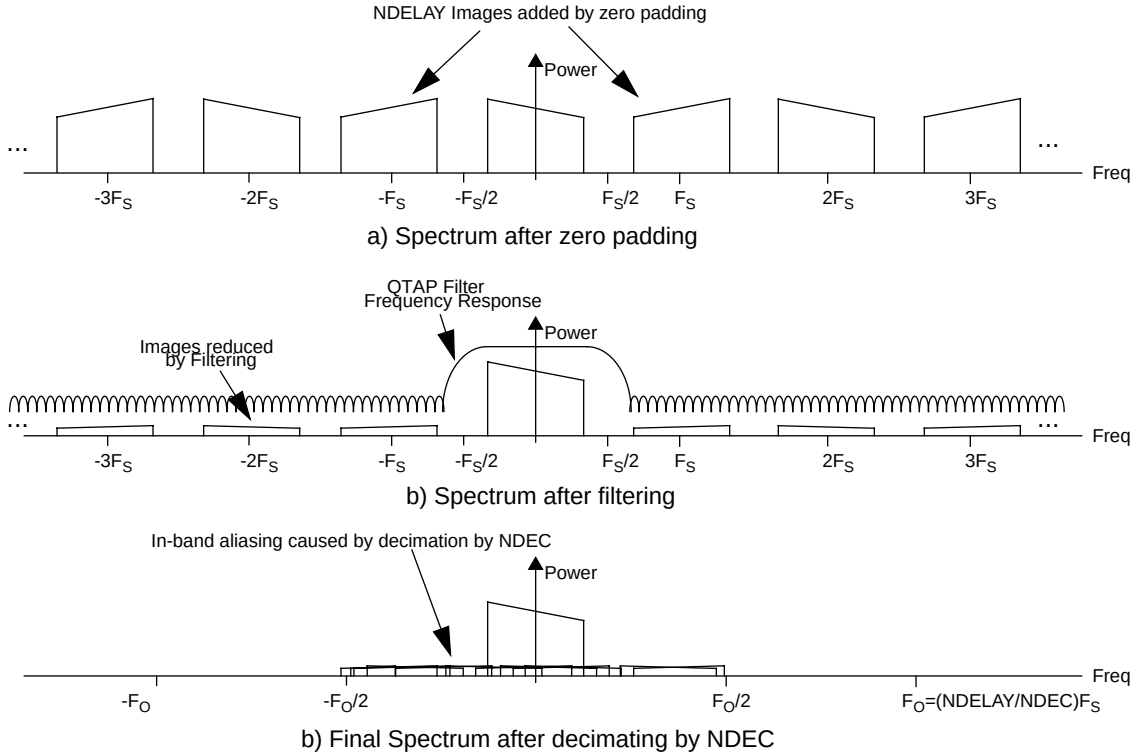


Figure 13. The Resampler's Spectral Response

using the FILTER_SEL controls in address 18 of the resampler control page. The filter lengths are cut in half if the filters are not symmetric. The coefficients are stored in memory with h_0 stored in the lowest address, where h_0 is the coefficient multiplied by the newest piece of data. The center tap of a symmetric filter is $h_{(QTAP/2)-1}$. The coefficients for multiple filters (NFILTER>1), are interleaved in the 256 word memory.

3.7.4 Restrictions on NMULT

The user does not directly set the value of NDELAY. The chip sets the value of NDELAY using NO_SYM_RES, NMULT and NFILTER according to:

$$NDELAY = Floor\_2\left[256\frac{(2-NO\_SYM\_RES)}{(NMULT)(NFILTER)}\right]$$

where the function FLOOR_2[X] means the power of two value that is equal to or less than "X". Since NMULT is restricted to be greater than or equal to 6 and less than or equal to 64, then NDELAY is either 4, 8, 16, 32 or 64. The length of the filter is then:

$$QTAP = (NDELAY)(NMULT)$$

The value of NMULT determines both the length of the filter and the number of delays in the resampling operation. In general one would choose the largest value of NMULT which gives an adequately large value of NDELAY. The choice of NMULT, however, must meet several restrictions. NMULT must be greater than a minimum, it cannot exceed the available number of multiplier cycles, and it must be less than the input delay line segment size. These restrictions are described below.

The minimum value of NMULT is determined by the minimum number of clock cycles required to update the resampler's state. This is a hardware restriction imposed by the chip's architecture. This limitation is:

$NMULT \geq 6$ if there are two or more channels

$NMULT \geq 7$ if there is only one channel (NCHAN=0)

The maximum value of NMULT must be less than, or equal to, twice the number of clock cycles available to calculate a resampler output. NMULT is the number of multiplier cycles used by the resampler to calculate each output. Since the resampler can perform two multiplies every clock cycle, the value of NMULT cannot exceed two times the number of clock cycles available to the resampler for each channel. The number of clock cycles available to the resampler is equal to the clock rate to the chip divided by the sum of the output sample rates for each resampler channel. Note that the resampler's output sample rate is usually much less than the clock rate, so that NMULT is rarely limited by this restriction.

The value of NMULT must also be less than the size of the delay line formed by the input buffer. The size of the delay line is either 16 for four resampler channels, 32 for two channels or 64 for a single channel as set by the NCHAN control in address 16 of the resampler control page. This limits NMULT to be less than or equal to 15, 31 or 63 dependent upon the number of resampler channels[1].

The typical resampler configuration will have four active channels, all using the same filter and the same resampling ratio. The typical configuration has NCHAN set to 4, NFILTER set to 1, NMULT set to 15 and NO_SYM_RES set to 0. This sets NDELAY to 32 and QTAPS to 480.

3.7.5 Resampler Shift and Round

The gain of each resampler output is adjusted by an up-shift by 0-15 bits (FINAL_SHIFT). This up-shift is applied just before rounding to 12, 16, 20 or 24 bits (ROUND). The values of FINAL_SHIFT and ROUND are set in control register 19 of the resampler control page. The resampler gain is:

$$RES\_GAIN = \left(\frac{RES\_SUM}{32768 \times NDELAY}\right)\left(2^{FINAL\_SHIFT}\right)$$

where RES_SUM is the sum of the QTAP coefficients.

3.7.6 By-Passing the Resampler

The resampler is bypassed by using a configuration which has h_0 set to 1024, all other taps set to zero, NMULT set to 7, NO_SYM_RES set to 1, FINAL_SHIFT set to 5, and RATIO set to 2^{26} (0x04000000). Note that the NDELAY term in the RES_GAIN equation shown above does not apply in this case and should be set to unity in the gain equation.

3.7.7 Resampler Output Buffer

The resampler output buffer stores resampler outputs until they are needed. The output is double buffered so that samples from each channel can be stored while previous samples are being output. Resampler output samples are held in the buffer until the RSTART signal is received. When RSTART is received, the buffered data is transferred to the serial output ports which begin to output the samples as

1. NOTE: If the resampler is being used at much less than its maximum capacity, i.e., NMULT is much less than twice the number of clock cycles available (See also RES_CLK_DIV), AND the channels are synchronous, then NMULT may equal the size of the delay line.

serial data streams. The RSTART pulse can only be one CK pulse wide.

The resampler serial output format is shown in Figure 14. The serial frame sync (ROFS) and serial data (ROUT)

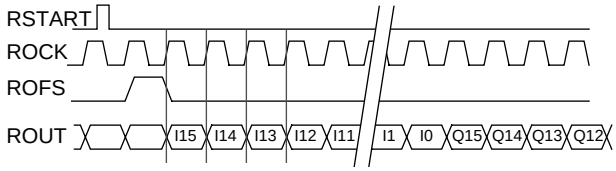


Figure 14. Resampler Serial Output

change on the rising edge of the serial clock (ROCK). The resampler serial outputs can be connected directly to the upconverter channel serial inputs if the polarity of the resampler serial clock is inverted by setting RES_CK_POL in address 18 of the resampler control page.

3.7.8 Resampler I/O Control

The Resampler will stop if the output buffer is full, or if the input buffer needs more samples. Typically the output rate is constant, such as when the resampler is feeding upconverter channels. The input rate is typically erratic, depending upon when the resampler needs more input data.

The resampler start control (RSTART) is used to start the serial outputs. The RSTART control transfers data from the output buffer into the serial output registers. The serial output frame will then start on the next rising edge of ROCK[1]. If the output buffer is full, then the resampler will stop until the next RSTART pulse has been received.

The resampler input data timing is controlled by the RREQ strobe and the Serial Controller described in the next Section. The RREQ strobe is output when the resampler needs more input data. The RREQ strobe should be connected to the SCSTART input of the Serial Controller. The Serial Controller is then programmed to tell the resampler that the serial transfer is done and new input data is ready. The frame length programmed into the Serial Controller tells the resampler that the new data samples are ready SC_FRAME_CNT+18 serial clocks after RREQ. SC_FRAME_CNT is set in address 21 of the IO control page. Note that the serial controller can be used to slow down the RREQ rate by setting the minimum period between RREQ strobes to be SC_FRAME_CNT+18 serial clocks.

1. Actually, the serial frame starts on the next rising edge of ROCK which is 2 CK pulses after RSTART.

3.8 SERIAL CONTROLLER

The Serial Controller block can be used to generate the necessary serial clock and frame strobes for the channel or resampler input ports. This frees the input data source (ASIC, FPGA or DSP chip) from having to generate these signals. In the case of a DSP chip, this may allow the input samples to be transferred in a background “DMA” mode that doesn’t interrupt the DSP before or after each serial transfer.

The Serial controller generates a serial clock and four serial frame strobes, one for each input serial port. Each frame strobe can be programmed to be delayed by a different amount from the Serial Controller start (SCSTART) pulse.

The serial controller contains a serial clock generator and a frame counter. The serial clock (SCCK) is generated by dividing down CK by 1 to 16 (see SC_CK_DIV in address 20 of the IO control page). The serial clocks in multiple chips can be synchronized by using the SIA or SIB sync inputs, as selected by the SCCK_SYNC control bits in address 20 of the IO control page. Two copies of the serial clock are output on pins SCCK0 and SCCK1. Two copies are output to increase the fanout of the clock.

The start signal (SCSTART) is clocked into the chip on the rising edge of CK. SCSTART is expected to be one CK clock cycle wide. Typically SCSTART is either connected to CHREQ or RREQ, depending upon whether the it is being used for the up convert channels or the resampler.

The 8 bit frame counter is started by SCSTART at the value SC_FRAME_CNT. The counter is decremented at the serial clock rate until it reaches zero. The counter will continue to decrement for 18 more serial clocks if it is being used with the resampler (SC_MODE=0 in address 17 of the IO Control page), at which time it will tell the resampler that the serial frame is done and a new resampler computation can begin. The counter will count down 2 more serial clocks and stop if the serial controller is being used with the channels (SC_MODE=1).

The serial frame strobes SCFSA, SCFSB, SCFSC and SCFSD are generated by comparing the upper four bits of the frame counter to SC_FS_DELAY_A, SC_FS_DELAY_B, SC_FS_DELAY_C and SC_FS_DELAY_D. A frame strobe is output when the delay values match the counter and the lower four bits of the counter are zero. This allows the frame strobes to be generated on 16 serial clock boundaries.

NOTE: If the 4 LSBs of SC_FRAME_CNT are zero, and one of the SC_FS_DELAY values match the upper 4 bits of SC_FRAME_CNT, then that frame strobe will be active when the serial controller is idle and waiting for another SCSTART

pulse. In general, the lower 4 bits of SC_FRAME_CNT should be non-zero.

The serial control supports both the packed and unpacked serial modes, where the unpacked mode expects a serial frame strobe for each 16 bit word of a complex pair, and the packed mode expects a single frame strobe for the 32 bit complex pair.

The frame strobe in the packed mode (PACKED=1 and SC_MODE=1, or RES_PACKED=1 and SC_MODE=0, in addresses 16 and 17 of the IO Control page) may be positioned in one of 15 delays, corresponding to SC_FS_DELAY values of 0 through 14. In the unpacked mode only the upper three bits of the counter are compared with the upper 3 bits of the SC_FS_DELAY values. The lower bit of the SC_FS_DELAY values must be zero. This means that the values will match twice, outputting two frame strobes, 16 bits apart.

If the input data is coming from four serial streams, so that the four frame strobes should be sent at the same time, then SCFRAME_CNT should be set to 17, and the four SC_FS_DELAY values should be set to “1”. Larger values of SC_FRAME_CNT can be used in this case in order to spread out the RREQ periods.

If the data is coming from a single TDM bus, then SCFSA (or SCSTART) can be sent to the data source to start the TDM frame, and then SCFSB, SCFSC and SCFSD can be delayed to identify the appropriate time slots in the TDM bus.

When the serial controller is being used with the channel inputs (not the resampler) and the upconvert interpolation factor is 32 or 36, then the frame delays must be used to delay the serial frames to start between 2 to 7 clocks before the next CHREQ strobe. This is because of the requirement that the serial transfer of 32 bit is completed 2 to 7 clocks before the next CHREQ strobe (See Section 3.2.1). This means that for an interpolation of 32 (the CIC interpolation factor N is 8), SC_FRAME_CNT should be set to 39 and the SC_FS_DELAY values should be “1”. For an interpolation of 36 (N=9) SC_FRAME_CNT should be 43. For larger interpolation factors the default value of 17 can be used. NOTE that if the serial clock is divided, then similar delay values may need to be used in order to insure that the serial frame is complete before the next CHREQ.

3.9 CLOCKING

The chip clock rate is equal to the output data rate which can be up to 100 MHz. An internal clock doubler doubles the clock rate so that the internal circuitry is clocked at twice the data rate. The clock doubler requires 4-5 clocks to adapt to the rate of the incoming clock during which time the reset should be active. A gated clock, not uniform clock period clock, is not suitable for this device above 40 MHz. A test mode (ext_2xck) allows the use of an external double rate clock (ck2x pin). This is intended for use in production test. Please contact Graychip if further information on this mode is needed.

3.10 POWER DOWN MODES

The chip has a power down and clock loss detect circuit. This circuit detects if the clock is absent long enough to cause dynamic storage nodes to lose state. If clock loss is detected, an internal reset state is entered to force the dynamic nodes to become static. The control registers are not reset and will retain their values, but any data values within the chip will be lost. When the clock returns to normal the chip will automatically return to normal. In the reset state the chip consumes only a small amount of standby power. The user can select whether this circuit is in the automatic clock-loss detect mode, is always on (power down mode), or is disabled (the clock reset never kicks in) using the DISABLE_CK_LOSS control bit in address 13 and the GLOBAL_RESET control bit in address 5. The whole chip, or individual down converter channels can be powered down. Individual channels are powered down using the RESET_A, B, C and D control bits in address 5.

3.11 SYNCHRONIZATION

Each GC4116 chip can be synchronized through the use of one of two sync input signals, an internal one shot sync generator, or a sync counter. The sync to each circuit can also be set to be always on or always off. Each circuit within the chip, such as the sine/cosine generators or the interpolation control counter can be synchronized to one of these sources. These syncs can also be output from the chip so that multiple chips can be synchronized to the syncs coming from a designated “master” GC4116 chip.

The 2 bit sync mode control for each sync circuit is defined in Table 1:

Table 1: Sync Modes

MODE	SYNC SOURCE
0	off (never asserted)
1	SIA or SIB (See Table 2)
2	TC (terminal count of the sync counter) or ONE_SHOT (if USE_ONESHOT in address 0 is set)
3	on (always active)

NOTE: the internal syncs are active high. The $\overline{SIA}$ and $\overline{SIB}$ inputs have been inverted to be the active high syncs SIA and SIB in Table1.

The ONE_SHOT sync (address 0, bit 7) can either be a level or a pulse as selected by the OS_MODE control bit in address 13. The level mode is used to initialize the chip, the pulse mode is used to synchronously switch frequency, phase or gain values.

The SIA and SIB external sync inputs are provided to allow independent synchronization of different features of the GC4116 chip. Sync mode 1 is either SIA or SIB, depending upon what circuit is being synchronized by the sync circuit. Table 2 lists all of the sync circuits, what they do, which sync mode 1 it uses, and the suggested default mode settings.

The SIA sync is intended to be used during initialization only. The circuits connected to SIA are ones that should be initialized once, and then let free run. SIB is intended to be used for those circuits which may be periodically initialized, such as changing frequency, phase and gain between TDMA bursts.

The interpolation control counter generates the request strobe (CHREQ) output from the chip. This counter can be syncronized using the input $\overline{SIA}$ sync (INT_SYNC=1). This allows the user to lock the timing of the request strobe to the $\overline{SIA}$ timing. If this is done, and BIG_SHIFT is even, then the CHREQ strobe will go high 8 clock cycles after the $\overline{SIA}$ strobe. For example, if the $\overline{SIA}$ signal is active during clock cycle 0, then CHREQ will go high during clock cycle 8 and then repeat every 4N clocks (or 2N clocks in the real input mode) thereafter. If BIG_SHIFT is odd then the delay is 7 clock cycles.

Table 2: Sync Descriptions

Sync Circuit	Mode 1	Description	Default
INT_SYNC	SIA	Interpolation control counter. Sets timing of CHREQ.	1(SIA)
COUNTER_ SYNC	SIA	Internal sync counter. Generates TC sync. Mode 2 is always ONE_SHOT	2 (OS)
OUTPUT_ SYNC	SIA	The output sync (SO) selection.	2 (TC)
GAIN_SYNC	SIB	A single bit sync selection. GAIN_SYNC=0 means the gain is applied immediately. GAIN_SYNC=1 means the gain is applied after SIB.	0
DIAG_SYNC	SIA	Selects when to start the diagnostic ramp and to store the diagnostic checksum.	2 (TC)
FREQ_SYNC	SIB	Selects when new frequency settings take effect.	3 (on)
PHASE_SYNC	SIB	Selects when new phase settings take effect.	3 (on)
NCO_SYNC	SIB	Reset the NCO phase accumulator	0 (off)
DITHER_ SYNC	SIB	Clears the NCO dither circuit.	0 (off)
FLUSH _ (A,B,C,D)	SIA	Starts a flush of the channel	1 (SIA)
ROCK_SYNC	SIA	Syncs the resampler's serial output clock. Mode 2 is SIB.	1 (SIA)
SCCK_SYNC	SIA	Syncs the serial controller's serial output clock. Mode 2 is SIB.	1 (SIA)
RES_SYNC	Note 1	Syncs the resampler during initialization	2 (SIA)
RATIO_SYNC	Note 1	Selects when a new resampler ratio takes effect.	3 (SIB)

Note 1: These use a 3 bit sync mode selection where modes 0,1 and 5 are "off", mode 2 is SIA, mode 3 is SIB, mode 4 is ONE_SHOT, and modes 6 and 7 are "on".

3.12 INITIALIZATION

Two initialization procedures are recommended. The first is recommended for multi-GC4116 chip configuration. The second can be used for stand alone GC4116 chips.

3.12.1 Initializing Multiple GC4116 Chips

The multi-GC4116 initialization procedure assumes that the $\overline{SIA}$ sync input pins of all GC4116 chips are tied together and are connected to the $\overline{SO}$ output of the "master" chip, or to a common sync source. The procedure is to:

(1) reset the chip by setting address 5, the reset register, to 0xFF;

(2) configure the rest of the chip including setting the INT_SYNC, RES_SYNC and FLUSH_(A,B,C,D) to be $\overline{SIA}$, the OS_MODE to be 1, and the OUTPUT_SYNC to be OS (see Table 1);

(3) assert the $\overline{SIA}$ sync input by setting the ONE_SHOT control bit high (or by setting the external $\overline{SIA}$ source low);

(4) release the global resets by setting address 5 to 0x00; and

(5) release the $\overline{SIA}$ sync by setting ONE_SHOT to 0 (or the external $\overline{SIA}$ source high).

The global resets are asserted before configuring the chip so that the operation of all of the pins, including the directions of the bidirectional and tristate pins, will be established before the global resets release them. The $\overline{SIA}$ sync is asserted before releasing the global resets so that the channels will remain in a reset state after the global resets are released. All channels and the resampler will then start synchronously by releasing the SIA sync. If there are multiple chips which need synchronized, then synchronously releasing the SIA sync to them all will force them all to be synchronized.

The frequency, phase and gain of multiple chips can be initialized by holding $\overline{SIB}$ low and then releasing it to all of the chips at the same time.

3.12.2 Initializing Stand Alone GC4116 chips

The initialization sequence for a stand alone GC4116 chip is similar to the one for the multi-GC4116 procedure, except that the ONE_SHOT is used to synchronize the chip, not the $\overline{SIA}$ input sync. The procedure is to:

(1) reset the chip by setting address 5, the reset register, to 0xFF;

(2) configure the rest of the chip including setting the INT_SYNC, RES_SYNC and FLUSH_(A,B,C,D) to be ONE_SHOT (mode 2) and the OS_MODE to be 1;

(3) assert the syncs by setting ONE_SHOT high;

(4) release the global resets by setting address 5 to 0x00; and

(5) release the syncs by setting ONE_SHOT to 0.

3.13 DATA LATENCY

The data latency through the chip is defined as the delay from the rising edge of a step function input to the chip to the rising edge of the step function as it leaves the chip. This delay is dominated by the number of taps in each of the filters. An estimate of the overall latency through the chip, expressed as the number of CK clock cycles is:

(CIC latency = 2.5N) + (CFIR latency = 16N) +
(PFIR latency = N*PTAP) + (Resampler latency) + (Input delay) + (Pipeline delay)

where N is the CIC interpolation ratio and PTAP is the number of PFIR taps. PTAP is normally 63. Latency can be reduced by using the NO_SYM_PFIR mode to shorten the filter.

The Resampler latency, if the resampler is being used, is approximately 2N*NMULT plus a resampler input sample period and a resampler output period to allow for resampler I/O buffering. The latency in the resampler can be minimized by using the bypass configuration (See Section 3.7.7).

The Input delay is approximately two input sample periods due to the double buffering in the serial input ports. The Pipeline delay is approximately 40 clock cycles.

3.14 DIAGNOSTICS

The chip has an internal ramp generator which can be used in place of the data inputs for diagnostics. An internal checksum circuit generates a checksum of the output data to verify the chip's operation. See Section 7.12 for diagnostic configurations and checksums.

Besides the internal diagnostics, the chip supports initial board debug through special input and output tests. The suggested procedure for bringing up the GC4116 chip on a board is to first check the control interface by writing to the control registers and reading them back. The diagnostics described in Section 7.12 should be run next, followed by the output and input tests described in Sections 7.13 and 7.14. If these pass successfully, then the configuration customized for the desired application should work.

3.15 JTAG

The GC4116 supports a four pin (TDI, TDO, TCK and TMS) boundary scan interface. Contact GRAYCHIP to receive the GC4116's BSDL file.

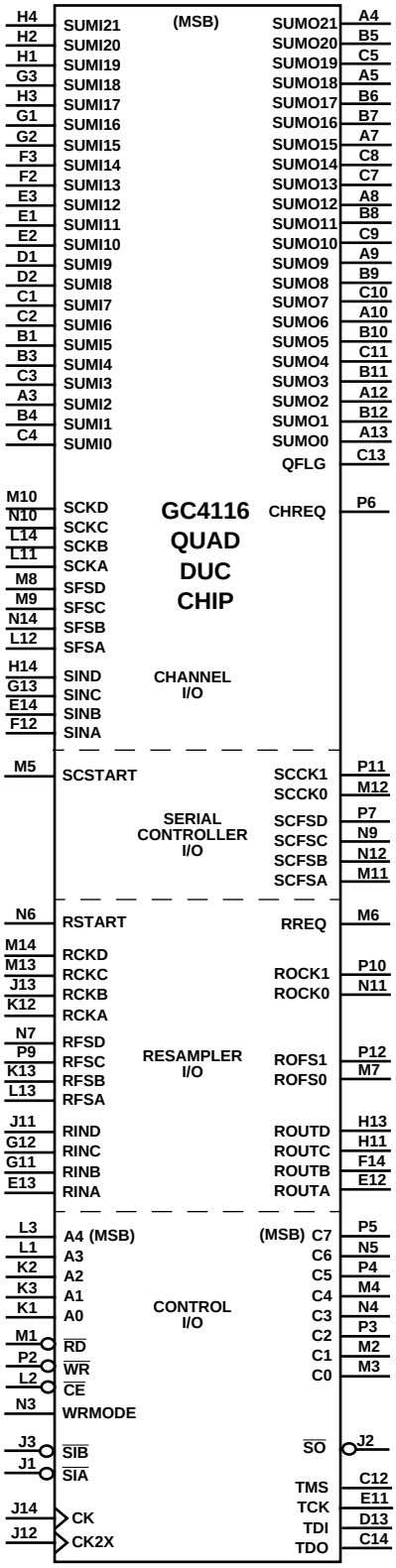
3.16 MASK REVISION REGISTER

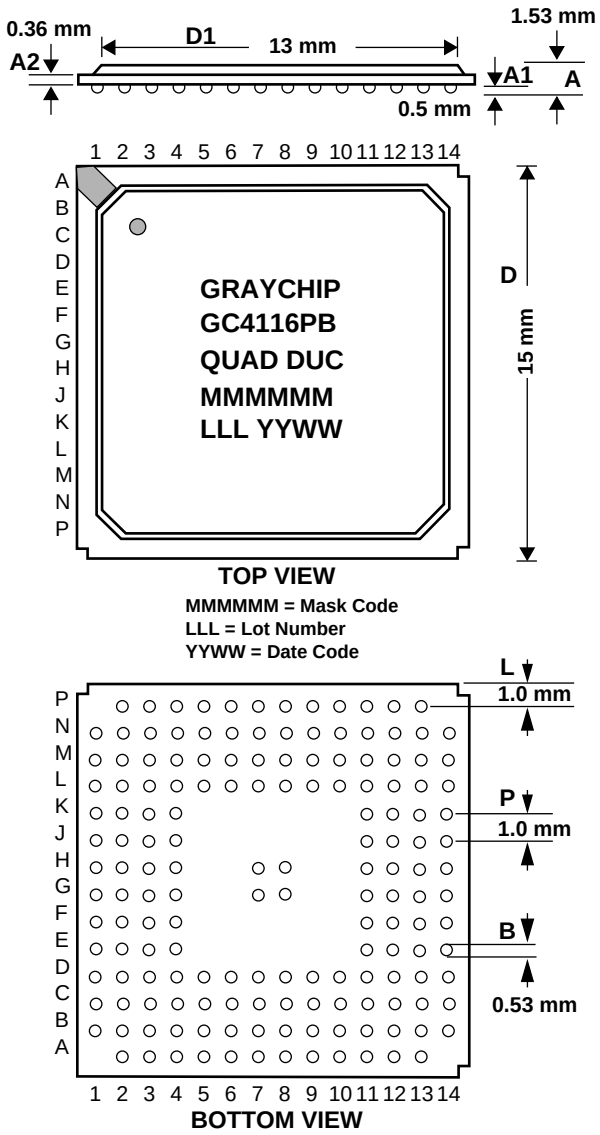
An 8 bit mask revision code (REVISION) can be read from address 31 of page 0. The revision code allows users to determine, through software, what version of the GC4116 chips are being used. The current mask revision codes are:

Table 3: Mask Revisions

GC4016			
Revision Code (REVISION)	Release Date	Mask Code on Package	Description
0	April 2000	SAMPLE	Early samples
1	Nov. 2000	1002ACB	First Release, Revision 1
2	March 2001	1002BCB	Revision 2, adds JTAG, corrects initialization bug

4.0 PACKAGING





DIMENSION	TYP	TOLERANCE
D (width body)	15 mm	mm
D1 (width cover)	13 mm	mm
P (ball pitch)	1.0 mm	mm
B (ball width)	0.53 mm	mm
L (overhang)	1.0 mm	mm
A (overall height)	1.53 mm	mm
A1 (ball height)	0.5 mm	mm
A2 (substrate thickness)	0.36 mm	mm

THERMAL GND BALLS: G7, G8, H7, H8

GND BALLS: A6, D3, D12, E4, F4, F11, G14, K4, K11, N8
B2, B13, C6, D5, D9, D11, L5, L7, L8, L10, N2, N13

VCORE BALLS: D4, D7, D14, F1, F13, G4, H12, J4, K14, P8

VPAD BALLS: A2, A11, B14, D6, D8, D10, L4, L6, L9, N1, P13

NOTE: 0.01 to 0.1 µf DECOUPLING CAPACITORS SHOULD BE PLACED AS CLOSE AS POSSIBLE TO EACH SIDE OF THE CHIP

Figure 15. 160 Pin Plastic Ball Grid Array (PBGA) Package

Table 4: GC4116 Pin Out Locations Top View

	1:	2:	3:	4:	5:	6:	7:	8:	9:	10:	11:	12:	13:	14:
A:		VPAD	SUMI2	SUMO21	SUMO18	GND	SUMO15	SUMO12	SUMO9	SUMO6	VPAD	SUMO2	SUMO0	
B:	SUMI5	GND	SUMI4	SUMI1	SUMO20	SUMO17	SUMO16	SUMO11	SUMO8	SUMO5	SUMO3	SUMO1	GND	VPAD
C:	SUMI7	SUMI6	SUMI3	SUMI0	SUMO19	GND	SUMO13	SUMO14	SUMO10	SUMO7	SUMO4	TMS	QFLG	TDO
D:	SUMI9	SUMI8	GND	VCORE	GND	VPAD	VCORE	VPAD	GND	VPAD	GND	GND	TDI	VCORE
E:	SUMI11	SUMI10	SUMI12	GND							TCK	ROUTA	RINA	SINB
F:	VCORE	SUMI13	SUMI14	GND							GND	SINA	VCORE	ROUTB
G:	SUMI16	SUMI15	SUMI18	VCORE			TGND	TGND			RINB	RINC	SINC	GND
H:	SUMI19	SUMI20	SUMI17	SUMI21			TGND	TGND			ROUTC	VCORE	ROUTD	SIND
J:	$\overline{SIA}$	$\overline{SO}$	$\overline{SIB}$	VCORE							RIND	CK2X	RCKB	CK
K:	A0	A2	A1	GND							GND	RCKA	RFSB	VCORE
L:	A3	$\overline{CE}$	A4	VPAD	GND	VPAD	GND	GND	VPAD	GND	SCKA	SFSA	RFSA	SCKB
M:	$\overline{RD}$	C1	C0	C4	SCSTART	RREQ	ROFS0	SFSD	SFSC	SCKD	SCFSA	SCCK0	RCKC	RCKD
N:	VPAD	GND	WRMODE	C3	C6	RSTART	RFSD	GND	SCFSC	SCKC	ROCK0	SCFSB	GND	SFSB
P:		$\overline{WR}$	C2	C5	C7	CHREQ	SCFSD	VCORE	RFSC	ROCK1	SCCK1	ROFS1	VPAD	

VPAD = Pad ring power
VCORE = Core power
TGND = Thermal ground

SIGNAL	DESCRIPTION
CK	**INPUT CLOCK.** *Active high input* The clock input to the chip. The **SUMI, RSTART, SCSTART, $\overline{\text{SIA}}$** and **$\overline{\text{SIB}}$** input signals are clocked into the chip on the rising edge of this clock. The SUMO, CHREQ, RREQ, ROUT, ROCK, ROFS, SCCK, SCFS and $\overline{\text{SO}}$ outputs are clocked out by the rising edge of CK.
CK2X	**DOUBLE RATE INPUT CLOCK.** *Active high input* The chip uses an internally doubled clock for normal processing. For test purposes the double rate clock can be supplied externally using this pin. Should be grounded for normal use.
$\overline{\text{SIA}}$, $\overline{\text{SIB}}$	**SYNC IN**. *Active low input* The sync inputs to the chip. These syncs are clocked into the chip on the rising edge of the input clock (**CK**). All timers, accumulators, and control counters are, or can be, synchronized to one of **$\overline{\text{SIA}}$** or **$\overline{\text{SIB}}$**.
$\overline{\text{SO}}$	**SYNC OUT**. *Active low output* This signal is either a delayed version of the input sync **$\overline{\text{SIA}}$**, the sync counter's terminal count (TC), or a one-shot strobe. The **$\overline{\text{SO}}$** signal is clocked out of the chip on the rising edge of the input clock (**CK**).
CHREQ	**CHANNEL DATA REQUEST**, *programmable active high or low output* The chip requests new input data for the channels by asserting this signal. CHREQ is clocked out of the chip on the rising edge of CK and is one CK cycle wide. The polarity of this signal is user programmable. This signal is typically connected to the RSTART input of the resampler, or the SCSTART input of the serial controller. It can also be used as a start pulse to dedicated circuitry or an interrupt to a DSP chip.
SIN A,B,C,D	**BIT SERIAL INPUT DATA,** *Active high input* The bit serial input data for the four channels. The I and Q halves of complex data are entered on the same pin. Each time the chip asserts **CHREQ** (See above) the I-half is entered and then the Q-half.
SCK A,B,C,D	**BIT SERIAL DATA CLOCK**, *Active high or low input* The serial data bits are clocked into the chip by these clocks. The active edge of these clocks are user programmable.
SFS A,B,C,D	**BIT SERIAL FRAME STROBE**, *Active high or low input* The bit serial word strobe. This strobe delineates the 16 bit words, or 32 bit complex pair, within the bit serial input stream. This strobe can be a pulse at the beginning of each bit serial word, or can act as a window enable which is active while the data bits are active.

SIGNAL	DESCRIPTION
RREQ	**RESAMPLER REQUEST**, *programmable active high or low output* The chip requests new input data for the resampler by asserting this signal. RREQ is clocked out of the chip on the rising edge of CK and is one CK cycle wide. The polarity of this signal is user programmable. This signal must be connected to the SCSTART input of the serial controller if the resampler is being used. It can also be used as an interrupt to a DSP chip, or as a start pulse to dedicated circuitry.
RSTART	**RESAMPLER START**, *active high input* This input requests the resampler to send data. Typically connected to CHREQ. RSTART is clocked into the chip on the rising edge of CK and can only be high for one CK cycle.
RIN A,B,C,D	**RESAMPLER INPUT BIT SERIAL DATA,** *Active high input* The bit serial input data for the resampler input. The I and Q halves of complex data are entered on the same pin, MSB to LSB, I-half followed by Q-half.
RCK A,B,C,D	**RESAMPLER INPUT SERIAL CLOCK**, *Active high or low input* The resampler serial data bits are clocked into the chip by these clocks. The active edge of these clocks are user programmable.
RFS A,B,C,D	**RESAMPLER INPUT FRAME STROBE**, *Active high or low input* The resampler bit serial frame strobe. This strobe delineates the 32 bit complex words within the bit serial input stream. This strobe can be a pulse at the beginning of each bit serial word, or can act as a window enable which is active while the data bits are active.
ROUT A,B,C,D	**RESAMPLER OUTPUT BIT SERIAL DATA,** *Active high output* The bit serial output data from the resampler. The I and Q halves of complex data are transmitted on the same pin, I followed by Q, 16 bits each, MSB first.
ROCK 0,1	**RESAMPLER OUTPUT SERIAL CLOCKS**, *programmable active high or low output* These outputs provide two copies of a programmable serial clock. Normally used to drive the serial clock inputs to the channels (SCK-A,B,C,D).
ROFS 0,1	**RESAMPLER OUTPUT FRAME STROBES**, *programmable active high or low output* The resampler outputs a single frame strobe common to all outputs. Two copies of this signal are provided for fan out. They are normally connected to the channels (SFS-A,B,C,D).

SIGNAL	DESCRIPTION
SCSTART	**SERIAL CONTROLLER START**, *active high input* The start pulse for the serial controller. Normally connected to CHREQ or RREQ. Can only be high for one CK cycle at a time.
SCCK 0,1	**SERIAL CONTROLLER OUTPUT CLOCKS**, *active high or low outputs* These outputs provide two copies of a programmable serial clock. Normally used to drive both the serial clock port of a DSP, FPGA or ASIC chip and the serial clock inputs of either the resampler block (RSCK-A,B,C,D) or the channels (SCK-A,B,C,D).
SCFS A,B,C,D	**SERIAL CONTROLLER OUTPUT FRAME STROBES**, *active high or low outputs* The frame strobe outputs of the serial controller. They are normally connected either to the resampler input frame strobes (RSFS-A,B,C,D) or the channel input frame strobes (SFS-A,B,C,D) as well as to a DSP, FPGA or ASIC chip's serial frame strobe input.
SUMI[0:21]	**SUM IO INPUT DATA.** *Active high inputs* The 22 bit two's complement sum tree input samples. New samples are clocked into the chip on the rising edge of CK. The input data rate is assumed to be equal to the clock rate.
SUMO[0:21]	**SUM IO OUTPUT DATA**. *Active high outputs* The 22 bit sum tree output data. The bits are clocked out on the rising edge of the clock (**CK**). Programmable two's complement or offset binary.
QFLG	**Q FLAG**. *Active high output* This output is high to identify the imaginary half of a complex sample. This is useful in complex output mode where I and Q are multiplexed onto the sum IO pins. QFLG is clocked out on the rising edge of CK.
TMS,TCK,TDI,TDO	**JTAG INTERFACE.** ***Active high input (****TCK, TMS, TDI****) and active high tristate output (****TDO****) pins*** The JTAG interface, see Section 3.15.

SIGNAL	DESCRIPTION
C[0:7]	**CONTROL DATA I/O BUS**. *Active high bidirectional* This is the 8 bit control data I/O bus. Control register data is loaded into the chip or read from the chip through these pins. The chip will only drive these pins when **$\overline{\text{CE}}$** is low and **$\overline{\text{RD}}$** is low and **$\overline{\text{WR}}$** is high.
A[0:4]	**CONTROL ADDRESS BUS**. *Active high input* These pins are used to address the control registers within the chip. Each of the control registers within the chip are assigned a unique address. A control register can be written to or read from by having the page register set to the appropriate page and then setting **A[0:4]** to the register's address.
$\overline{\text{RD}}$	**READ ENABLE**. *Active low input* This pin enables the chip to output the contents of the selected register on the **C[0:7]** pins when **$\overline{\text{CE}}$** is also low.
$\overline{\text{WR}}$	**WRITE ENABLE**. *Active low input* This pin enables the chip to write the value on the **C[0:7]** pins into the selected register when **$\overline{\text{CE}}$** is also low.
$\overline{\text{CE}}$	**CHIP ENABLE**. *Active low input* This control strobe enables the read or write operation. The contents of the register selected by **A[0:5]** will be output on **C[0:7]** when **$\overline{\text{RD}}$** is low and **$\overline{\text{CE}}$** is low. If **$\overline{\text{WR}}$** is low and **$\overline{\text{CE}}$** is low, then the selected register will be loaded with the contents of **C[0:7].**
WRMODE	**WRITE MODE**. *Active high input* This pin changes the write timing on the control port so that the data need only be stable relative to the rising edge of either **$\overline{\text{WR}}$** or **$\overline{\text{CE}}$**.
VCORE	**CORE SUPPLY VOLTAGE**. These pins are used to supply the core logic. Nominally set at 2.5V.
VPAD	**INTERFACE VOLTAGE**. These pins are used to set the voltage I/O levels for all pins. Nominally set at 3.3V. Still functional at lower supplies but at reduced speed.
GND	**GROUND.**
TGND	**THERMAL GROUND** These pins are used to extract heat from the die and should be connected to the ground plane.

5.0 CONTROL REGISTERS

The chip is configured and controlled through the use of eight bit control registers. These registers are accessed for reading or writing using the control bus pins (**$\overline{CE}$**, **$\overline{RD}$**, **$\overline{WR}$**, **A[0:4]**, and **C[0:7]**) described in the previous section. The registers are divided into 16 global registers and 16 paged registers. Addresses 0-15 are reserved for global registers. Addresses 16-31 are used for paged registers. Address 15 is the page register which selects which control registers are accessed by addresses 16 through 31.

5.1 GLOBAL REGISTERS

The 16 global control registers are:

Table 5: GLOBAL CONTROL REGISTERS

ADDRESS	NAME	DESCRIPTION
0	Sync Mode	Syncs for interpolation, counter, and output. Also ONE_SHOT control.
1	Interpolation Mode	Real in, SplitIQ, gain sync, no symmetry, and diagnostic.
2	Interpolation Gain	Set CIC gain.
3	Interpolation Byte 0	CIC interpolation count least significant byte.
4	Interpolation Byte 1	CIC interpolation count most significant bye.
5	Reset	Resets for the four channels, resampler, outputs, and global reset.
6	Counter Byte 0	Sync counter least significant byte.
7	Counter Byte 1	Sync counter most significant byte.
8	Chan A sync	Syncs for channel A's frequency, phase, NCO, and dither.
9	Chan B sync	Syncs for channel B's frequency, phase, NCO, and dither.
10	Chan C sync	Syncs for channel C's frequency, phase, NCO, and dither.
11	Chan D sync	Syncs for channel D's frequency, phase, NCO, and dither.
12	Flush	Flush controls for all four channels.
13	Miscellaneous	Complex out, msb invert, and various test control bits.
14	Status	Status feedback from chip including: ready/missed flags for channel and resampler, and overflow flags from many places w/in the chip.
15	Page	Page register

ADDRESS 0: **Sync Mode**, *suggested default = 0x69*

BIT	TYPE	NAME	DESCRIPTION
0,1 (LSBs)	R/W	INT_SYNC	Synchronizes the interpolation control counter. The interpolation counter controls the filtering of each channel. Mode 1 is SIA.
2,3	R/W	COUNTER_SYNC	Synchronizes the sync counter. This counter is used to generate the periodic "TC" sync pulses. Mode 2 is OS, not TC, for the counter. Mode 1 is SIA.
4,5	R/W	OUTPUT_SYNC	The selected sync is inverted and output on the $\overline{\mathbf{SO}}$ pin. Mode 1 is SIA.
6	R/W	USE_ONESHOT	The terminal count mode in table 1 is replaced by ONE_SHOT (OS) when this bit is set.
7	R/W	ONE_SHOT	The one shot sync signal (OS) is generated when this bit is set. If OS_MODE in register 13 is low, then a one shot pulse (one clock cycle wide) is generated. If OS_MODE is high, then the ONE_SHOT sync is active while this bit is high. This bit must be cleared before another one shot pulse can be generated.

ADDRESS 1: **Interpolation Mode**, *suggested default = 0x00*

BIT	TYPE	NAME	DESCRIPTION
0 LSB	R/W	REAL	The input samples are real when this bit is set and are up-converted as a single sideband signal. The input samples are treated as complex when this bit is low. The input rate is $F_{CK}/4N$ when this bit is low and is $F_{CK}/2N$ when this bit is high, where F_{CK} is the chip's clock rate and N is the interpolation setting in registers 3 and 4 (See Section 5.4). If double sideband real data is to be up-converted, then the complex mode should be used with the Q-half set to zero.
1	R/W	SPLIT_IQ	This control bit puts all four channels into the SPLITIQ mode where each channel processes real data at twice the input rate. Two channels work in tandem (A with B and C with D) to process the complex input signal. This mode allows the chip to upconvert two channels at double bandwidth. This mode is used to provide UMTS transmit capability.
2	R/W	GAIN_SYNC	Selects when the input gain is updated. If 0 the input gain (see page 2) takes effect immediately. If 1, then gain is updated on the first sample following SIB.
3	R/W	TEST	Special test mode. Set to 0 for normal use.
4	R/W	NOSYM	When 0 the PFIR filter is symmetric with 63 taps. When 1, the PFIR filter is non-symmetric with 32 taps. The newest data sample is multiplied by h_{31}.
5	R/W	DIAG	Use the diagnostic ramp as input data.
6,7	R/W	DIAG_SYNC	The diagnostic ramp is synchronized by the sync selected by these bits according to table 1. This sync also loads the checksum register. Mode 1 is SIA

ADDRESS 2: **Interpolation Gain**, *suggested default = 0x09*

BIT	TYPE	NAME	DESCRIPTION
0-3	R/W	SCALE	SCALE ranges from 0 to 15.
4,5	R/W	BIG_SHIFT	BIG_SHIFT equals 0, 1 or 2.
6,7	R/W	UNUSED	

The CIC filter has a gain which is equal to N^4. To remove this gain the CIC outputs are shifted down by (3+SCALE+12*BIG_SHIFT) bits and then rounded to 16 bits before they are sent to the mixer circuit. The value chosen for BIG_SHIFT must also satisfy: $2^{(12*BIG\_SHIFT+18)} \geq N^4$. Overflows due to improper gain settings will go undetected if this relationship is violated. This restriction means that BIG_SHIFT is 0 for N between 8 and 22, BIG_SHIFT is 1 for N between 23 and 181, and BIG_SHIFT is 2 for N between 182 and 1448. The interpolation gain settings apply to all channels in the chip.

ADDRESS 3: Interpolation Byte 0, *suggested default = 0x07*

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**INT**[0:7]	The LSBs of the interpolation control word INT. INT is N-1.

ADDRESS 4: Interpolation Byte 1, *suggested default = 0x00*

BIT	TYPE	NAME	DESCRIPTION
0-5	R/W	**INT**[8:13]	The 6 MSBs of the interpolation control word INT. INT is N-1.
6,7	R/W	Unused	

Where **INT** is equal to **N**-1. The chip interpolates the input data by a factor of 2**N** for real input data and 4**N** for complex input data, where **N** ranges from 8 to 16384. This provides an interpolation range from 32 to 65,536 for complex input signals and 16 to 32,768 for real input signals. NOTE: The chip needs to be flushed each time the interpolation registers are changed. See Section 5.8. Values of **N** exceeding 1448 should be avoided since they will cause overflow unless the input signal amplitude is correspondingly reduced. For complex output the signal is decimated by two after the CIC and before the mixer. As a result, the effective interpolation amount is only **N**/2, but the gain needs to be calculated for "**N**". The interpolation factor applies to all channels in the chip.

In the SPLIT_IQ mode (see Section 3.3.4 and bit 1, address 1), INT is set to **INT**=2**N**-1, where N ranges from 4 to 8192.

ADDRESS 5: Reset Register, *Set to 0xff on power up.*

BIT	TYPE	NAME	DESCRIPTION
0 LSB	R/W	RESET_A	This bit resets channel A. It is set during power up. While in reset the channel consumes very modest power (uWatts).
1	R/W	RESET_B	This bit resets channel B.
2	R/W	RESET_C	This bit resets channel C.
3	R/W	RESET_D	This bit resets channel D.
4	R/W	RESAMPLER_RESET	This bit resets the resampler.
5	R/W	NOCK_RESET	Allows output enables to flow through registers in output pads. Set on power up so that all outputs are tristated at power up. The user should reset this bit when ready for outputs to drive.
6	R/W	PAD_RESET	This bit resets the output formatter block.
7	R/W	GLOBAL_RESET	This bit powers down the chip.

The reset register powers up to the reset state of 0xff. The register should be set to 0xff during initialization, and then cleared to begin operation. See Section 3.12 for initialization details.

ADDRESS 6: Counter Byte 0, *suggested default = 0xff*

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**CNT**[0:7]	The LSBs of the counter cycle period

ADDRESS 7: Counter Byte 1, *suggested default = 0xff*

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**CNT**[8:15]	The 8 MSBs of the counter cycle period

The chip's internal sync counter counts in cycles of 128(**CNT**+1) clocks. A terminal count signal (TC) is output at the end of each cycle. The counter can be synchronized to an external sync as specified in the Sync mode Register (See Address 0). If **CNT** is set so that 128(**CNT**+1) is a multiple of twice the interpolation ratio (i.e., a multiple of 16N), then the terminal count of this counter can be output on the $\overline{\textbf{SO}}$ pin and used to periodically synchronize multiple GC4116 chips.

ADDRESS 8: Channel-A Sync Modes, *suggested default = 0x5f*

ADDRESS 9: Channel-B Sync Modes

ADDRESS 10: Channel-C Sync Modes

ADDRESS 11: Channel-D Sync Modes

Registers 8,9,10 and 11 control the synchronization modes of the four channels. The sync modes described here are unique to each of the channels. Sync mode 1 is SIB. The sync modes are shown in Table 1 (See Section 3.11).

BIT	TYPE	NAME	DESCRIPTION
0,1 LSB	R/W	FREQ_SYNC	The new frequency setting takes affect on this sync
2,3	R/W	PHASE_SYNC	The new phase offset takes affect on this sync
4,5	R/W	NCO_SYNC	The NCO is initialized to the phase setting by this sync
6,7 MSB	R/W	DITHER_SYNC	The dither circuit is initialized by this sync to zero.

The NCO_SYNC mode is usually set to be always "off", unless the user wants to coherently control the phases of multiple channels. The FREQ_SYNC and PHASE_SYNC modes are typically set to be always "on" so that frequency and phase settings will take effect immediately as they are written into their control registers (See pages 0 and 1). The DITHER_SYNC is used to turn on or off the dithering of the NCO phase. To turn off dithering set the DITHER_SYNC to be always "on" so that it remains initialized to zero. To turn dithering on set the sync to be always "off". During diagnostics the NCO_SYNC and DITHER_SYNC should be set to "TC".

ADDRESS 12: Channel Flush Register, *suggested default = 0x55*

BIT	TYPE	NAME	DESCRIPTION
0,1 LSB	R/W	FLUSH_A[0:1]	The flush sync for channel A.
2,3	R/W	FLUSH_B[0:1]	The flush sync for channel B.
4,5	R/W	FLUSH_C[0:1]	The flush sync for channel C.
6,7 MSB	R/W	FLUSH_D[0:1]	The flush sync for channel D.

This register controls flushing the four channels. Each channel is flushed when the selected sync occurs. Sync mode 1 is SIA. The sync is selected according to Table 1 in Section 3.11.

Each channel needs to be flushed when the chip is being initialized or when the interpolation control is changed. The flush lasts for 8N clocks after the sync occurs. The channel flush syncs will normally be left in a “never” mode. During diagnostics the channels will need to be flushed at the beginning of each sync cycle.

ADDRESS 13: Miscellaneous Register, *Set to zero on power up*

BIT	TYPE	NAME	DESCRIPTION
0 LSB	R/W	DISABLE_AUTO_FLUSH	The chip normally automatically flushes a channel if instability in the channel’s CIC filter is detected. If this bit is set the auto flush feature is disabled.
1	R/W	MSB_INVERT	Inverts the MSB of the output data (SUMO21) for use with offset binary DACs. Should not be set for chips feeding the sumin port of another GC4116.
2	R/W	COMPLEX_OUT	Complex output is generated with I followed by Q. Interpolation amount is 2N for complex input and N for real input.
3	R/W	EXT_2XCK	For test purposes an external 2x clock can be supplied. This control bit enables its use. Normal use will set this bit to zero.
4	R/W	CK2X_TEST	For test purposes the internally generated 2x clock can be routed to the soB pin for test. Normal use will set this bit to zero.
5	R/W	DISABLE_CK_LOSS	The absence of a clock for extended times (1mS) can cause a current surge. An internal circuit detects this condition prior to the current surge and puts the chip into a reset state. This control bit disables this feature. Normal use will set this bit to zero.
6	R/W	FOUR_OUT _MODE (GC4117 only)	Puts the chip into the GC4117’s four separate output mode. Is only valid for the 208 ball GC4117 package. Must be set low for the 160 ball GC4116 package.
7	R/w	OS_MODE	The ONE_SHOT signal is a level, not a pulse when this bit is set.

ADDRESS 14: Status Register

BIT	TYPE	NAME	DESCRIPTION
0 LSB	R/W	CHAN_INPUT_READY	The user sets this bit after loading the input registers. The chip clears this bit when the values have been read and it is time to load new ones. Part of the channel's parallel input handshake protocol.
1	R/W	CHAN_MISSED	The chip sets this bit If the user has not set the INPUT_READY bit before the chip reads the input registers. This bit high indicates that an error has occurred. Part of the channel's parallel input handshake protocol.
2	R/W	RES_INPUT_READY	The user sets this bit after loading the input registers. The chip clears this bit when the values have been read and it is time to load new ones. Part of the resampler's parallel input handshake protocol.
3	R/W	RES_MISSED	The chip sets this bit If the user has not set the INPUT_READY bit before the chip reads the input registers. This bit high indicates that an error has occurred. Part of the resampler's parallel input handshake protocol.
4	R/W	CHAN_OVERFLOW	Overflow was detected in the CIC shifter.
5	R/W	SUMIO_OVERFLOW	Overflow was detected in the sumio path at the final rounder. For normal uses this should not occur except in the final chip in a sumpath. In the final chip the D/A loading is often optimized to balance clipping and rounding noise resulting in a SUMIO_OVERFLOW every 10,000 to 100,000 samples.
6	R/W	RES_OVERFLOW	This bit is set by the chip if an overflow is detected in the resampler. This should never happen if the resampler is properly programmed.
7	R/W	CK_LOSS_DETECTED	The chip sets this bit if it detects a clock loss.

This register is modified by the chip setting or clearing bits to indicate status of a variety of conditions. The user reads the status register to detect the status and rewrites it to be able to detect the next change in status.

The CHAN_INPUT_READY and RES_INPUT_READY bits are used to tell an external processor when to load new input samples. If desired, the CHREQ and RREQ pins can be used as an interrupt to the external processor to tell the processor when to load new samples. The user does not need to set the INPUT_READY bits if interrupts are used. If INPUT_READY is not set, however, the MISSED flag will not be valid. The same input block design is used for channels and the resampler. The resampler always requires complex input data. The channels can accept real input data. The parallel input mode assumes the data are being entered as complex pairs, even when the data are real. To enter real data in the parallel mode, the user must put two real samples into each complex pair, the first sample in the I-half and the second in the Q-half.

ADDRESS 15: Page Register

BIT	TYPE	NAME	DESCRIPTION
0-5	R/W	Page[0:5]	Page number for addresses 16 through 31.
6,7	R/W	Unused	

5.2 PAGED REGISTERS

Addresses 16 through 31 are used in pages as determined by the page map register (address 15). The page assignments are:

Table 6: Page Assignments

PAGE	DESCRIPTION
0	Frequency and Phase for Channels A and B Also Checksum And Revision Registers
1	Frequency and Phase for Channels C and D
2	Input Gain Settings
3	Channel Input Registers
4	Resampler Input Registers
5	I/O Control Registers
6,7	unused
8	Resampler Control Registers
9	Resampler Ratio Registers
10-15	unused
16-19	Channel A PFIR Coefficients
20-23	Channel B PFIR Coefficients
24-27	Channel C PFIR Coefficients
28-31	Channel D PFIR Coefficients
32-63	Resampler Coefficients

5.3 FREQUENCY AND PHASE PAGES (PAGES 0 AND 1)

Pages 0 and 1 are used to set the tuning frequencies and phase offsets of the four channels. Page 0 also contains the read only checksum diagnostic register and the mask revision register.

The 32 bit frequency control word is defined as: $FREQ = 2^{32}F/F_{CK}$ where F is the desired tuning frequency and F_{CK} is the chip's clock rate (not the CK2X rate). Use positive frequency values to upconvert signals. Use negative frequency values to upconvert inverted spectrums. The 32 bit 2's complement frequency words are entered as four bytes, the least significant byte in the lowest address, the most significant in the highest address.

The 16 bit phase offset is defined as: $PHASE = 2^{16}P/2\pi$ where P is the desired phase in radians from 0 to 2π.

PAGE 0: Channels A and B

ADDRESSES 16, 17, 18, and 19: Frequency Channel A

ADDRESS	TYPE	NAME	DESCRIPTION
16	R/W	FREQ_A[0:7]	Byte 0 (LSBs) of FREQ_A
17	R/W	FREQ_A[8:15]	Byte 1 of FREQ_A
18	R/W	FREQ_A[16:23]	Byte 2 of FREQ_A
19	R/W	FREQ_A[24:31]	Byte 3 (MSBs) of FREQ_A

ADDRESSES 20, 21: Phase Channel A

ADDRESS	TYPE	NAME	DESCRIPTION
20	R/W	PHASE_A[0:7]	Byte 0 (LSBs) of PHASE_A
21	R/W	PHASE_A[8:15]	Byte 1 (MSBs) of PHASE_A

ADDRESSES 24, 25, 26, and 27: Frequency Channel B

ADDRESS	TYPE	NAME	DESCRIPTION
24	R/W	FREQ_B[0:7]	Byte 0 (LSBs) of FREQ_B
25	R/W	FREQ_B[8:15]	Byte 1 of FREQ_B
26	R/W	FREQ_B[16:23]	Byte 2 of FREQ_B
27	R/W	FREQ_B[24:31]	Byte 3 (MSBs) of FREQ_B

ADDRESSES 28, 29: Phase Channel B

ADDRESS	TYPE	NAME	DESCRIPTION
20	R/W	PHASE_B[0:7]	Byte 0 (LSBs) of PHASE_B
21	R/W	PHASE_B[8:15]	Byte 1 (MSBs) of PHASE_B

ADDRESSES 30, 31: Checksum and Revision Registers

ADDRESS	TYPE	NAME	DESCRIPTION
30	Ronly	CHECKSUM	The 8 bit diagnostic checksum. See Section 3.14.
31	Ronly	REVISION	The 8 bit Revision number. See Section 3.16.

PAGE 1: Channels C and D

ADDRESSES 16, 17, 18, and 19: Frequency Channel C

ADDRESS	TYPE	NAME	DESCRIPTION
16	R/W	FREQ_C[0:7]	Byte 0 (LSBs) of FREQ_C
17	R/W	FREQ_C[8:15]	Byte 1 of FREQ_C
18	R/W	FREQ_C[16:23]	Byte 2 of FREQ_C
19	R/W	FREQ_C[24:31]	Byte 3 (MSBs) of FREQ_C

ADDRESSES 20, 21: Phase Channel C

ADDRESS	TYPE	NAME	DESCRIPTION
20	R/W	PHASE_C[0:7]	Byte 0 (LSBs) of PHASE_C
21	R/W	PHASE_C[8:15]	Byte 1 (MSBs) of PHASE_C

ADDRESSES 24, 25, 26, and 27: Frequency Channel D

ADDRESS	TYPE	NAME	DESCRIPTION
24	R/W	FREQ_D[0:7]	Byte 0 (LSBs) of FREQ_D
25	R/W	FREQ_D[8:15]	Byte 1 of FREQ_D
26	R/W	FREQ_D[16:23]	Byte 2 of FREQ_D
27	R/W	FREQ_D[24:31]	Byte 3 (MSBs) of FREQ_D

ADDRESSES 28, 29: Phase Channel D

ADDRESS	TYPE	NAME	DESCRIPTION
20	R/W	PHASE_D[0:7]	Byte 0 (LSBs) of PHASE_D
21	R/W	PHASE_D[8:15]	Byte 1 (MSBs) of PHASE_D

5.4 INPUT GAIN PAGE (PAGE 2)

This page contains independent gain settings for the four channels. Gain is G/128, where G is in two's complement format. Page two registers are listed in the table below.

ADDRESSES 16, 17, 18, and 19: Input Gain

ADDRESS	TYPE	NAME	DESCRIPTION
16	R/W	GAIN_A[0:7]	The gain (G) for channel A
17	R/W	GAIN_B[0:7]	The gain (G) for channel B
18	R/W	GAIN_C[0:7]	The gain (G) for channel C
19	R/W	GAIN_D[0:7]	The gain (G) for channel D

5.5 CHANNEL INPUT PAGE (PAGE 3)

Page 3 is used to enter input data in the parallel mode (see PARALLEL_A,B,C and D in address of the IO control page).

ADDRESSES 16 to 31: Channel Inputs

ADDRESS	TYPE	NAME	DESCRIPTION
16	R/W	CHAN_A_I[0:7]	The 8 LSBs of Channel A's I input
17	R/W	CHAN_A_I[8:15]	The 8 MSBs of Channel A's I input
18	R/W	CHAN_A_QI[0:7]	The 8 LSBs of Channel A's Q input
19	R/W	CHAN_A_Q[8:15]	The 8 MSBs of Channel A's Q input
20	R/W	CHAN_B_I[0:7]	The 8 LSBs of Channel A's I input
21	R/W	CHAN_B_I[8:15]	The 8 MSBs of Channel A's I input
22	R/W	CHAN_B_QI[0:7]	The 8 LSBs of Channel A's Q input
23	R/W	CHAN_B_Q[8:15]	The 8 MSBs of Channel A's Q input
24	R/W	CHAN_C_I[0:7]	The 8 LSBs of Channel A's I input
25	R/W	CHAN_C_I[8:15]	The 8 MSBs of Channel A's I input
26	R/W	CHAN_C_QI[0:7]	The 8 LSBs of Channel A's Q input
27	R/W	CHAN_C_Q[8:15]	The 8 MSBs of Channel A's Q input
28	R/W	CHAN_D_I[0:7]	The 8 LSBs of Channel D's I input
29	R/W	CHAN_D_I[8:15]	The 8 MSBs of Channel D's I input
30	R/W	CHAN_D_QI[0:7]	The 8 LSBs of Channel D's Q input
31	R/W	CHAN_D_Q[8:15]	The 8 MSBs of Channel D's Q input

The CHAN_INPUT_READY and CHAN_MISSED control bits in the status register (address 14) can be used as "handshake" signals between the chip and the external processor providing the data. The external processor sets CHAN_INPUT_READY after it has loaded the channel inputs into page 3. The chip will then clear CHAN_INPUT_READY when it has used the new inputs. The external processor can monitor CHAN_INPUT_READY to determine when it is time to load new inputs. If the external processor has not set CHAN_INPUT_READY when the chip wants to use the inputs, then it will set CHAN_MISSED to let the external processor know that a handshake error has occurred and input samples have been missed.

The external processor can also use the CHREQ output as an interrupt to know new samples are needed.

5.6 RESAMPLER INPUT PAGE (PAGE 4)

Page 4 is used to enter input data in the parallel mode (see PARALLEL_A,B,C and D in address of the IO control page).

ADDRESSES 16 to 31: Resampler Inputs

ADDRESS	TYPE	NAME	DESCRIPTION
16	R/W	RES_A_I[0:7]	The 8 LSBs of Resampler Channel A's I input
17	R/W	RES_A_I[8:15]	The 8 MSBs of Resampler Channel A's I input
18	R/W	RES_A_QI[0:7]	The 8 LSBs of Resampler Channel A's Q input
19	R/W	RES_A_Q[8:15]	The 8 MSBs of Resampler Channel A's Q input
20	R/W	RES_B_I[0:7]	The 8 LSBs of Resampler Channel A's I input
21	R/W	RES_B_I[8:15]	The 8 MSBs of Resampler Channel A's I input
22	R/W	RES_B_QI[0:7]	The 8 LSBs of Resampler Channel A's Q input
23	R/W	RES_B_Q[8:15]	The 8 MSBs of Resampler Channel A's Q input
24	R/W	RES_C_I[0:7]	The 8 LSBs of Resampler Channel A's I input
25	R/W	RES_C_I[8:15]	The 8 MSBs of Resampler Channel A's I input
26	R/W	RES_C_QI[0:7]	The 8 LSBs of Resampler Channel A's Q input
27	R/W	RES_C_Q[8:15]	The 8 MSBs of Resampler Channel A's Q input
28	R/W	RES_D_I[0:7]	The 8 LSBs of Resampler Channel D's I input
29	R/W	RES_D_I[8:15]	The 8 MSBs of Resampler Channel D's I input
30	R/W	RES_D_QI[0:7]	The 8 LSBs of Resampler Channel D's Q input
31	R/W	RES_D_Q[8:15]	The 8 MSBs of Resampler Channel D's Q input

The RES_INPUT_READY and RES_MISSED control bits in the status register (address 14) can be used as "handshake" signals between the chip and the external processor providing the data. The external processor sets RES_INPUT_READY after it has loaded the channel inputs into page 3. The chip will then clear RES_INPUT_READY when it has used the new inputs. The external processor can monitor RES_INPUT_READY to determine when it is time to load new inputs. If the external processor has not set RES_INPUT_READY when the chip wants to use the inputs, then it will set RES_MISSED to let the external processor know that a handshake error has occurred and input samples have been missed.

The external processor can also use the RREQ output as an interrupt to know new samples are needed.

5.7 I/O CONTROL PAGE (PAGE 5)

Page 5 controls the formatting and IO speed of channel and resampler inputs, resampler output, sumout and enables for the various outputs. Page five registers are listed in the table below:

Table 7: IO Control Page Registers (Page 5)

ADDRESS	NAME	DESCRIPTION
16	Channel Input Mode	Channel input format (packed, clock and frame polarity, parallel or serial).
17	Resampler Input Mode	Resampler input format (packed, clock and frame polarity, parallel or serial).
18	Resampler Output Mode	Controls resampler output clock rate, sync, polarity, and frame polarity.
19	Sum IOMode	Sum IO path rounding, delay, shifting, and clear.
20	Serial Controller Modes	Controls request clock rate, sync, and polarity.
21	Serial Controller Frame Count	Sets the serial controller's frame length.
22	Serial Controller Frame Delays A and B	Delay positions for serial controller frame strobes A and B.
23	Serial Controller Frame Delays C and D	Delay positions for serial controller frame strobes C and D.
24	Output Enables	Output enables for sum, resampler, request, frame strobes, sync out, and request polarities.
25	Resampler Clock Divider	Sets the clock rate for the resampler computations
26-31	Unused	

ADDRESS 16: Channel Input Mode Register, *suggested default = 0x01*

BIT	TYPE	NAME	DESCRIPTION
0 LSB	R/W	PACKED	Puts the channel serial inputs into the 32 bit transfer mode where each complex pair is packed into 32 bit words. The complex pair is formatted as I word in the upper 16 bits and the Q word in the lower 16 bits. Each word is formatted as MSB first.
1	R/W	Unused	
2	R/W	SCK_POL	The **SIN** Input bits and **SFS** frame strobes are clocked in on the trailing edge of SCK when this bit is set. The rising edge is used when this bit is low.
3	R/W	SFS_POL	The **SFS** signal is treated as active low when this bit is set. Otherwise the signal is treated as active high.
4	R/W	PARALLEL_A	The parallel/Serial control for channel input A. When low input for channel A is taken from the serial port. When high it is taken from the channel input page registers.
5	R/W	PARALLEL_B	The parallel/Serial control for channel B.
6	R/W	PARALLEL_C	The parallel/Serial control for channel C.
7	R/W	PARALLEL_D	The parallel/Serial control for channel D.

I/O CONTROL PAGE 5 (continue)

ADDRESS 17: Resampler Input Mode Register, *suggested default = 0x03*

BIT	TYPE	NAME	DESCRIPTION
0 LSB	R/W	RES_PACKED	Puts the resampler serial inputs into the 32 bit transfer mode where each complex pair is packed into 32 bit words. The complex pair is formatted as I word in the upper 16 bits and the Q word in the lower 16 bits. Each word is formatted as MSB first.
1	R/W	SC_MODE	Set to zero when the serial controller is being used with the resampler and is set to 1 when it is used with the channels.
2	R/W	RCK_POL	The **RIN** Input bits and **RFS** frame strobes are clocked in on the trailing edge of RSCK when this bit is set. The rising edge is used when this bit is low.
3	R/W	RFS_POL	The **RFS** signal is treated as active low when this bit is set. Otherwise the signal is treated as active high.
4	R/W	RES_PARALLEL_A	The parallel/Serial control for resampler input A. When low input for resampler channel A is taken from the serial port. When high it is taken from the resampler input page registers.
5	R/W	RES_PARALLEL_B	The parallel/Serial control for resampler channel B.
6	R/W	RES_PARALLEL_C	The parallel/Serial control for resampler channel C.
7	R/W	RES_PARALLEL_D	The parallel/Serial control for resampler channel D.

ADDRESS 18: Resampler Output Mode Register, *suggested default = 0x51*

BIT	TYPE	NAME	DESCRIPTION
0-3 LSB	R/W	ROCK_RATE	The resampler serial output clock rate is ROCK = CK/(1+ROCK_RATE). The serial clock changes on the rising edge of CK when ROCK_RATE is even.
4	R/W	ROCK_POL	Resampler serial output clock polarity. Inverts ROCK. When ROCK_POL=0 and ROCK_RATE=0, ROCK is a slightly delayed version of CK.
5	R/W	ROFS_POL	Resampler frame strobe polarity. If low, the frame strobe pulses high for one RCK period prior to the first transmitted bit. If high the frame strobe pulses low.
6,7	R/W	ROCK_SYNC	Sync control for the resampler output clock. The sync settings are 0 =never; 1 = SIA; 2 =SIB; 3=Always.

ADDRESS 19: Sum IOMode Register, *suggested default = 0x80*

BIT	TYPE	NAME	DESCRIPTION
0-2 LSB	R/W	SUM_ROUND	Round the output to 22-(2*SUM_ROUND) bits. The remaining low order bits are cleared. In normal use SUM_ROUND is 0 for all chips in a sum path except the final one. The final one is programmed to match the number of bits used by the D/A or other follow-on devices.
3-5	R/W	SUM_SCALE	Shift the sum output up by SUM_SCALE bits prior to rounding. In normal use SUM_SCALE is 0 for all chips in a sum path except the final one. The final one is typically programmed so that the output has a 14 dB crest factor.
6	R/W	SUM_DELAY	The latency sumin to sumout is 8 cycles. Enabling this bit adds 8 cycles of latency to the output of the 4 internal channels to match the delay from one previous chip.
7	R/W	SUM_CLEAR	Clears sumin data so that regardless of the input to the sumin port it does not affect the sum output.

I/O CONTROL PAGE 5 (continue)

ADDRESS 20: Serial Controller Output Mode Register, *suggested default = 0x51*

BIT	TYPE	NAME	DESCRIPTION
0-3 LSB	R/W	SCCK_RATE	The SCCK output rate is set to SCCK = CK / SCCK_RATE. The serial clock is always approximately 50% duty cycle. The serial clock changes on the rising edge of CK when SCCK_RATE even.
4	R/W	SCCK_POL	Serial controller clock polarity. Inverts REQSCK. When SCCK_POL=0 and SCCK_RATE=0, RCK is a slightly delayed version of CK.
5	R/W	SCFS_POL	Serial controller frame strobe polarity. If low, the frame strobe pulses high for one SCCK period prior to the first transmitted bit. If high the frame strobe pulses low.
6,7	R/W	SCCK_SYNC	Sync control for the SCCK clock. The sync settings are 0 = never; 1=SIA; 2=SIB; 3=Always.

ADDRESS 21: Serial Controller Frame Count, *suggested default = 0x17*

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	SC_FRAME_CNT	The initial value for the serial controller frame counter. Sets the serial controller's frame length.

The frame counter is preloaded with this value and held there until SCSTART. Once SCSTART is received the counter is decremented with each SCCK clock. When the lower four bits are zero and the upper four bits match one of the SC_FRAME_DELAY values, then the respective frame strobe is output. If unpacked then bit 4 of the counter is forced to zero for the match, resulting in a pair of strobes separated by 16 clocks for each frame strobe delay value.

ADDRESS 22: SC Frame Delays A and B, *suggested default = 0x11*

BIT	TYPE	NAME	DESCRIPTION
0-3	R/W	SC_FRAME_DELAY_A	Delay value for serial controller output frame strobe A.
4-7	R/W	SC_FRAME_DELAY_B	Delay value for serial controller output frame strobe B.

ADDRESS 23: SC Frame Delays C and D, *suggested default = 0x11*

BIT	TYPE	NAME	DESCRIPTION
0-3	R/W	SC_FRAME_DELAY_C	Delay value for serial controller output frame strobe C.
4-7	R/W	SC_FRAME_DELAY_D	Delay value for serial controller output frame strobe D.

I/O CONTROL PAGE 5 (continue)

ADDRESS 24: Output Enable Register, *suggested default = 0x3f*

BIT	TYPE	NAME	DESCRIPTION
0 LSB	R/W	SUM_EN	Enable sumout pins.
1	R/W	RES_EN	Enable resampler serial data out, resampler frame strobes, and resampler serial clocks.
2	R/W	REQ_EN	Enable resampler and channel request outputs.
3	R/W	SC_EN	Enable serial controller serial clocks and frame strobes.
4	R/W	SO_EN	Enable the sync output ($\overline{SO}$) pin
5	R/W	Unused	
6	R/W	CHREQ_POL	Invert the channel request. This is useful when the request signal is used as a frame strobe with some DSPs (such as Lucent 1620).
7	R/W	RREQ_POL	Invert the resampler request. This is useful when the request signal is used as a frame strobe with some DSPs (such as Lucent 1620).

ADDRESS 25: Resampler Clock Divide Register, *Must be set to 0x00*

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	RES_CLK_DIV	Resampler clock division.

The resampler clock divider is not functional and must be set to zero.

5.8 RESAMPLER CONTROL PAGE (PAGE 8)

This page controls the resampler. The address assignments are:

Table 8: Resampler Control Registers

ADDRESS	NAME	DESCRIPTION
16	N-channels	Sets the number of resampler channels and filters
17	N-Multiplies	Sets the number of multiplies per output
18	Filter Select	Maps filters to resampler channels
19	Final Shift	Sets the final gain shift
20	Serial Map	Maps serial inputs to resampler channels
21	Ratio Sync	Synchronizes the ratio selection changes.
22	unused	
23	Ratio Map	Maps ratios to resampler channels
24-31	Unused	

ADDRESS 16: N-Channels Out Register, *Suggested default = 0x23*

BIT	TYPE	NAME	DESCRIPTION
0-1 LSB	R/W	NC	Must be set to NC=NCHAN-1, where NCHAN is the number of resampler channels to be generated. A value of NC=0 means one resampler channel. A value of NC=1 means two resampler channels. Use a value of NC=3 for either three or four resampler channels. A value of 2 is illegal and will produce erroneous results.
2-3	R/W	NF	Must be set to NF=NFILTER-1, where NFILTER is the number of resampler filters. Used to partition the resampler coefficient RAM. A value of NF=0 means one filter (normal case). A value of NF=1 means two filters. A value of NF=3 means four filters. A value of 2 is illegal.
4-6	R/W	RES_SYNC	The resampler is synchronized to this sync source. This sync clears the delay accumulators in all channels at the same time. The sync modes are: 0,1 and 5 are “never”, 2=SIA, 3=SIB, 4=OS, and 6,7 are “always”.
7 MSB	R/W	Unused	

ADDRESS 17: N-Multiplies Register, *Suggested default = 0x0E*

BIT	TYPE	NAME	DESCRIPTION
0-5 LSB	R/W	NM	Must be set to NM=NMULT-1, where NMULT is the number of resampler multiplies. The minimum legal value is NM=5, the maximum is NM=63 but typically the maximum will be set by other constraints (see Section 3.7.4). In the case of a single channel output the minimum value is NM=6.
6	R/W	NO_SYM_RES	The resampler filter is presumed to be symmetric unless this bit is set.
7 MSB	R/W	Unused	

RESAMPLER CONTROL PAGE 8 (continue)

ADDRESS 18: Filter Select Register, *Suggested default = 0x00*

BIT	TYPE	NAME	DESCRIPTION
0-1 LSB	R/W	FILTER_SEL_0	The filter map for resampler channel 0. This select which of the NFILTER filters to use for this channel. Must be less than or equal to NFILTER
2-3	R/W	FILTER_SEL_1	The filter map for resampler channel 1.
4-5	R/W	FILTER_SEL_2	The filter map for resampler channel 2.
6-7 MSB	R/W	FILTER_SEL_3	The filter map for resampler channel 3.

ADDRESS 19: Final Shift Register, *Suggested default = 0x14*

BIT	TYPE	NAME	DESCRIPTION
0-3 LSB	R/W	FINAL_SHIFT	The final shift up applied to all resampler channels before rounding and outputting. Legal values are 0-15.
4-5	R/W	ROUND	Round the output to 12 (ROUND=0), 16 (ROUND=1), 20 bits (ROUND=2) or 24 bits (ROUND=3). Note, ROUND must be set to 1 (16 bits).
6,7 (MSB	R/W	Unused	

ADDRESS 20: Serial Map Register, *Suggested default = 0xE4*

BIT	TYPE	NAME	DESCRIPTION
0-1 LSB	R/W	SERIAL_MAP_A	The map for serial input A. This tells the hardware which resampler channel serial input A should be directed to.
2-3	R/W	SERIAL_MAP_B	The map for serial input B.
4-5	R/W	SERIAL_MAP_C	The map for serial input C.
6-7 MSB	R/W	SERIAL_MAP_D	The map for serial input D.

This register maps resampler serial inputs to resampler channels. For most applications this will be a simple map of input A to resampler channel 0, input B to resampler channel 1, etc. However, for two channel and one channel modes the mapping is non-standard. The resampler input buffer requires that serial input D is always active, so in the single channel mode serial input D must be mapped to resampler channel 0. This requires the serial map register to be set to 0x00. For two channels, serial inputs C and D will be active and they should be mapped to resampler channels 0 and 1. This requires the serial map register to be set to 0x40.

ADDRESS 21: Ratio Sync, *Suggested default = 0x20*

BIT	TYPE	NAME	DESCRIPTION
0-3 LSB	R/W	TEST	For Factory test purposes, must be set to zero.
4-6	R/W	RATIO_SYNC	Changes to the ratio map (address 23) are synchronized to this sync source. The sync modes are: 0,1 and 5 are “never”, 2=SIA, 3=SIB, 4=OS, and 6,7 are “always”.
7 MSB	R/W	Unused	

When processing complex input signals partial results are computed in adjacent channels that must be summed together to produce a meaningful result. This control bit informs the resampler to save the data presented to it’s input and add it to the next sample presented (if the chip is properly set up this will be from the next channel). In this manner the real and imaginary portions of the input are rejoined prior to resampling.

RESAMPLER CONTROL PAGE 8 (continue)

ADDRESS 23: Ratio Map Register *Suggested default = 0x00*

BIT	TYPE	NAME	DESCRIPTION
0-1 LSB	R/W	RATIO_MAP_0	The ratio map for resampler channel 0. This tells the hardware which resampler ratio should be use for resampler channel 0.
2-3	R/W	RATIO_MAP_1	The ratio map for resampler channel 1.
4-5	R/W	RATIO_MAP_2	The ratio map for resampler channel 2.
6-7 MSB	R/W	RATIO_MAP_3	The ratio map for resampler channel 3.

The default ratio maps select ratio 0 for all four channels. The resampler in the GC4116 must use the same ratio for all resampler channels, which means that the valid values for the ratio map are 0x00, 0x55, 0xAA and 0xFF to select ratio 0, 1, 2 or 3.

The ratio maps can also be used to synchronously switch between resampling ratios. This allows the chip's resampler to be used in timing loops where the ratio must toggle between several values which have been programmed into the chip.

5.9 RESAMPLER RATIO PAGE (PAGE 9)

This page stores four resampler ratios to be used by the resampler channels. Each ratio is the 32 bit ratio of the input sample rate to the output sample rate with an implicit decimal point six bits down from the top. The total range for the ratio is then 0 to 63. The hardware limits the decimation to be less than 32 (hence the MSB of the 32 bit word should always be zero).

$$RATIO = 2^{26}(\text{Input Sample Rate})/(\text{Output Sample Rate})$$

Table 9: Resampler Ratio Page

ADDRESS	NAME	ADDRESS	NAME
16	RATIO_0 (LSBs)	24	RATIO_2 (LSBs)
17	RATIO_0	25	RATIO_2
18	RATIO_0	26	RATIO_2
19	RATIO_0 (MSBs)	27	RATIO_2 (MSBs)
20	RATIO_1 (LSBs)	28	RATIO_3 (LSBs)
21	RATIO_1	29	RATIO_3
22	RATIO_1	30	RATIO_3
23	RATIO_1 (MSBs)	31	RATIO_3 (MSBs)

The ratio map register selects which ratio is used by the resampler.

5.10 PFIR COEFFICIENT PAGES (PAGES 16 to 31)

The user programmable filter PFIR coefficients are stored using pages16 to 19 for channel A, pages 20 to 23 for channel B, pages 24 to 27 for channel C, and pages 28 to 31 for channel D.

Table 10: PFIR Coefficient Pages

Address	Pages 16, 20, 24 or 28	Pages 17, 21, 25 or 29	Pages 18, 22, 26 or 30	Pages 19, 23, 27 or 31
	Description	Description	Description	Description
16	h_0 LSBs (end tap)	h_8 LSBs	h_{16} LSBs	h_{24} LSBs
17	h_0 MSBs (end tap)	h_8 MSBs	h_{16} MSBs	h_{24} MSBs
18	h_1 LSBs	h_9 LSBs	h_{17} LSBs	h_{25} LSBs
19	h_1 MSBs	h_9 MSBs	h_{17} MSBs	h_{25} MSBs
20	h_2 LSBs	h_{10} LSBs	h_{18} LSBs	h_{26} LSBs
21	h_2 MSBs	h_{10} MSBs	h_{18} MSBs	h_{26} MSBs
22	h_3 LSBs	h_{11} LSBs	h_{19} LSBs	h_{27} LSBs
23	h_3 MSBs	h_{11} MSBs	h_{19} MSBs	h_{27} MSBs
24	h_4 LSBs	h_{12} LSBs	h_{20} LSBs	h_{28} LSBs
25	h_4 MSBs	h_{12} MSBs	h_{20} MSBs	h_{28} MSBs
26	h_5 LSBs	h_{13} LSBs	h_{21} LSBs	h_{29} LSBs
27	h_5 MSBs	h_{13} MSBs	h_{21} MSBs	h_{29} MSBs
28	h_6 LSBs	h_{14} LSBs	h_{22} LSBs	h_{30} LSBs
29	h_6 MSBs	h_{14} MSBs	h_{22} MSBs	h_{30} MSBs
30	h_7 LSBs	h_{15} LSBs	h_{23} LSBs	h_{31} LSBs (center tap)
31	h_7 MSBs	h_{15} MSBs	h_{23} MSBs	h_{31} MSBs (center tap)

Coefficient h_0 is the first coefficient and coefficient h_{31} is the center coefficient of the filter's impulse response. The 16 bit 2's complement coefficients are stored in two bytes, least significant byte first, for example, the LSBs of coefficient 0 are stored in address 16 and the MSBs in address 17.

TO LOAD A COEFFICIENT THE USER MUST WRITE THE LSBYTE FIRST FOLLOWED BY THE MSBYTE. Unknown values will be written into the LSBs if the MSB is written first. The coefficient registers are read/write.

5.11 RESAMPLER COEFFICIENT PAGES (PAGES 32-63)

These pages store the 256 resampler coefficients. Storing resampler coefficient values is similar to storing the coefficients for the PFIR filters. The resampler coefficients are 12 bits with the 8 LSBs written in one address, and the upper 4 bits written as the 4 LSBs of the next address. When reading back resampler coefficients the top four bits of the second address always read back zero.

The resampler coefficient RAM must be written in blocks of eight addresses (four coefficients). Writes to the RAM occur when a write is done to addresses 23 or 31. Supplying coefficients in sequential order will write correctly to the RAM. If just a portion of the resampler coefficient RAM is to be updated, then one must write in blocks of the eight addresses 16 to 23, or 24 to 31. Writing to less than eight addresses will either result in no change to the RAM or unknown changes to some coefficients.

TO LOAD A COEFFICIENT THE USER MUST WRITE IN BLOCKS OF FOUR COEFFICIENTS. ONE MUST WRITE TO ADDRESSES 16-22 THEN ADDRESS 23 OR TO ADDRESSES 24-30 THEN ADDRESS 31.

Table 11: Resampler Coefficient Pages (Single filter mode)

Address	Page															
	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
16	h_0	h_8	h_{16}	h_{24}	h_{32}	h_{40}	h_{48}	h_{56}	h_{64}	h_{72}	h_{80}	h_{88}	h_{96}	h_{104}	h_{112}	h_{120}
17	h_0	h_8	h_{16}	h_{24}	h_{32}	h_{40}	h_{48}	h_{56}	h_{64}	h_{72}	h_{80}	h_{88}	h_{96}	h_{104}	h_{112}	h_{120}
18	h_1	h_9	h_{17}	h_{25}	h_{33}	h_{41}	h_{49}	h_{57}	h_{65}	h_{73}	h_{81}	h_{89}	h_{97}	h_{105}	h_{113}	h_{121}
19	h_1	h_9	h_{17}	h_{25}	h_{33}	h_{41}	h_{49}	h_{57}	h_{65}	h_{73}	h_{81}	h_{89}	h_{97}	h_{105}	h_{113}	h_{121}
20	h_2	h_{10}	h_{18}	h_{26}	h_{34}	h_{42}	h_{50}	h_{58}	h_{66}	h_{74}	h_{82}	h_{90}	h_{98}	h_{106}	h_{114}	h_{122}
21	h_2	h_{10}	h_{18}	h_{26}	h_{34}	h_{42}	h_{50}	h_{58}	h_{66}	h_{74}	h_{82}	h_{90}	h_{98}	h_{106}	h_{114}	h_{122}
22	h_3	h_{11}	h_{19}	h_{27}	h_{35}	h_{43}	h_{51}	h_{59}	h_{67}	h_{75}	h_{83}	h_{91}	h_{99}	h_{107}	h_{115}	h_{123}
23	h_3	h_{11}	h_{19}	h_{27}	h_{35}	h_{43}	h_{51}	h_{59}	h_{67}	h_{75}	h_{83}	h_{91}	h_{99}	h_{107}	h_{115}	h_{123}
24	h_4	h_{12}	h_{20}	h_{28}	h_{36}	h_{44}	h_{52}	h_{60}	h_{68}	h_{76}	h_{84}	h_{92}	h_{100}	h_{108}	h_{116}	h_{124}
25	h_4	h_{12}	h_{20}	h_{28}	h_{36}	h_{44}	h_{52}	h_{60}	h_{68}	h_{76}	h_{84}	h_{92}	h_{100}	h_{108}	h_{116}	h_{124}
26	h_5	h_{13}	h_{21}	h_{29}	h_{37}	h_{45}	h_{53}	h_{61}	h_{69}	h_{77}	h_{85}	h_{93}	h_{101}	h_{109}	h_{117}	h_{125}
27	h_5	h_{13}	h_{21}	h_{29}	h_{37}	h_{45}	h_{53}	h_{61}	h_{69}	h_{77}	h_{85}	h_{93}	h_{101}	h_{109}	h_{117}	h_{125}
28	h_6	h_{14}	h_{22}	h_{30}	h_{38}	h_{46}	h_{54}	h_{62}	h_{70}	h_{78}	h_{86}	h_{94}	h_{102}	h_{110}	h_{118}	h_{126}
29	h_6	h_{14}	h_{22}	h_{30}	h_{38}	h_{46}	h_{54}	h_{62}	h_{70}	h_{78}	h_{86}	h_{94}	h_{102}	h_{110}	h_{118}	h_{126}
30	h_7	h_{15}	h_{23}	h_{31}	h_{39}	h_{47}	h_{55}	h_{63}	h_{71}	h_{79}	h_{87}	h_{95}	h_{103}	h_{111}	h_{119}	h_{127}
31	h_7	h_{15}	h_{23}	h_{31}	h_{39}	h_{47}	h_{55}	h_{63}	h_{71}	h_{79}	h_{87}	h_{95}	h_{103}	h_{111}	h_{119}	h_{127}

Address	Page															
	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
16	h_{128}	h_{136}	h_{144}	h_{152}	h_{160}	h_{168}	h_{176}	h_{184}	h_{192}	h_{200}	h_{208}	h_{216}	h_{224}	h_{232}	h_{240}	h_{248}
17	h_{128}	h_{136}	h_{144}	h_{152}	h_{160}	h_{168}	h_{176}	h_{184}	h_{192}	h_{200}	h_{208}	h_{216}	h_{224}	h_{232}	h_{240}	h_{248}
18	h_{129}	h_{137}	h_{145}	h_{153}	h_{161}	h_{169}	h_{177}	h_{185}	h_{193}	h_{201}	h_{209}	h_{217}	h_{225}	h_{233}	h_{241}	h_{249}
19	h_{129}	h_{137}	h_{145}	h_{153}	h_{161}	h_{169}	h_{177}	h_{185}	h_{193}	h_{201}	h_{209}	h_{217}	h_{225}	h_{233}	h_{241}	h_{249}
20	h_{130}	h_{138}	h_{146}	h_{154}	h_{162}	h_{170}	h_{178}	h_{186}	h_{194}	h_{202}	h_{210}	h_{218}	h_{226}	h_{234}	h_{242}	h_{250}
21	h_{130}	h_{138}	h_{146}	h_{154}	h_{162}	h_{170}	h_{178}	h_{186}	h_{194}	h_{202}	h_{210}	h_{218}	h_{226}	h_{234}	h_{242}	h_{250}
22	h_{131}	h_{139}	h_{147}	h_{155}	h_{163}	h_{171}	h_{179}	h_{187}	h_{195}	h_{203}	h_{211}	h_{219}	h_{227}	h_{235}	h_{243}	h_{251}
23	h_{131}	h_{139}	h_{147}	h_{155}	h_{163}	h_{171}	h_{179}	h_{187}	h_{195}	h_{203}	h_{211}	h_{219}	h_{227}	h_{235}	h_{243}	h_{251}
24	h_{132}	h_{140}	h_{148}	h_{156}	h_{164}	h_{172}	h_{180}	h_{188}	h_{196}	h_{204}	h_{212}	h_{220}	h_{228}	h_{236}	h_{244}	h_{252}
25	h_{132}	h_{140}	h_{148}	h_{156}	h_{164}	h_{172}	h_{180}	h_{188}	h_{196}	h_{204}	h_{212}	h_{220}	h_{228}	h_{236}	h_{244}	h_{252}
26	h_{133}	h_{141}	h_{149}	h_{157}	h_{165}	h_{173}	h_{181}	h_{189}	h_{197}	h_{205}	h_{213}	h_{221}	h_{229}	h_{237}	h_{245}	h_{253}
27	h_{133}	h_{141}	h_{149}	h_{157}	h_{165}	h_{173}	h_{181}	h_{189}	h_{197}	h_{205}	h_{213}	h_{221}	h_{229}	h_{237}	h_{245}	h_{253}
28	h_{134}	h_{142}	h_{150}	h_{158}	h_{166}	h_{174}	h_{182}	h_{190}	h_{198}	h_{206}	h_{214}	h_{222}	h_{230}	h_{238}	h_{246}	h_{254}
29	h_{134}	h_{142}	h_{150}	h_{158}	h_{166}	h_{174}	h_{182}	h_{190}	h_{198}	h_{206}	h_{214}	h_{222}	h_{230}	h_{238}	h_{246}	h_{254}
30	h_{135}	h_{143}	h_{151}	h_{159}	h_{167}	h_{175}	h_{183}	h_{191}	h_{199}	h_{207}	h_{215}	h_{223}	h_{231}	h_{239}	h_{247}	h_{255}
31	h_{135}	h_{143}	h_{151}	h_{159}	h_{167}	h_{175}	h_{183}	h_{191}	h_{199}	h_{207}	h_{215}	h_{223}	h_{231}	h_{239}	h_{247}	h_{255}

Table 11 shows the coefficient register assignments when there is a single filter (NF=0). For two filters (NF=1), the two filters are interleaved, i.e., the h_{even} in Table 11 will contain one filter and h_{odd} will contain the other. Four four filters (NF=3), the four filters are interleaved, i.e., h_0, h_4, h_8, ... is the first filter, h_1, h_5, ... is the second, etc.

6.0 SPECIFICATIONS

6.1 ABSOLUTE MAXIMUM RATINGS

Table 12: Absolute Maximum Ratings

CAUTION: Exceeding the absolute maximum ratings (min or max) may cause permanent damage to the part. These are stress only ratings and are not intended for operation.

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Pad Ring Supply Voltage	V_{PAD}	-0.3	4.1	V	
Core Supply Voltage	V_{CORE}	-0.3	3.0	V	
Input voltage (undershoot and overshoot)	V_{IN}	-0.5	V_{PAD}+0.5	V	
Storage Temperature	T_{STG}	-65	150	^{o}C	
Junction Temperature under operation	T_J		125	^{o}C	1
Lead Soldering Temperature (10 seconds)			300	^{o}C	
ESD Classification	Class 3A Human Body Model (4 kV) (JESD22-A114-B) Class 4 Charged Device Model (1 kV) (JESD22-C101-A)				
Moisture Sensitivity	Class 2				

1. The circuit is designed for junction temperatures up to 125C. Sustained operation above 125C junction temperature will reduce long term reliability.

6.2 RECOMMENDED OPERATING CONDITIONS

Table 13: Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Pad Ring Supply Voltage	V_{PAD}	3.0	3.6	V	1
Core Supply Voltage	V_{CORE}	2.3	2.7	V	1
Temperature Ambient, no air flow	T_A	-40	+85	^{o}C	1
Junction Temperature	T_J		100	^{o}C	2

1. DC and AC specifications in Tables 15 and 16 are production tested over these ranges.
2. Thermal management may be required for full rate operation, See Table 22 below and Section 7.4.

6.3 THERMAL CHARACTERISTICS

Table 14: Thermal Data

THERMAL CONDUCTIVITY	SYMBOL	160 PBGA		UNITS
		0.5 Watt	1 Watt	
Theta Junction to Ambient	θ_{JA}	TBD	TBD	^{o}C/W
Theta Junction to Case	θ_{JC}	TBD	TBD	^{o}C/W

Note: Air flow will reduce θ**ja** and is highly recommended.

6.4 POWER CONSUMPTION

The power consumption is a function of the operating mode of the chip. The following equation estimates the typical power supply current for the chip. Chip to chip variation is typically +/- 5%. The AC specification in Table 16 is the current tested for during production test and represents the absolute maximum power supply current.

$$I_{PAD}\ (TYP)\ =\ (V_{PAD})\left(\frac{F_{CK}}{4}\right)(N_{out})(C_{out})$$

$$I_{CORE}\ (TYP)\ =\ \left(\frac{V_{CORE}}{2.5}\right)\left(\frac{F_{CK}}{100M}\right)\left[20 + A\left(30 + \frac{450}{N}\right) + 15R\right]mA$$

Where A is the number of active channels (0 to 4), N is the CIC decimation ratio, $F_{CK}$is the clock rate, Nout is the number of active output data pins, and Cout is the average capacitive load on each data pin. R is one if the resampler is active, and is 0 if the resampler is off (RES_RESET=1 in address 5). The equation assumes random data transition density of 1 rising edge per four clock cycles.

6.5 DC CHARACTERISTICS

Table 15: DC Operating Conditions (-40 to 85°C case unless noted)

PARAMETER	SYMBOL	V_{PAD} = 3.0 to 3.6V		UNITS	TEST LEVEL
		MIN	MAX		
Voltage input low	V_{IL}		0.8	V	IV
Voltage input high	V_{IH}	2.3		V	IV
Voltage output low (I_{OL} = 2mA)	V_{OL}		0.5	V	IV
Voltage output high (I_{OH} = -2mA)	V_{OH}	2.4		V	IV
Leakage current (V_{IN} = 0V or V_{PAD}) Inputs or Outputs in tristate condition	$\mid I_{IN} \mid$		1	uA	IV
Pullup current (V_{IN} = 0V) (**TDI, TMS, TCK**)	$\mid I_{PU} \mid$	5	35	uA	IV
Quiescent supply current, I_{CORE} or I_{PAD} (V_{IN}=0 or V_{IN}=V_{PAD}, Address 0 = F0, LVDS=0)	I_{CCQ}		2	mA	IV
Data input capacitance (All inputs except **CK**)	C_{IN}	4 (typical)		pF	I
Clock input capacitance (**CK** input)	C_{CK}	13 (typical)		pF	I

Notes:
Currents are measured at nominal voltages, high temperature (85C).
Voltages are measured at low speed. Output voltages are measured with the indicated current load

Test Levels:
I. Controlled by design and process and not directly tested or recommended practice.
II. Verified on initial part evaluation.
III. 100% tested at room temperature, sample tested at hot and cold.
IV. 100% tested at hot, sample tested cold.
V. 100% tested at hot and cold.

6.6 AC CHARACTERISTICS

Table 16: AC Characteristics (-40 TO +85^{o}C Case, unless noted)

PARAMETER	SYMBOL	2.3 V to 2.7 V		UNITS	TEST LEVEL
		MIN	MAX		
Clock Frequency	F_{CK}	Note 1	100	MHz	IV
Clock low or high period	$t_{CKL/H}$	3		ns	IV
Clock Duty Cycle (t_{CKH} as a percentage of the clock period)			70	%	II
Clock rise and fall times (V_{IL} to V_{IH})	t_{RF}		2	ns	I
Input setup before **CK** goes high (**IN** or **$\overline{SI}$**)	t_{SU}	2		ns	IV
Input hold time after **CK** goes high	t_{HD}	0.8		ns	IV
Serial Clock Frequency	F_{SCK}	0	100	MHz	IV
Serial Clock low or high period	$t_{SCKL/H}$	3		ns	IV
Serial Data Setup before SCK	t_{SSU}	2		ns	IV
Serial Data Hold from SCK	t_{SHD}	0.8			IV
Data output delay from rising edge of **CK**. (**OUT, CHREQ, RSREQ, QFLG** or **$\overline{SO}$**)	t_{DLY}	1	5	ns	IV
Output skew between **SCCK** and **SCFS**	t_{SCSK}	-2	2.5	ns	IV
Output skew between **ROCK** and **ROFS or ROUT**	t_{ROSK}	-2	2.5	ns	IV
JTAG Clock Frequency	F_{JCK}	0	40	MHz	IV
JTAG Clock low or high period	$t_{JCKL/H}$	10		ns	IV
JTAG Input (**TDI** or **TMS**) setup before **TCK** goes high	t_{JSU}	5		ns	IV
JTAG Input (**TDI** or **TMS**) hold time after **TCK** goes high	t_{HD}	10		ns	IV
JTAG output (**TDO**) delay from rising edge of **TCK**.	t_{DLY}		10	ns	IV
Control Setup before both **$\overline{CE}$**, **$\overline{WR}$** or **$\overline{RD}$** go low (See section 3.1)	t_{CSU}	2		ns	IV
Control data setup during writes (edge mode). (See section 3.1)	t_{EWCSU}	4		ns	IV
Control hold after **$\overline{CE}$**, **$\overline{WR}$** or **$\overline{RD}$** go high. (See section 3.1)	t_{CHD}	1		ns	IV
Control strobe (**$\overline{CE}$** or **$\overline{WR}$**) pulse width (Write operation). (See section 3.1)	t_{CSPW}	20		ns	IV
Control recovery time between reads or writes. (See section 3.1)	t_{REC}		20	ns	IV
Control output delay **$\overline{CE}$** and **$\overline{RD}$** low to **C** (Read Operation). (See section 3.1)	t_{CDLY}		12	ns	IV
Control tristate delay after **$\overline{CE}$** and **$\overline{RD}$** go high. (See section 3.1)	t_{CZ}		4	ns	I
Supply current (F_{CK} =100MHz, N=9, all channels active). (See section 6.4)	I_{CORE}		395	mA	IV

Notes:
1. The minimum clock rate must satisfy $F_{CK}/(4N)$ > 10KHz, where N is the CIC interpolation ratio.
2. Timing between signals is measured from mid-voltage ($V_{PAD}/2$) to mid-voltage. Output loading is a 50 Ohm transmission line.

Test Levels:
I. Controlled by design and process and not directly tested or recommended practice.
II. Verified on initial part evaluation.
III. 100% tested at room temperature, sample tested at hot and cold.
IV. 100% tested at hot, sample tested cold.
V. 100% tested at hot and cold.

6.7 APPLICATION NOTES

6.8 POWER AND GROUND CONNECTIONS

The GC4116 chip is a very high performance chip which requires solid power and ground connections to avoid noise on the V_{CC}, V_{PAD} and GND pins. If possible the GC4116 chip should be mounted on a circuit board with dedicated power and ground planes and with at least two decoupling capacitors (0.01 μf), one for V_{CC} and one for V_{PAD} adjacent to each side of the GC4116 chip. If dedicated power and ground planes are not possible, then the user should place decoupling capacitors across as many V_{CC} or V_{PAD} and GND pairs as is practical.

IMPORTANT

The GC4116 chip may not operate properly if these power and ground guidelines are violated.

6.9 STATIC SENSITIVE DEVICE

The GC4116 chips are fabricated in a high performance CMOS process which is sensitive to the high voltage transients caused by static electricity. These parts can be permanently damaged by static electricity and should only be handled in static free environments. The parts are tested to exceed 2 Kv human body model.

6.10 MOISTURE SENSITIVE PACKAGE

The GC4016 come in level 2 moisture sensitive packages. Dry pack storage is required prior to assembly.

6.11 THERMAL MANAGEMENT

The parameters in Section 6.0 are tested at a junction temperature of 100^{O}C. In any case, the junction temperature must be kept below 125 ^{O}C for reliable operation. To determine the junction temperature, the user should calculate the chip's power dissipation using the equation for supply current in Section 6.4 and then use the package's thermal conductivity shown in Section 6.3. The junction temperature is calculated by adding the operating ambient temperature (or case temperature) to the product of the power consumption times the thermal conductivity.

For example, the GC4116 chip operating in the GSM mode described in Section 7.8, consumes 0.XX Watts of power. The junction to ambient rise of the 160 BGA package is XXX degrees per Watt. This represents a rise of 25 degrees over ambient. This means that under these conditions the ambient temperature has to be less than 75^{O}C to keep the junction temperature below 100^{O}C. Air flow will decrease the thermal resistance by 10% to 40%, allowing ambient temperatures between 78^{O}C and 85^{O}C. Increasing the decimation ratio (N) or decreasing the number of active channels (A) will also allow a higher ambient temperature.

6.12 REFERENCE DESIGNS

Figure 16 illustrates how to use the GC4116 without the Resampler. The Serial Controller generates the serial clock and frame strobes used to clock the data out of the user's data source ASIC or DSP chip. This configuration guarantees that the data will be received by the GC4116 at the correct times. If a serial TDM bus is used as the data source, then the single serial data source is connected to all four serial inputs of the GC4116 chip, and the CHREQ output from the GC4116 chip is used as the frame start signal to the data source chip. The four serial frame strobes are used by the GC4116 chip to identify the appropriate time slots within the TDM stream.

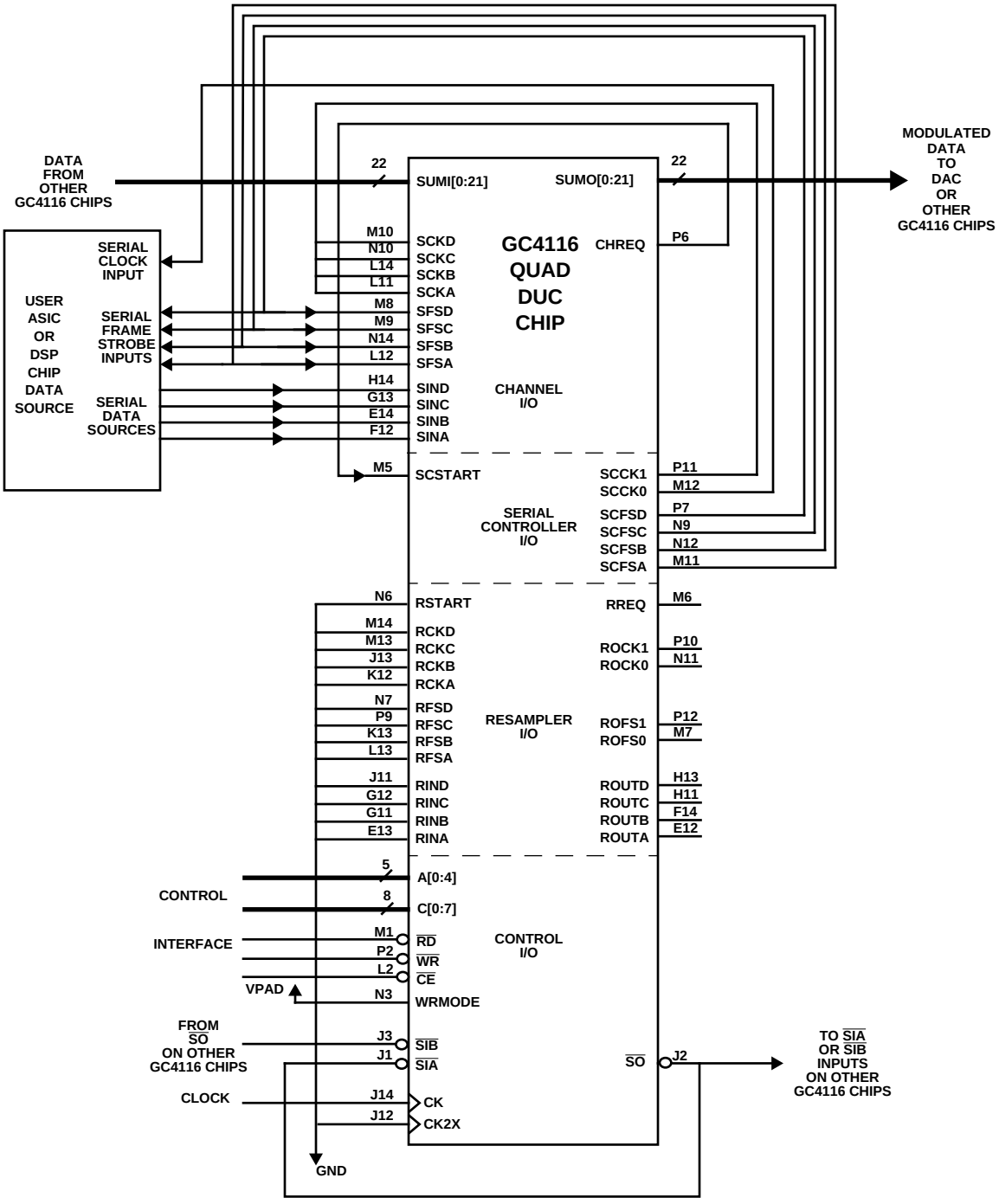


Figure 16. Reference Design Without the Resampler

Figure 17 illustrates how the resampler section is used with the GC4116. As in the previous configuration, TDM serial data can be handled by connecting all four resampler serial inputs to the single TDM source and using the RREQ output as the start of frame signal. In this configuration the resampler outputs drive the channel inputs directly, and the Serial Controller is used to drive the resampler input timing.

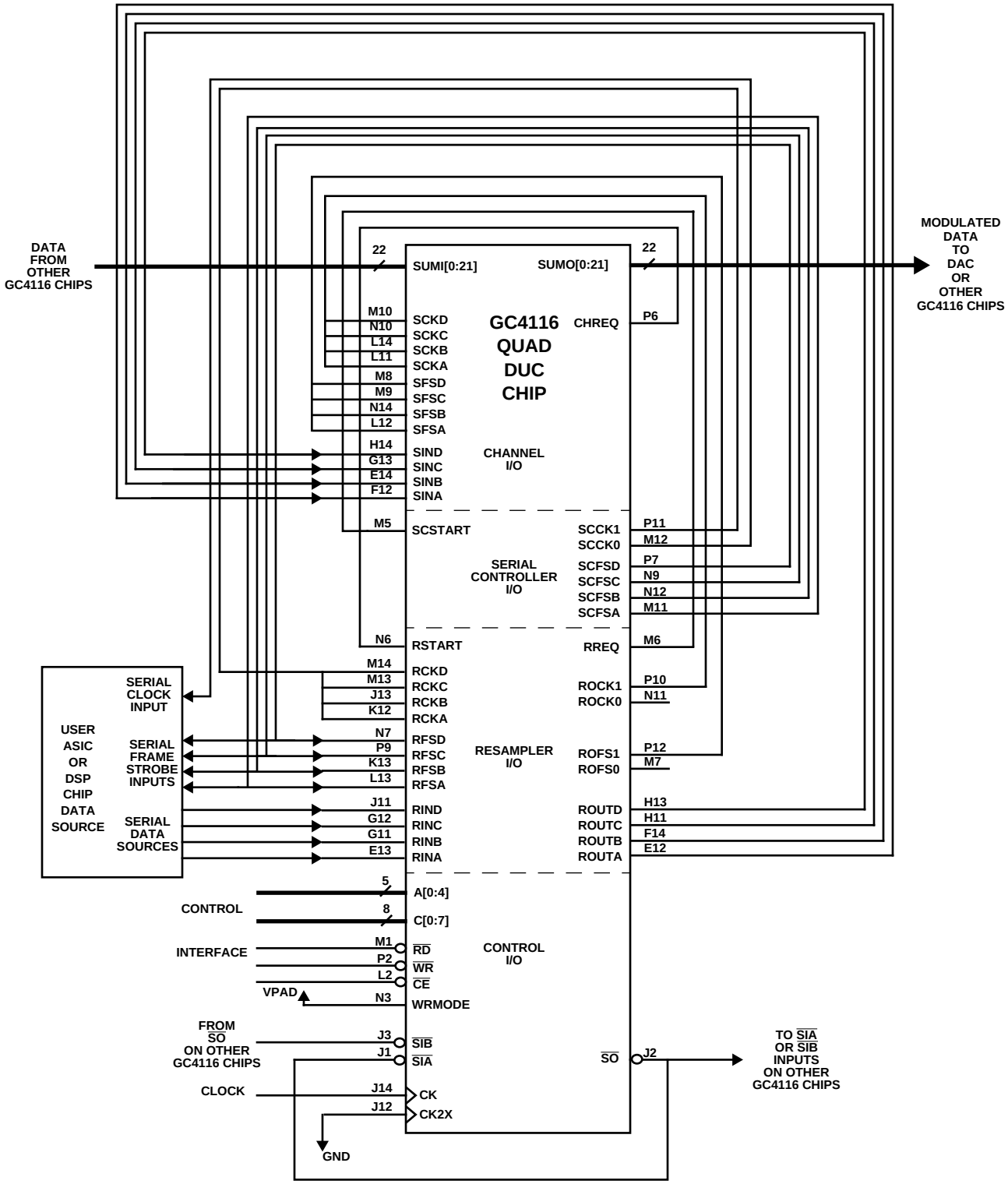


Figure 17. Reference Design Using the Resampler

The following Sections are in progress. Contact GRAYCHIP for the latest information

6.13 EXAMPLE PFIR FILTER SETS

6.14 EXAMPLE RESAMPLER CONFIGURATIONS

6.15 NOISE ANALYSIS

6.16 EXAMPLE GSM APPLICATION

6.17 EXAMPLE IS-136 DAMPS APPLICATION

6.18 EXAMPLE IS-95 NB-CDMA APPLICATION

6.19 EXAMPLE UMTS WB-CDMA APPLICATION

6.20 DIAGNOSTICS

6.21 OUTPUT TEST CONFIGURATION

6.22 INPUT TEST CONFIGURATION

Graychip reserves the right to make changes in circuit design and/or specifications at any time without notice. The user is cautioned to verify that datasheets are current before placing orders. Information provided by Graychip is believed to be accurate and reliable. No responsibility is assumed by Graychip for its use, nor for any infringement of patents or other rights of third parties which may arise from its use. No license is granted by implication or otherwise under any patent rights of Graychip.

GC4116 REGISTER ASSIGNMENT QUICK REFERENCE GUIDE.

Page	Address	Name	7(MSB)	6	5	4	3	2	1	0(LSB)	Suggested Default
Global	0	Sync Mode	ONE_SHOT	USE_OS	OUTPUT_SYNC (SIA)		COUNTER_SYNC (SIA)		INT_SYNC (SIA)		E9 then 69
	1	Int Mode	DIAG_SYNC (SIA)		DIAG	NOSYM	TEST	GAIN_SYNC	SPLIT_IQ	REAL	00
	2	Int Gain	-		BIG_SHIFT		SCALE				09
	3	Int Byte 0	INT[0:7]								07
	4	Int Byte 1	-		INT[8:13]						00
	5	Reset	GLOBAL	PAD_RESET	NOCK_RESET	RES_RESET	RESET_D	RESET_C	RESET_B	RESET_A	FF then 00
	6	Counter Byte 0	CNT[0:7]								00
	7	Counter Byte 1	CNT[7:15]								00
	8	Chan A Sync	DITHER_SYNC (SIB)		NCO_SYNC (SIB)		PHASE_SYNC (SIB)		FREQ_SYNC (SIB)		5F
	9	Chan B Sync	DITHER_SYNC (SIB)		NCO_SYNC (SIB)		PHASE_SYNC (SIB)		FREQ_SYNC (SIB)		5F
	10	Chan C Sync	DITHER_SYNC (SIB)		NCO_SYNC (SIB)		PHASE_SYNC (SIB)		FREQ_SYNC (SIB)		5F
	11	Chan D Sync	DITHER_SYNC (SIB)		NCO_SYNC (SIB)		PHASE_SYNC (SIB)		FREQ_SYNC (SIB)		5F
	12	Flush	FLUSH_D (SIA)		FLUSH_C (SIA)		FLUSH_B (SIA)		FLUSH_A (SIA)		55
	13	Miscellaneous	OS_MODE	4_OUT_MODE	DIS_CK_LOSS	CK2X_TEST	EXT_CK2X	CMPLX_OUT	MSB_INVERT	NO_AUTO_FL	80
	14	Status	CK_LOSS	RES_OVFLW	SUMIO_OVFL	CHAN_OVFLW	RES_MISSED	RES_IN_RDY	CHAN_MISSD	CHAN_IN_RDY	00
	15	Page	-		PAGE						00
Page 0 Frequency and Phase A,B	16,17,18,19	FREQ_A	32 bit channel A tuning frequency, LSBs in 16, MSBs in 19, FREQ = $2^{32}F/F_{CK}$								00000000
	20,21	PHASE_A	16 bit channel A phase, LSBs in 20, MSBs in 21, PHASE=$2^{16}P/2\pi$								0000
	24,25,26,27	FREQ_B	32 bit channel B tuning frequency, LSBs in 24, MSBs in 27, FREQ = $2^{32}F/F_{CK}$								00000000
	28,29	PHASE_B	16 bit channel B phase, LSBs in 28, MSBs in 29, PHASE=$2^{16}P/2\pi$								0000
	30	Checksum	CHECKSUM								read only
	31	Revision	REVISION								read only
Page 1 Frequency and Phase A,B	16,17,18,19	FREQ_C	32 bit channel C tuning frequency, LSBs in 16, MSBs in 19, FREQ = $2^{32}F/F_{CK}$								00000000
	20,21	PHASE_C	16 bit channel C phase, LSBs in 20, MSBs in 21, PHASE=$2^{16}P/2\pi$								0000
	24,25,26,27	FREQ_D	32 bit channel D tuning frequency, LSBs in 24, MSBs in 27, FREQ = $2^{32}F/F_{CK}$								00000000
	28,29	PHASE_D	16 bit channel D phase, LSBs in 28, MSBs in 29, PHASE=$2^{16}P/2\pi$								0000
Page 2 Input Gain	16	GAIN_A	8 bit input gain (G) for channel A. GAIN = G/128								80
	17	GAIN_B	8 bit input gain (G) for channel B. GAIN = G/128								80
	18	GAIN_C	8 bit input gain (G) for channel C. GAIN = G/128S								80
	19	GAIN_D	8 bit input gain (G) for channel D. GAIN = G/128								80
Page 3 Channel Inputs	16,17	CHAN_A_I	Channel A Input Data, I-Half. LSBs in 16, MSBs in 17								00
	18,19	CHAN_A_Q	Channel A Input Data, Q-Half. LSBs in 18, MSBs in 19								00
	20,21	CHAN_B_I	Channel B Input Data, I-Half. LSBs in 20, MSBs in 21								00
	22,23	CHAN_B_Q	Channel B Input Data, Q-Half. LSBs in 22, MSBs in 23								00
	24,25	CHAN_C_I	Channel C Input Data, I-Half. LSBs in 24, MSBs in 25								00
	26,27	CHAN_C_Q	Channel C Input Data, Q-Half. LSBs in 26, MSBs in 27								00
	28,29	CHAN_D_I	Channel D Input Data, I-Half. LSBs in 28, MSBs in 29								00
	30,31	CHAN_D_Q	Channel D Input Data, Q-Half. LSBs in 30, MSBs in 31								00
Page 4 Re-sampler Inputs	16,17	RES_A_I	Resampler A Input Data, I-Half. LSBs in 16, MSBs in 17								00
	18,19	RES_A_Q	Resampler A Input Data, Q-Half. LSBs in 18, MSBs in 19								00
	20,21	RES_B_I	Resampler B Input Data, I-Half. LSBs in 20, MSBs in 21								00
	22,23	RES_B_Q	Resampler B Input Data, Q-Half. LSBs in 22, MSBs in 23								00
	24,25	RES_C_I	Resampler C Input Data, I-Half. LSBs in 24, MSBs in 25								00
	26,27	RES_C_Q	Resampler C Input Data, Q-Half. LSBs in 26, MSBs in 27								00
	28,29	RES_D_I	Resampler D Input Data, I-Half. LSBs in 28, MSBs in 29								00
	30,31	RES_D_Q	Resampler D Input Data, Q-Half. LSBs in 30, MSBs in 31								00
PFIR 16-19	16-31	PFIR_A Taps	32 PFIR Coefficients for channel A. Load LSBs in even addresses, MSBs in odd addresses								
PFIR 20-23	16-31	PFIR_B Taps	32 PFIR Coefficients for channel B. Load LSBs in even addresses, MSBs in odd addresses								
PFIR 24-27	16-31	PFIR_C Taps	32 PFIR Coefficients for channel C. Load LSBs in even addresses, MSBs in odd addresses								
PFIR 28-31	16-31	PFIR_D Taps	32 PFIR Coefficients for channel D. Load LSBs in even addresses, MSBs in odd addresses								

SYNC MODE	SYNC SOURCE
0	off (never asserted)
1	SIA or SIB, See each sync for (SIA) or (SIB)
2	TC (OS if USE_OS is set)
3	on (always active)

GC4116 REGISTER ASSIGNMENT QUICK REFERENCE GUIDE

Page		Address	Name	7(MSB)	6	5	4	3	2	1	0(LSB)	Suggested Default
I O C O N T R O L	7	16	Channel Input	PARALLEL_D	PARALLEL_C	PARALLEL_B	PARALLEL_A	SFS_POL	SCK_POL	-	PACKED	01
		17	Resampler Input	RES_PAR_D	RES_PAR_C	RES_PAR_B	RES_PAR_A	RFS_POL	RCK_POL	SC_MODE	RES_PACKED	03
		18	Resampler Out	ROCK_SYNC (See below)		ROFS_POL	ROCK_POL	ROCK_RATE				51
		19	Sum IO Mode	SUM_CLEAR	SUM_DELAY	SUM_SCALE			SUM_ROUND			80
		20	Serial Controller	SCCK_SYNC (See Below)		SCFS_POL	SCCK_POL	SCCK_RATE				51
		21	SC Frame Count	SC_FRAME_CNT								17
		22	SC FS Delay A,B	SC_FRAME_DELAY_B				SC_FRAME_DELAY_A				11
		23	SC FS Delay C,D	SC_FRAME_DELAY_D				SC_FRAME_DELAY_C				11
		24	Output Enables	RREQ_POL	CHREQ_POL	-	SO_EN	SC_EN	REQ_EN	RES_EN	SUM_EN	1F
		25	Res Clock Divder	RES_CLK_DIV clock rate = $2*F_{CK}/(1+RES\_CLK\_DIV)$								00
R E S A M P L E R	8	16	N-Channels	-	RES_SYNC			NF=(NFILTER-1)		NC =(NCHAN-1)		23
		17	N-Multiplies	-	NO_SYM_RES	NM=(NMULT-1)						0E
		18	Filter Select	FILTER_SEL_3		FILTER_SEL_2		FILTER_SEL_1		FILTER_SEL_0		00
		19	Final Shift	-	-	ROUND (12B,16B, 20B,24B)		FINAL_SHIFT				34
		20	Channel Map	CHAN_MAP_D		CHAN_MAP_C		CHAN_MAP_B		CHAN_MAP_A		E4
		21	Ratio Sync	-	RATIO_SYNC			TEST (must be 0)				70
		22	unused	-								00
		23	Ratio Map	RATIO_MAP_3		RATIO_MAP_2		RATIO_MAP_1		RATIO_MAP_0		00
	9	16-19	Res Ratio 0	RATIO_0, Resampler ratio 0. RATIO = 2^{26}(Resampler input sample rate)/(Resampler output sample rate)								04000000
		20-23	Res Ratio 1	RATIO_1, Resampler ratio 1.								04000000
		24-27	Res Ratio 2	RATIO_2, Resampler ratio 2.								04000000
		28-31	Res Ratio 3	RATIO_3, Resampler ratio 3.								04000000
	32-63	16-31	Filter Taps	Resampler Coefficients, 8 LSBs in even addresses, 4 MSBs in odd addresses. (Must be loaded in the blocks 16-23 and 24-31)								

$$GAIN = \left\{\frac{G}{128}\right\}\left\{\frac{PFIR\_SUM}{65536}\right\}\left\{N^4 2^{-(SCALE + 12 \times BIG\_SHIFT + 3)}\right\}\left\{2^{SUM\_SCALE - 7}\right\} \qquad RES\_GAIN = \left(\frac{RES\_SUM}{32768 \times NDELAY}\right)\left(2^{FINAL\_SHIFT}\right)$$

Sync Circuit	Mode 1	Description	Default	Sync Circuit	Mode 1	Description	Default
INT_SYNC	SIA	Interpolation control counter. Sets timing of CHREQ.	1(SIA)	GAIN_SYNC	SIB	A single bit sync selection. GAIN_SYNC=0 means the gain is applied immediately. GAIN_SYNC=1 means the gain is applied after SIB.	0
COUNTER_ SYNC	SIA	Internal sync counter. Generates TC sync. Mode 2 is always ONE_SHOT	2 (OS)	DIAG_SYNC	SIA	Selects when to start the diagnostic ramp and to store the diagnostic checksum.	2 (TC)
OUTPUT_ SYNC	SIA	The output sync (SO) selection.	2 (TC)	FREQ_SYNC	SIB	Selects when new frequency settings take effect.	3 (on)
ROCK_SYNC	SIA	Syncs the resampler's serial output clock. Mode 2 is SIB.		PHASE_SYNC	SIB	Selects when new phase settings take effect.	3 (on)
SCCK_SYNC	SIA	Syncs the serial controller's serial output clock. Mode 2 is SIB.		NCO_SYNC	SIB	Reset the NCO phase accumulator	0 (off)
RES_SYNC	Note 1	Syncs the resampler during initialization		DITHER_ SYNC	SIB	Clears the NCO dither circuit.	0 (off)
RATIO_SYNC	Note 1	Selects when a new resampler ratio takes effect.		FLUSH _ (A,B,C,D)	SIA	Starts a flush of the channel	1 (SIA)

Note 1: These use a 3 bit sync mode selection where modes 0,1 and 5 are "off", mode 2 is SIA, mode 3 is SIB, mode 4 is ONE_SHOT, and modes 6 and 7 are "on".