HD-LINX™ GS1501
HDTV Serial Digital Formatter with ANC FIFOs

DATA SHEET

KEY FEATURES

- **SMPTE 292M compliant**
- **NRZ(I) encoding**
- **SMPTE 292M scrambler with BYPASS option**
- **internal FIFOs for ANC data insertion (1024 Bytes on Y and C channels)**
- **selectable TRS insertion**
- **selectable line number insertion**
- **selectable line based CRC insertion**
- **selectable active picture illegal code re-mapping**
- **20 bit 3.3V CMOS compatible input data bus**
- **optimized output interface to GS1522**
- **single +3.3V power supply**
- **5V tolerant I/O**

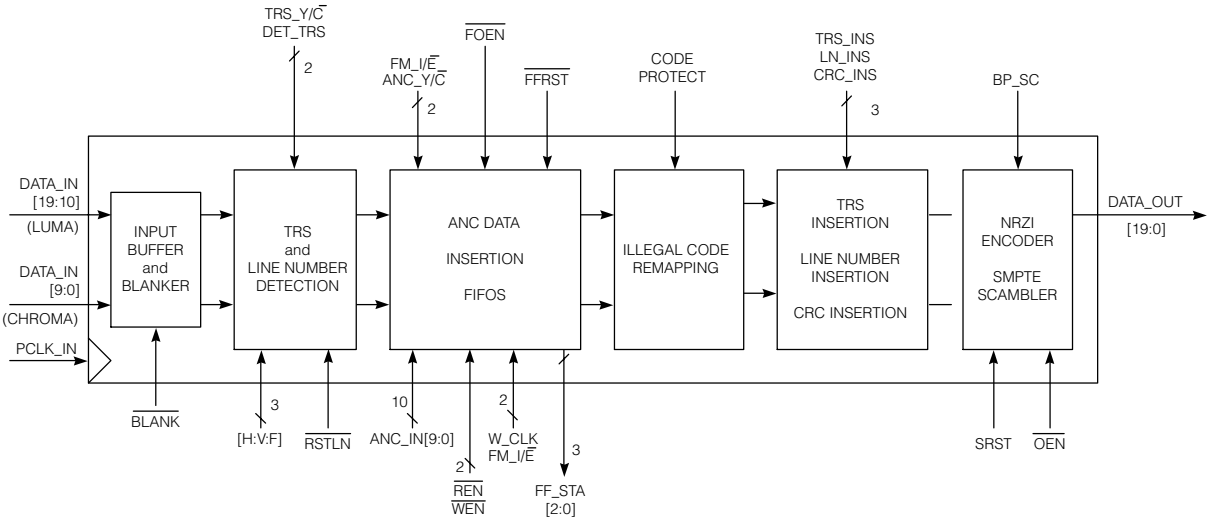
APPLICATIONS

- SMPTE 292M Serial Digital Interfaces

DESCRIPTION

The GS1501 HDTV Serial Digital Formatter formats the HDTV Luma and Chroma data according to SMPTE 292M prior to serialization by the GS1522 HDTV Serializer. The GS1501 optionally inserts TRS and line number signals based on externally supplied H, V and F signals. The device also allows the insertion of CRCs based on TRS signals embedded in the input data streams, should the user choose not to supply external HVF signals.

Following the insertion of TRS, Line Number, and CRC, protected words of 000-003 and 3FC to 3FF occurring during the active video period are optionally re-mapped to 004 and 3FB respectively. In addition, ANC data may be inserted into the video stream through an internal FIFO interface. Prior to exiting the device SMPTE 292M compliant NRZ(I) encoding and scrambling may be performed on the data stream.



GS1501 FUNCTIONAL BLOCK DIAGRAM

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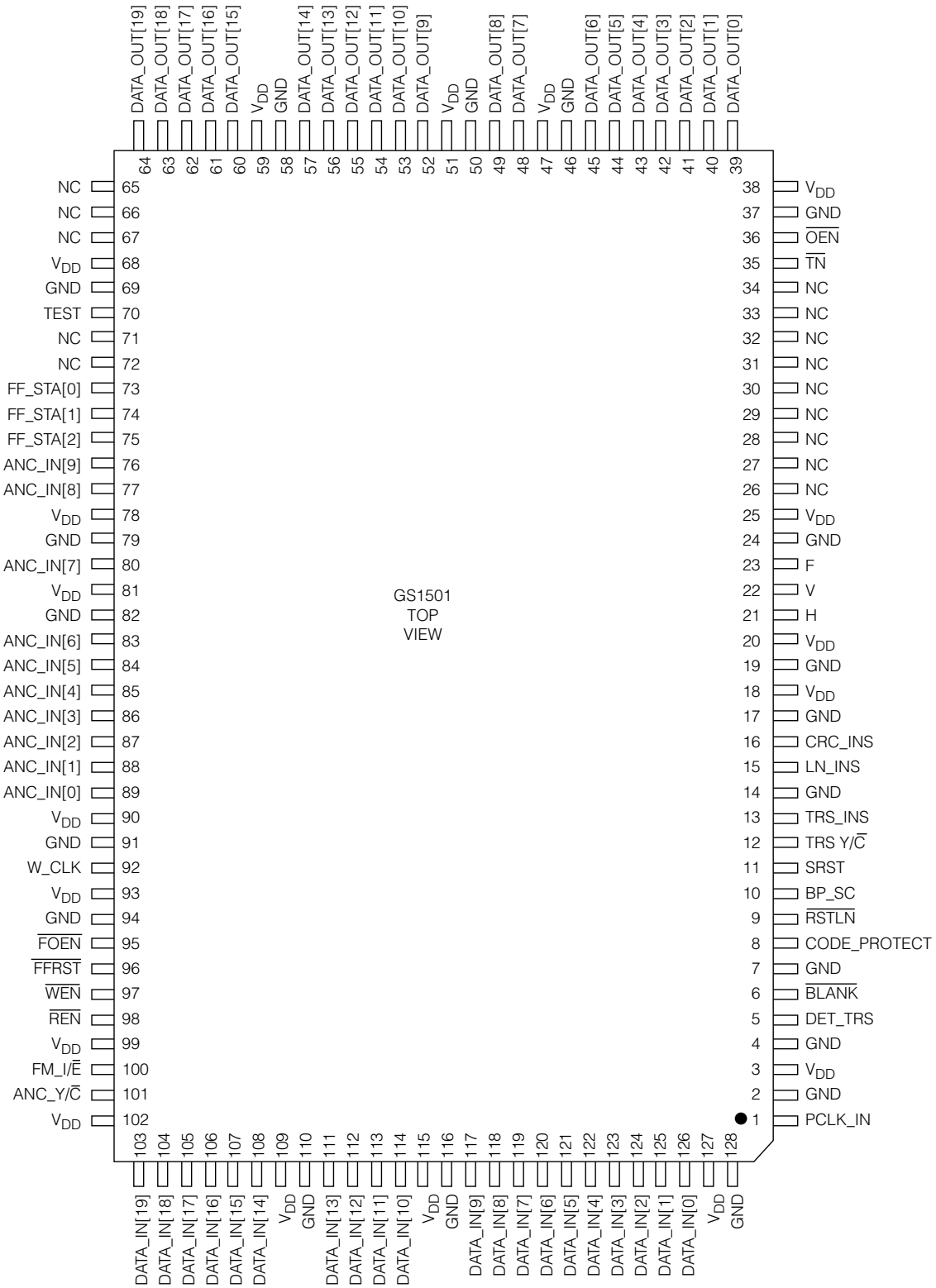
1. PIN OUT

1.1 PIN ASSIGNMENT



1.2 PIN DESCRIPTIONS

PIN NUMBER	NAME	TIMING	TYPE	DESCRIPTION
1	PCLK_IN	Synchronous	Input	**Parallel data clock input.** 74.25MHz or 74.25/1.001MHz.
2, 4, 14, 19, 24, 37, 46, 50, 58, 69, 79, 82, 91, 94, 110, 116, 128	GND	N/A	Ground	**Ground.** Ground power supply connections.
3, 18, 20, 25, 38, 47, 51, 59, 68, 78, 81, 90, 93, 99, 109, 115, 127	V_{DD}	N/A	Power	**Power.** Positive power supply connections.
5	DET_TRS	Non-synchronous	Input	**Control Signal Input.** Used to enable or disable the detection of the TRS signals embedded in the video stream. When DET _TRS is high, the device detects the TRS signals embedded in the input video stream and uses the detected HVF signals instead of the external HVF signals. When DET _TRS is low, TRS detection is disabled. The device uses the external supplied HVF signals.
6	$\overline{\text{BLANK}}$	Synchronous wrt PCLK_IN	Input	**Control Signal Input.** When $\overline{\text{BLANK}}$ is low, the device sets the accompanying LUMA and CHROMA data to their appropriate blanking levels. When $\overline{\text{BLANK}}$ is high, the LUMA and CHROMA data streams pass through this stage of the device unaltered. See Figure 3.
7, 17	GND	N/A		This pin must be connected to GND for normal operation
8	CODE_PROTECT	Non-synchronous	Input	**Control Signal Input.** Used to enable or disable re-mapping of out-of-range words contained in the active portion of the video signal. When this signal is high, the device re-maps out-of-range words contained within the active portion of the video signal into CCIR-601 compliant words. Values between 000-003 are re-mapped to 004. Values between 3FC and 3FF are re-mapped to 3FB. When this signal is low, out-of-range words in the active video region pass through the device unaltered.
9	$\overline{\text{RSTLN}}$	Synchronous wrt PCLK_IN	Input	**Control Signal Input.** Line number reset signal which must be asserted once per frame at the beginning of the frame (for example, on the falling edge of the F signal). A high to low transition will reset the line number counter of the device to one (1). See Figure 2 for timing.
10	BP_SC	Non-synchronous	Input	**Control Signal Input.** Used to enable or bypass the SMPTE292M scrambler and NRZ(I) encoder. When BP_SC is low, the video stream is scrambled according to SMPTE 292M and NRZ(I) encoded. When BP_SC is high, the scrambler and NRZ(I) encoder are by-passed.
11	SRST	Non-synchronous	Input	**Control Signal Input.** Used to reset the SMPTE292M scrambler and NRZI encoder. When SRST is low, the scrambler and encoder operate normally. A low to high transition on SRST causes the scrambler and encoder to reset.
12	TRS_Y/$\overline{\text{C}}$	Non-synchronous	Input	**Control Signal Input.** Only used when DET_TRS is high. When TRS_Y/$\overline{\text{C}}$ is high, the device detects and uses TRS signals embedded in the LUMA (DATA_IN[19:10]) channel. When TRS_Y/$\overline{\text{C}}$ is low, the device detects and uses TRS signals embedded in the CHROMA (DATA_IN[9:0]) channel.

1.2 PIN DESCRIPTIONS (Continued)

PIN NUMBER	NAME	TIMING	TYPE	DESCRIPTION
13	TRS_INS	Non-synchronous	Input	**Control Signal Input.** Used to enable or disable insertion of TRS into the video streams. When TRS_INS is high, the device inserts SMPTE 292M compliant TRS signals into the input LUMA and CHROMA data streams based on the supplied HVF signals. When TRS_INS is low, the device does not insert TRS signals.
15	LN_INS	Non-synchronous	Input	**Control Signal Input.** Used to enable or disable insertion of line numbers into the video stream. When LN_INS is high, the device inserts SMPTE 292M compliant line number information into the LUMA and CHROMA channels. When LN_INS is low, the device does not insert the line number information into the LUMA and CHROMA channels. Line number insertion is only available when user supplied external FVH data is used (DET_TRS set LOW).
16	CRC_INS	Non-synchronous	Input	**Control Signal Input.** Used to enable or disable insertion of CRC's into the video stream. When CRC_INS is high, the device calculates and inserts line based CRCs. When CRC_INS is low, this feature is disabled.
21	H	Synchronous wrt PCLK_IN	Input	**Control Signal Input.** This signal indicates the Horizontal blanking period of the input video data stream. The device inserts HDTV TRS based on the supplied HVF signals. Refer to Figure 4 for required timing of H relative to LUMA (DATA_IN[19:10]) and CHROMA (DATA_IN[9:0]).
22	V	Synchronous wrt PCLK_IN	Input	**Control Signal Input.** This signal indicates the vertical blanking period of the input video data streams. Refer to Figure 4 for required timing of V relative to LUMA (DATA_IN[19:10]) and CHROMA (DATA_IN[9:0]).
23	F	Synchronous wrt PCLK_IN	Input	**Control Signal Input.** This signal indicates the ODD/EVEN field of the input video data streams. Refer to Figure 4 for required timing of F relative to LUMA (DATA_IN[19:10]) and CHROMA (DATA_IN[9:0]). When the input video format is progressive scan, F should remain low at all times.
26, 27, 28, 29, 30, 31, 32, 33, 34, 65, 66, 67, 71, 72,	NC	N/A		**No Connect.** Do not connect these pins
35	$\overline{TN}$	N/A	TEST	**Test Pin.** Used for test purposes only. This pin must be connected to V_{DD} for normal operation
36	$\overline{OEN}$	See A/C Electrical Characteristics section	Input	**Control Signal Input.** Used to enable DATA_OUT[19:0] output bus or set it to a high Z state. When $\overline{OEN}$ is low, the DATA_OUT[19:0] bus is enabled. When $\overline{OEN}$ is high, the DATA_OUT[19:0] bus is disabled and in a high Z state.
64, 63, 62, 61, 60, 57, 56, 55, 54, 53, 52, 49, 48, 45, 44, 43, 42, 41, 40, 39	DATA_OUT[19:0]	Synchronous wrt PCLK_IN	Outputs	**Output Data Bus.** The device generates a 20 bit wide data stream running at 74.25 (or 74.25/1.001) MHz. DATA_OUT[19] is the MSB and DATA_OUT[0] is the LSB.
70	TEST	N/A	TEST	**Test Pin.** Used for test purposes only. This pin must be connected to GND for normal operation.

1.2 PIN DESCRIPTIONS (Continued)

PIN NUMBER	NAME	TIMING	TYPE	DESCRIPTION
75, 74, 73	FF_STA[2:0]		Output	**Control Signal Output.** FF_STA[2:0] is the FIFO status output to indicate the content level of the internal FIFO. FF_STA[2:0]=000: Error flag, FIFO is under run. FF_STA[2:0]=001: FIFO is empty. FF_STA[2:0]=010: FIFO is almost empty (32 bytes filled). FF_STA[2:0]=011: FIFO is ready. FF_STA[2:0]=100: FIFO is half full. FF_STA[2:0]=101: FIFO is almost full (992 bytes filled). FF_STA[2:0]=110: FIFO is full. FF_STA[2:0]=111: Error flag, FIFO is over run. When ANC_Y/$\overline{C}$ is high, FF_STA indicates the status of the LUMA ANC data buffer. When ANC_Y/$\overline{C}$ is low, it indicates the status of the CHROMA ANC data buffer. See timing diagrams Figures 5 to 14 and Table 1.
76, 77, 80, 83, 84, 85, 86, 87, 88, 89	ANC_IN[9:0]	Synchronous wrt W_CLK	Input	**ANC Data Input Bus.** ANC data to be inserted into the video stream is supplied via the ANC_IN[9:0] input data port. ANC_IN[9] is the MSB (pin 76) and ANC_IN[0] is the LSB (pin 89). When FM_I/$\overline{E}$=1, ANC data intended to be placed into the current HANC region is written into the internal FIFO during the time that the preceding active video region is passing through the device. The device begins inserting ANC data stored in the FIFO immediately after the line based CRC words regardless of any other ANC data that may be present in the stream (i.e. the device will over-write existing ANC data in the data stream).
92	W_CLK	N/A	Input	**Input Clock.** Used to write information to the internal FIFO. On the rising edge of W_CLK, externally supplied ANC data may be written into the internal LUMA or CHROMA FIFO as determined by ANC_Y/$\overline{C}$.

1.2 PIN DESCRIPTIONS (Continued)

PIN NUMBER	NAME	TIMING	TYPE	DESCRIPTION
95	$\overline{\text{FOEN}}$	Non-synchronous	Input	**Control Signal Input.** Used to enable or disable the FIFO status flags. When $\overline{\text{FOEN}}$ is low, the FIFO status flags are enabled. When $\overline{\text{FOEN}}$ is high, the FIFO status flags are disabled.
96	$\overline{\text{FFRST}}$	Synchronous wrt PCLK_IN	Input	**Control Signal Input.** $\overline{\text{FFRST}}$ is used to supply synchronous reset signals to the FIFO. When $\overline{\text{FFRST}}$ is low, the FIFO is reset and all internal read and write address pointers are set to their starting locations.
97	$\overline{\text{WEN}}$	Synchronous wrt W_CLK	Input	**Control Signal Input.** Used to enable or disable writing to the internal FIFO. When $\overline{\text{WEN}}$ is high, writing to the internal FIFO is not allowed. Internal write address pointers are stopped at their current position. $\overline{\text{WEN}}$ is sampled on the rising edge of W_CLK. When $\overline{\text{WEN}}$ is low, writing to the FIFO is enabled.
98	$\overline{\text{REN}}$	Synchronous wrt PCLK_IN	Input	**Control Signal Input.** Used to enable or disable incrementation of the internal read address pointers. When $\overline{\text{REN}}$ is low, the internal read address pointers are incremented with each clock pulse. When $\overline{\text{REN}}$ is high, the internal read address pointers are stopped at their current position.
100	FM_I/$\overline{\text{E}}$	Non-synchronous	Input	**Control Signal Input.** When FM_I/$\overline{\text{E}}$ is high, the device operates in a mode where the FIFO reset and read enable signals are generated internally. In this mode, the device limits the data insertion to the HANC region of the video stream. The ANC data to be inserted into the current HANC region are externally supplied via the FIFO interface during the active video period of the previous line using the $\overline{\text{WEN}}$ signal. When FM_I/$\overline{\text{E}}$ is low, the device operates in another mode where the FIFO reset and read enable signals are generated externally by the user and supplied to the device via the $\overline{\text{FFRST}}$ and $\overline{\text{REN}}$ control signal inputs.
101	ANC_Y/$\overline{\text{C}}$	Synchronous wrt W_CLK	Input	**Control Signal Input.** Used to control insertion of ANC data into the LUMA or CHROMA FIFO. When ANC_Y/$\overline{\text{C}}$ is high, data written to the device is placed into the internal LUMA FIFO, or read into the Luma data stream. When ANC_Y/$\overline{\text{C}}$ is low, data written to the device is placed into the internal CHROMA FIFO, or read into the Chroma data stream.
103,104,105, 106, 107, 108, 111, 112, 113, 114	DATA_IN [19:10] (LUMA channel)	Synchronous wrt PCLK_IN	Input	**Input Data Bus.** LUMA CHANNEL. DATA_IN [19] is the MSB of the LUMA input signal (pin 103). DATA_IN [10] is the LSB of the LUMA input signal (pin 114).
117, 118, 119, 120, 121, 122, 123, 124, 125, 126	DATA_IN [9:0] (CHROMA channel)	Synchronous wrt PCLK_IN	Input	**CHROMA Input Data Bus.** CHROMA CHANNEL DATA_IN [9] is the MSB of the CHROMA signal (pin 117). DATA_IN [0] is the LSB of the CHROMA signal (pin 126).

2. ELECTRICAL CHARACTERISTICS

2.1 ABSOLUTE MAXIUMUM RATINGS

PARAMETER	VALUE
Supply Voltage	-0.5V to +4.6V
Input Voltage Range (any input)	$-0.5V < V_{IN} < 5.5V$
Operating Temperature Range	$0°C \le T_A \le 70°C$
Storage Temperature Range	$-40°C \le T_S \le 125°C$
Lead Temperature (soldering 10 seconds)	260°C

2.2 DC ELECTRICAL CHARACTERISTICS

V_{DD} = 3.0 to 3.6V, T_A = 0°C to 70°C, unless otherwise shown

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Positive Supply Voltage	V_{DD}		3.0	3.3	3.6	V	
Supply Current	I_{DD}	f = 74.25MHz, T_A = 25°C	-	413	480	mA	
Input Logic LOW Voltage	V_{IL}	$I_{LEAKAGE} < 10\mu A$	-	-	0.8	V	
Input Logic HIGH Voltage	V_{IH}	$I_{LEAKAGE} < 10\mu A$	2.1	3.3	5.0	V	
Output Logic LOW Voltage	V_{OL}	V_{DD} = 3.0 to 3.6V, I_{OL} = 4mA	-	0.3	0.4	V	
Output Logic HIGH Voltage	V_{OH}	V_{DD} = 3.0 to 3.6V, I_{OH} = -4mA	2.6	-	-	V	

2.3 AC ELECTRICAL CHARACTERISTICS

V_{DD} = 3.0 to 3.6V, T_A = 0°C to 70°C, unless otherwise shown

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Clock Input Frequency	F_{HSCI}		-	74.25	80	MHz	Also supports 74.25/ 1.001MHz
Input Data Setup Time	t_{SU}		2.5	-	-	ns	50% levels
Input Data Hold Time	t_{IH}		1.5	-	-	ns	50% levels
Input Clock Duty Cycle			40	-	60	%	
Output Data Hold Time	t_{OH}	With 15pF load	2.0	-	-	ns	
Output Enable Time	t_{oen}	With 15pF load	-	-	8	ns	
Output Disable Time	t_{odis}	With 15pF load	-	-	10	ns	
Output Data Delay Time	t_{OD}	With 15pF load	-	-	10	ns	Note 2
Output Data Rise/Fall Time		With 15pF load	-	-	2.75	ns	20% to 80% levels
FIFO Input Data Setup Time	t_{FSU}		8.0	-	-	ns	Note 1
FIFO Input Data Hold Time	t_{FIH}		4.0	-	-	ns	Note 1

NOTES:

1. The following signals need to adhere to this timing: ANC_Y/$\overline{C}$, $\overline{REN}$, $\overline{WEN}$, ANC_IN[9:0], $\overline{FFRST}$.
2. Timing of the FF_STA[2:0] outputs may be greater than specified.

3. DETAILED DESCRIPTION

3.1 DATA INPUT AND OUTPUTS

Data enters and exits the device synchronous to the rising edge of PCLK_IN as shown in Figure 1.

3.2 INPUT BLANKER

Data words entering the GS1501 can be dynamically set to Luma and Chroma blanking levels if desired as shown in Figure 3. Blanking is applied to both the LUMA and CHROMA channels simultaneously.

3.3 FIFO

The device does not flag transmission errors which might exist in the ANC data packages. The internal FIFO is 1024 words deep for each of LUMA and CHROMA channels. For those formats where the HANC region is greater than 1024 words, the user must take steps to ensure the FIFO does not overflow, otherwise data may be lost. The GS1501 provides status signals to indicate the current content level of the internal FIFO buffers, as described in section 3.1.

3.3.1 FIFO Status Bits

The device provides a status output signal FF_STA[2:0] that indicates the state of the current content level of the internal FIFOs. FF_STA[2:0] outputs 110, should the user supplied ANC data have completely filled the internal FIFO buffer. It is noted that once the internal FIFO is full, any attempt to write data into the FIFO will cause the FIFO to overrun. The device flags this overrun state by setting FF_STA[2:0]=111. FF_STA[2:0] outputs 001, should all ANC data in the FIFO be extracted and inserted into the video stream and the internal FIFO becomes empty. It is noted that once the internal FIFO is empty, any attempt to read data from the FIFO will cause the FIFO to underrun. The device flags this underrun state by setting FF_STA[2:0]=000 and no data is inserted into the video stream. When ANC_Y/$\overline{C}$ is high, FF_STA indicates the status of the LUMA FIFO buffer and when ANC_Y/$\overline{C}$ is low, FF_STA indicates the status of the CHROMA FIFO buffer.

It is important that the FIFO status flags are as up-to-date as possible. Therefore, certain FIFO status flags are synchronized with respect to W_CLK, and others are synchronized with respect to PCLK_IN. During a write cycle, status flags controlled by W_CLK experience a three-cycle latency with respect to W_CLK. During a read cycle, status flags controlled by PCLK_IN experience a three-cycle latency with respect to PCLK_IN. This information is summarized in Table 1, and illustrated in Figures 5 to 14.

NOTE: If a simultaneous FIFO read and write operation is to be performed, the FF_STA[2:0] outputs should not be used as they may indicate incorrect FIFO status.

3.3.2 FIFO Write Control

The FIFO control signal $\overline{WEN}$ is the write enable signal used to enable the loading of ANC data into the internal FIFO by the user through the FIFO interface. Note that the device only allows loading to one of the two internal FIFO buffers through the FIFO interface at a time. When ANC_Y/$\overline{C}$ is high, the LUMA FIFO may be loaded. When ANC_Y/$\overline{C}$ is low, the CHROMA FIFO may be loaded.

When the internal FIFO is not in the full or overrun states, it is ready to accept ANC data. This should prompt the user to supply up to 1024 data words to the FIFO by writing them through the FIFO interface. Upon seeing a rising edge on W_CLK, the device will accept the word being presented on ANC_IN[9:0] into the selected FIFO. Each time W_CLK is toggled, the internal write address pointer (LUMA or CHROMA) is incremented while $\overline{WEN}$ is low. If $\overline{WEN}$ is high, the write address pointer is not incremented and writing to the FIFO is disabled.

3.3.4 FIFO Read Control

The FIFO control signal $\overline{REN}$ is the read enable signal used to enable ANC data insertion from the internal LUMA or CHROMA FIFO buffer into its corresponding video stream, depending on the value of ANC_Y/$\overline{C}$. The read address pointer increments with the internal clock at the video data rate while $\overline{REN}$ is low. If $\overline{REN}$ is high, the read address pointer will not increment. Both address pointers for read and write can be reset to their starting positions by toggling the FIFO reset signal $\overline{FFRST}$ from high to low.

The device will insert the ANC data into the video streams whenever data is present in the respective FIFO buffer and the control signal $\overline{REN}$ is low. ANC data will be extracted from the internal FIFO buffer and inserted into the video stream until it is completely empty. When all words have been read from the FIFO, the FF_STA[2:0] signal will be set to 001.

3.3.4 ANC/Data Insertion

In many cases, the user only wants to insert ANC data into the HANC region. In order to make this frequently used mode easy, the device provides an automated insertion mode. When the control signal FM_I/$\overline{E}$ is high, the FIFO control signals $\overline{FFRST}$ and $\overline{REN}$ cannot be used for the purpose described above. In this mode of operation, the device generates these reset and enable signals internally, which allows an automated insertion of ANC data into the HANC region of the incoming LUMA or CHROMA data streams. The user still needs to supply a proper $\overline{WEN}$ signal to enable the loading of ANC data into the FIFO. Up to 1024 ANC data words of each of the LUMA or CHROMA FIFO(s)

may be inserted during the HANC period. These data should be supplied into the FIFO during the active video period. Once all words have been read from the FIFO, the FF_STA signal will be set to 001.

3.3.5 FIFO External Reset

In external FIFO control mode, the internal FIFO address pointers are reset to zero (0) using $\overline{\text{FFRST}}$. A recommended external reset process is shown in Figure 15.

TABLE 1: FIFO Status Indicator

FF_STA[2:0]	DESCRIPTION	SYNCHRONIZED TO
000	ERROR flag; FIFO is under run	PCLK_IN
001	FIFO is empty	PCLK_IN
010	FIFO is almost empty; ≤ 32 bytes filled	PCLK_IN
011	FIFO is ready	-
100	FIFO is half full	W_CLK
101	FIFO is almost full; ≥ 992 bytes filled	W_CLK
110	FIFO is full	W_CLK
111	ERROR flag; FIFO is over run	W_CLK

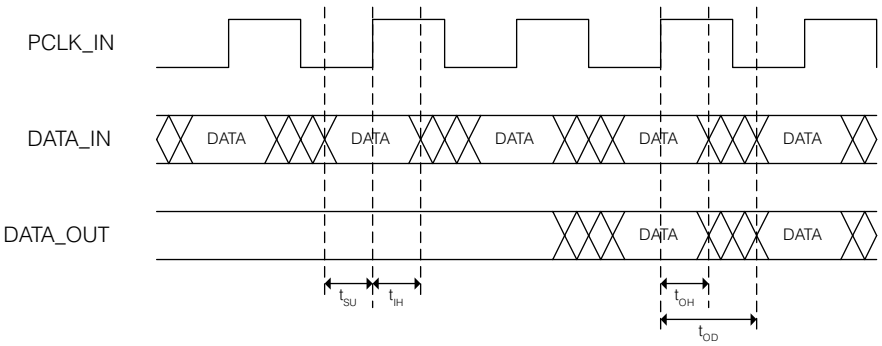


Fig. 1 Synchronous I/O Time

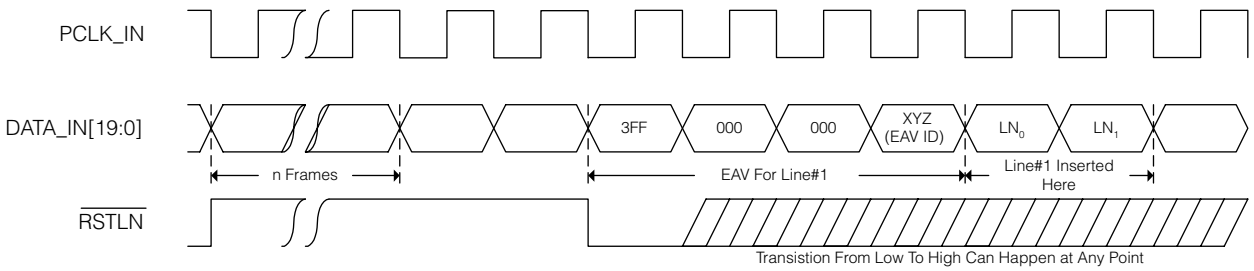


Fig. 2 $\overline{\text{RSTLN}}$ Timing

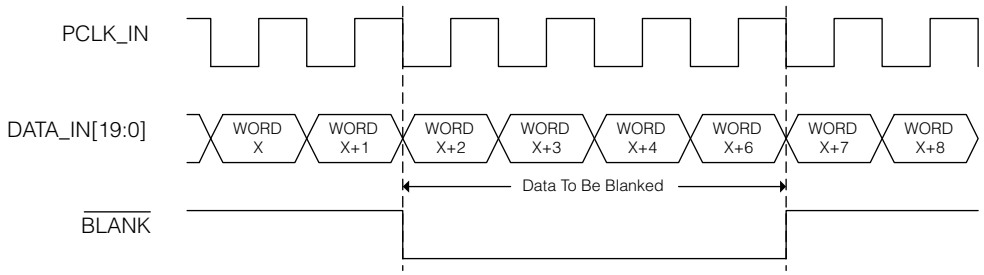


Fig. 3 Timing of Dynamic Data Blanking

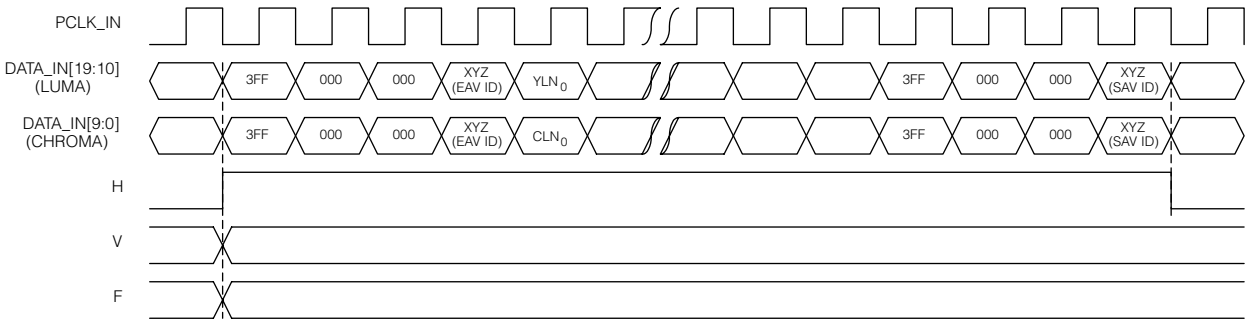
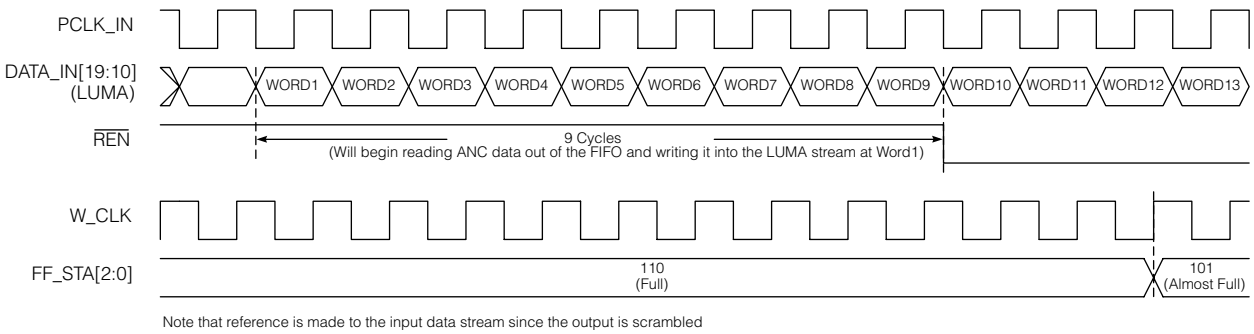


Fig. 4 HVF Input Timing



Note that reference is made to the input data stream since the output is scrambled

Fig. 5 FIFO Full to Almost Full Read Timing

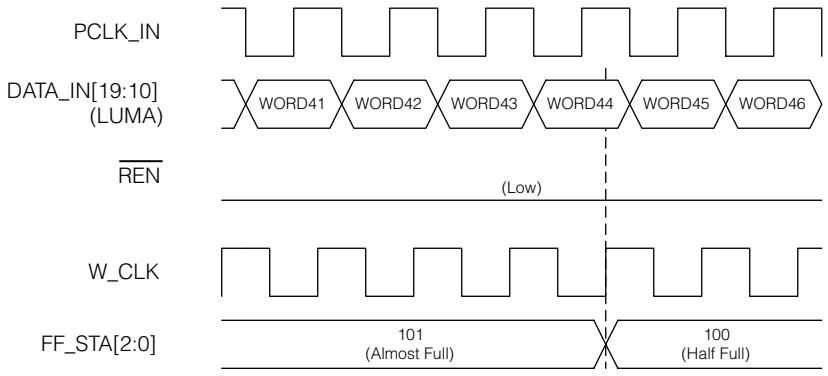


Fig. 6 FIFO Almost Full to Half Full Read Timing

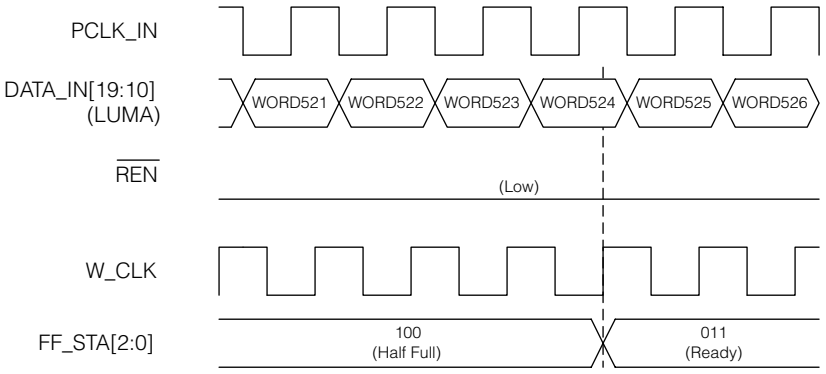


Fig. 7 FIFO Half Full to Ready Read Timing

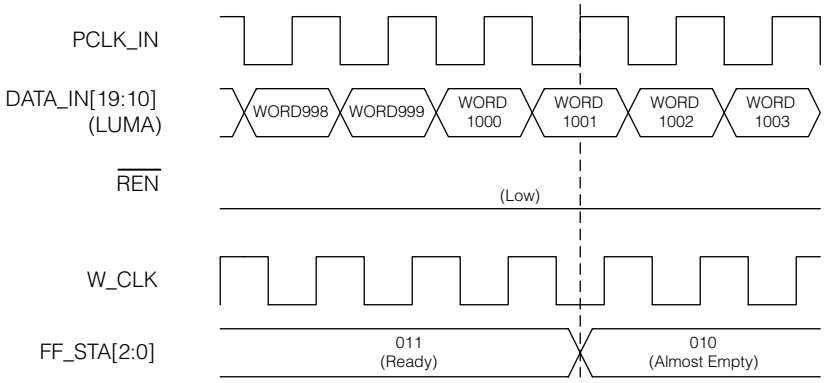


Fig. 8 FIFO Ready to Almost Empty Read Timing

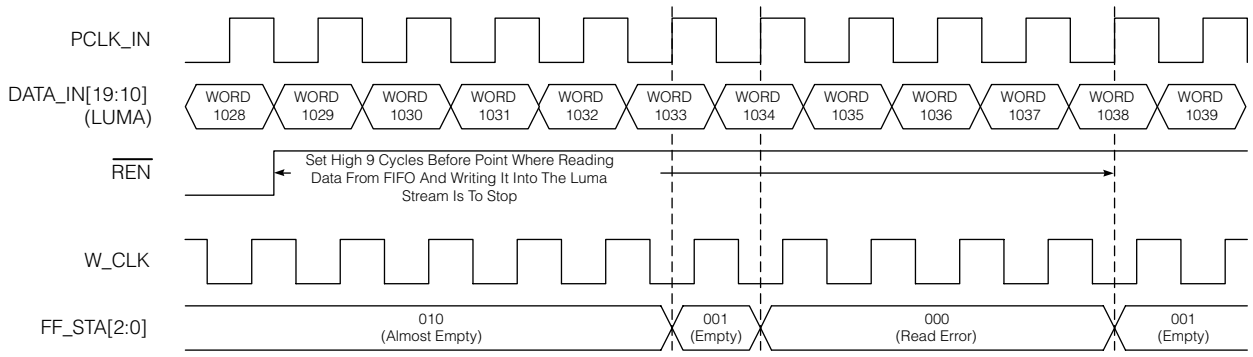


Fig. 9 FIFO Almost Empty to Empty to Read Error Timing

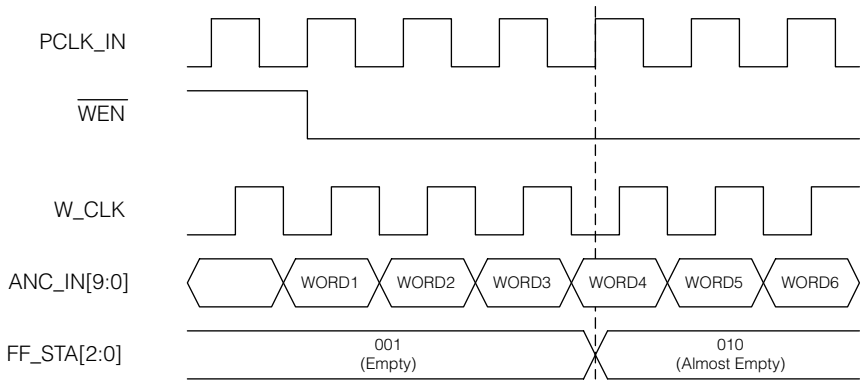


Fig. 10 FIFO Empty to Almost Empty Write Timing

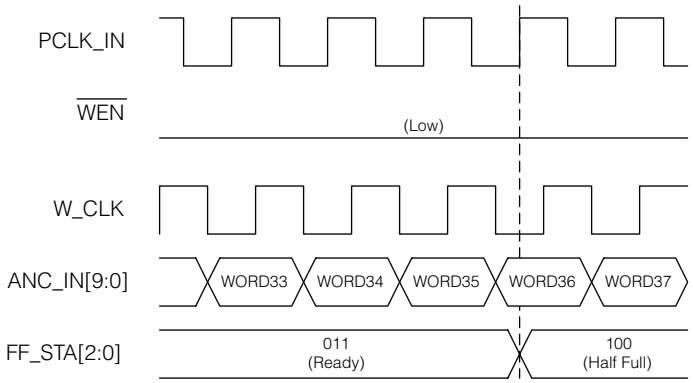


Fig. 11 FIFO Ready to Half Full Write Timing

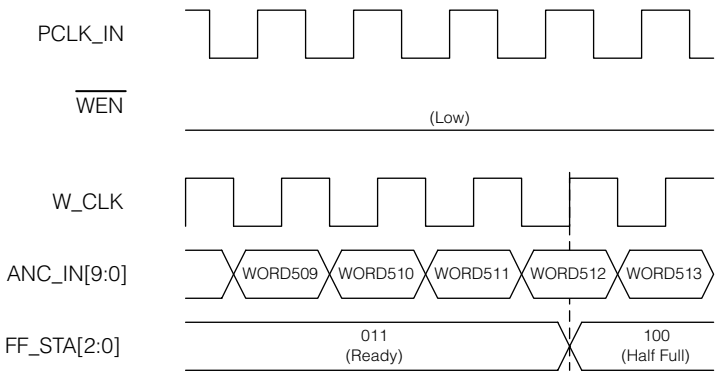


Fig. 12 FIFO Ready to Half Full Write Timing

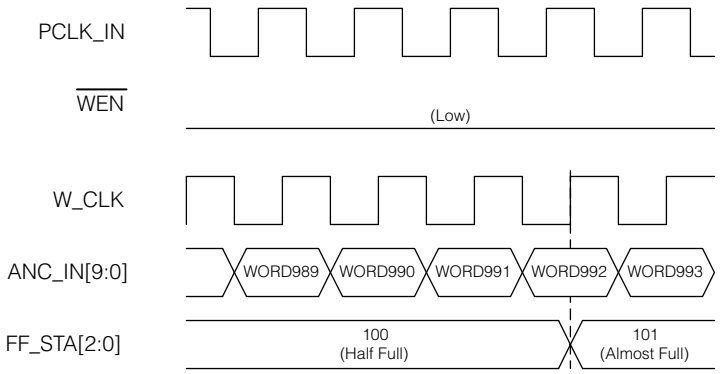


Fig. 13 FIFO Half Full to Almost Full Write Timing

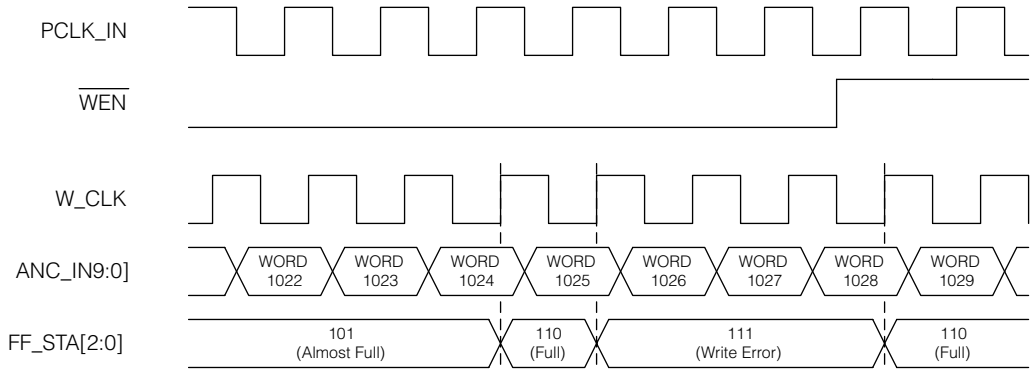


Fig. 14 FIFO Almost Full to Full to Write Error Timing

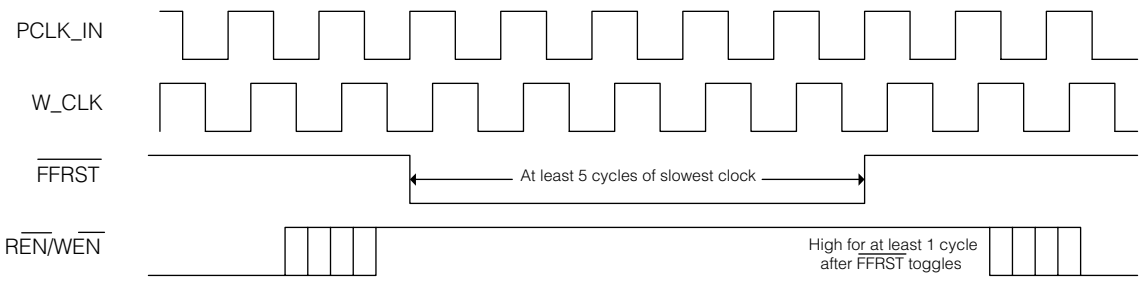


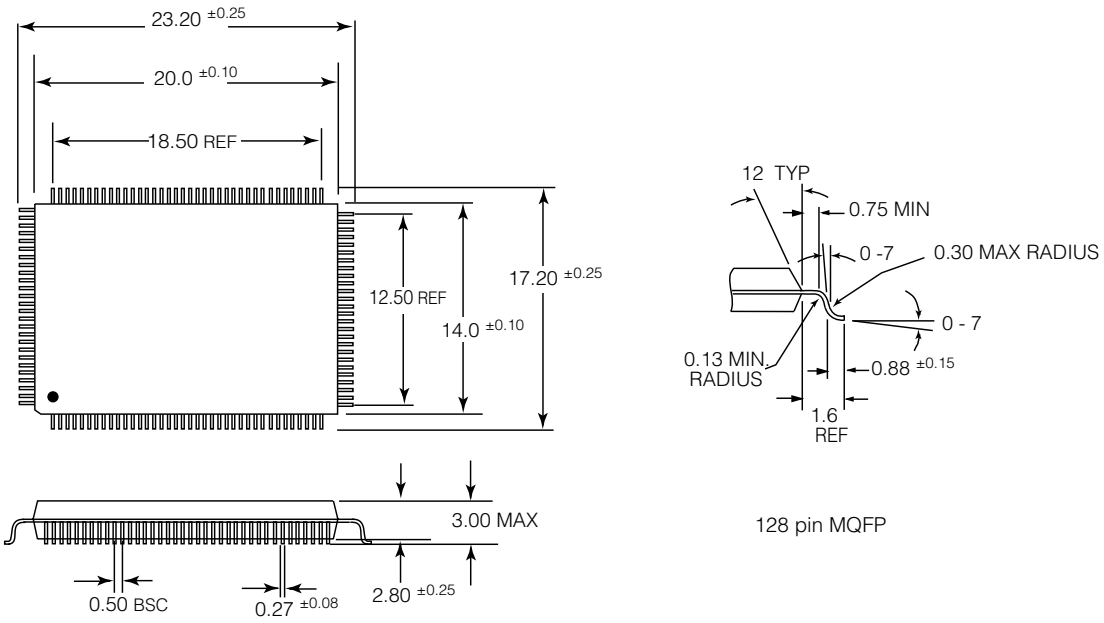
Fig. 15 Recommended External FIFO Reset Process

4. REFERENCES

Compliant with SMPTE 292M.

5. PACKAGE & ORDERING INFORMATION

5.1 PACKAGE DIMENSIONS



128 pin MQFP

5.2 ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE RANGE
GS1501-CQR	128 pin MQFP	0°C to 70°C

CAUTION
ELECTROSTATIC
SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

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DATA SHEET
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