TOSHIBA INSULATED GATE BIPOLAR TRANSISTOR SILICON N CHANNEL IGBT

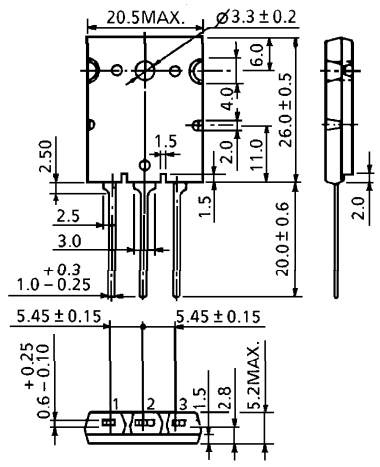
GT50G321

THE 4TH GENERATION

CURRENT RESONANCE INVERTER SWITCHING APPLICATIONS

- FRD Included Between Emitter and Collector
- Enhancement-Mode
- High Speed : $t_f = 0.30\ \mu s$ (Typ.) ($I_C = 60$ A)
- Low Saturation Voltage : $V_{CE\ (sat)} = 1.8$ V (Typ.) ($I_C = 60$ A)

Unit in mm



1. GATE
2. COLLECTOR (HEAT SINK)
3. EMITTER

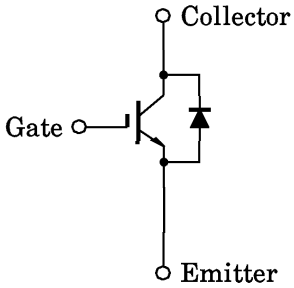
JEDEC	—
JEITA	—
TOSHIBA	2-21F2C

Weight : 9.75 g

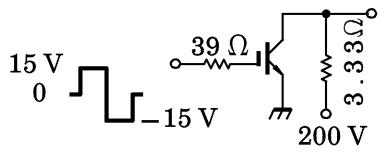
MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Collector-Emitter Voltage		V_{CES}	400	V
Gate-Emitter Voltage		V_{GES}	±25	V
Collector Current	DC	I_C	50	A
	1 ms	I_{CP}	100	
Emitter-Collector Foward Current	DC	I_F	15	A
	1 ms	I_{FP}	30	
Collector Power Dissipation (Tc = 25°C)		P_C	130	W
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_{stg}	−55~150	°C

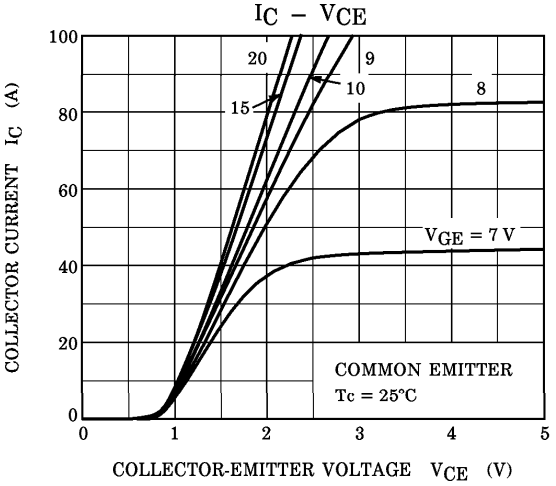
EQUIVALENT CIRCUIT



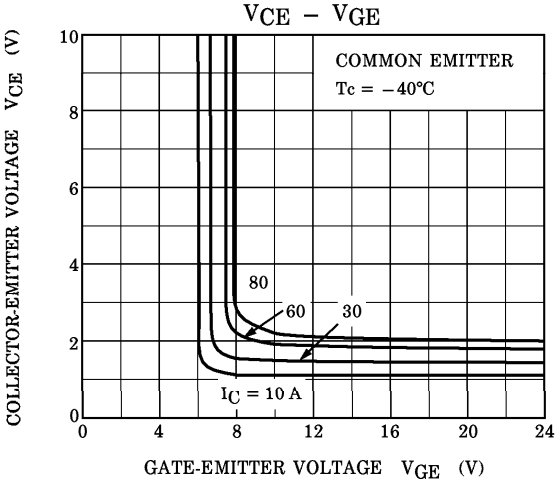
ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP	MAX.	UNIT
Gate Leakage Current		I_{GES}	V_{GE} = ±25 V, V_{CE} = 0	—	—	±500	nA
Collector Cut-off Current		I_{CES}	V_{CE} = 400 V, V_{GE} = 0	—	—	1.0	mA
Gate-Emitter Cut-off Voltage		$V_{GE\ (OFF)}$	I_C = 60 mA, V_{CE} = 5 V	3.0	—	6.0	V
Collector-Emitter Saturation Voltage		$V_{CE\ (sat)}$	I_C = 60 A, V_{GE} = 15 V	—	1.8	2.5	V
Input Capacitance		C_{ies}	V_{CE} = 10 V, V_{GE} = 0, f = 1 MHz	—	3900	—	pF
Switching Time	Rise Time	t_r		—	0.33	—	μs
	Turn-on Time	t_{on}		—	0.43	—	
	Fall Time	t_f		—	0.30	0.40	
	Turn-off Time	t_{off}		—	0.54	—	
Forward Voltage		V_F	I_F = 15 A, V_{GE} = 0	—	—	2.0	V
Reverse Recovery Time		t_{rr}	I_F = 15 A, V_{GE} = 0 di / dt = −100 A / μs	—	—	0.2	μs
Thermal Resistance		$R_{th\ (j\text{-}c)}$	IGBT	—	—	0.96	°C / W
Thermal Resistance		$R_{th\ (j\text{-}c)}$	Diode	—	—	2.08	°C / W

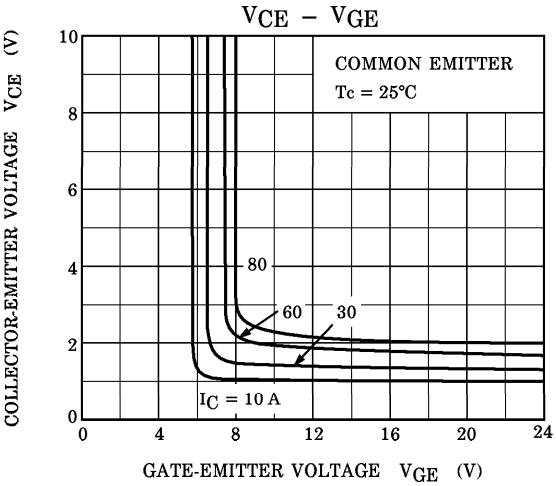
I_C – V_{CE}



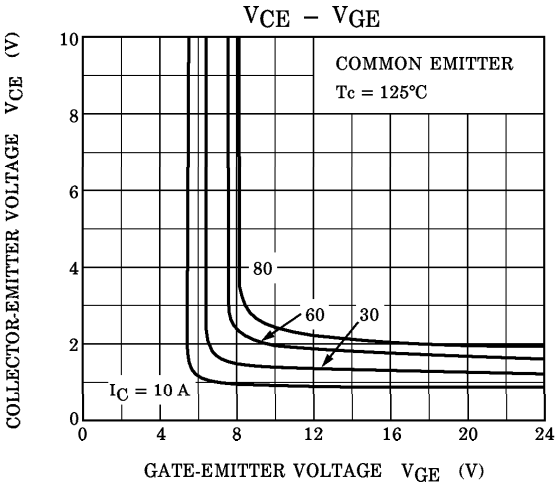
V_{CE} – V_{GE}



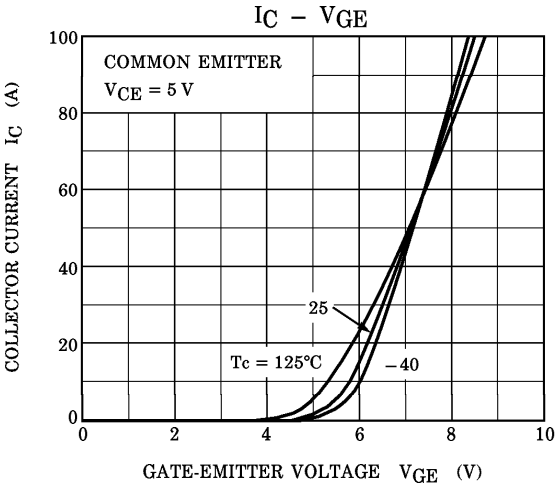
V_{CE} – V_{GE}



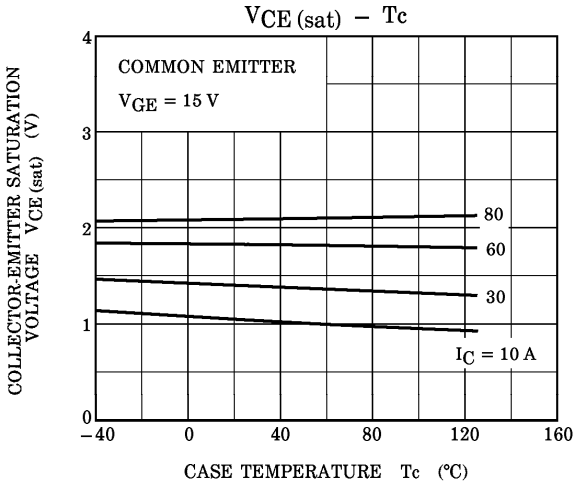
V_{CE} – V_{GE}



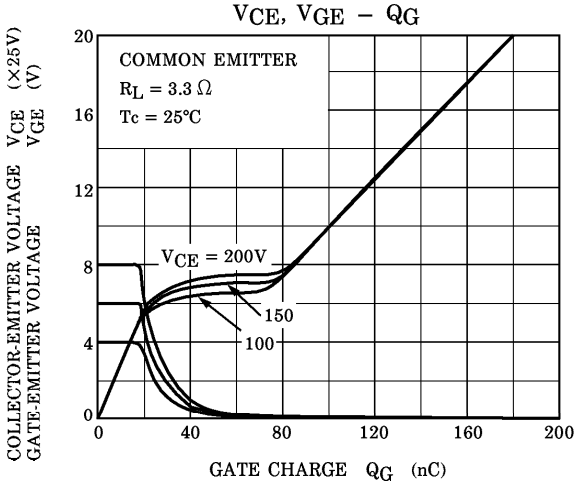
I_C – V_{GE}



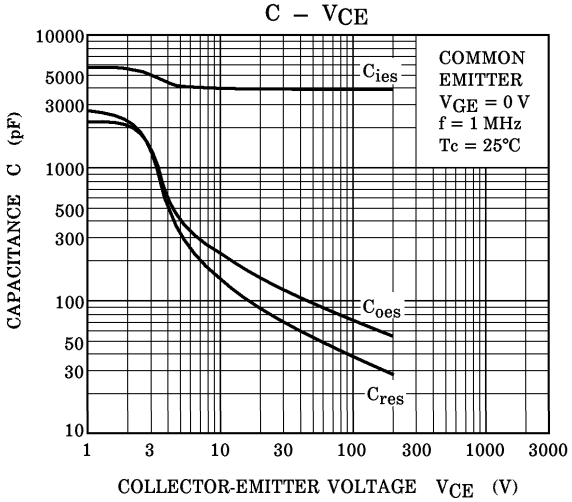
$V_{CE\,(sat)}$ – Tc



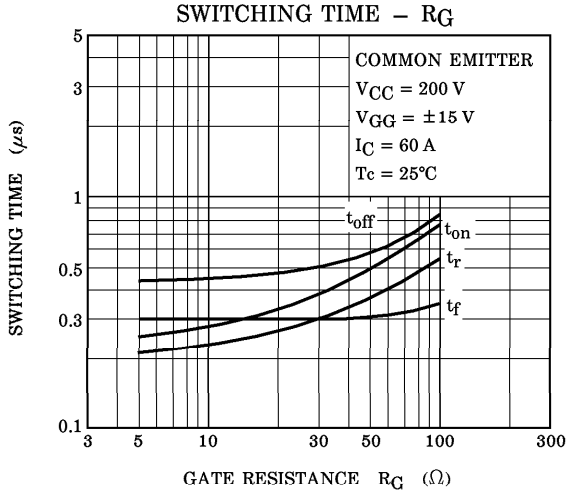
V_{CE}, V_{GE} – Q_G



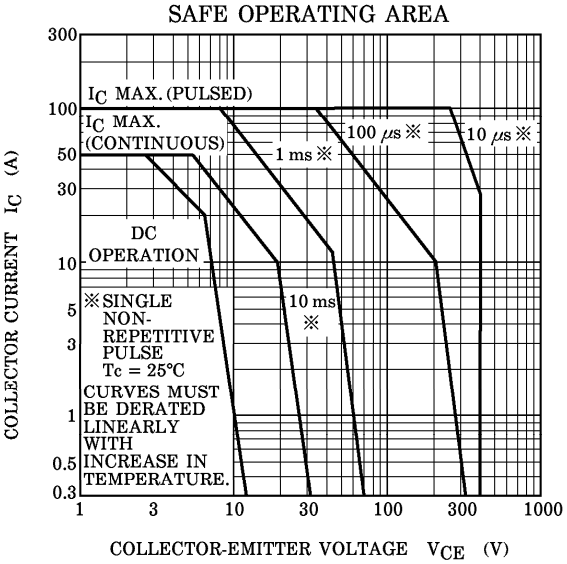
C – V_{CE}



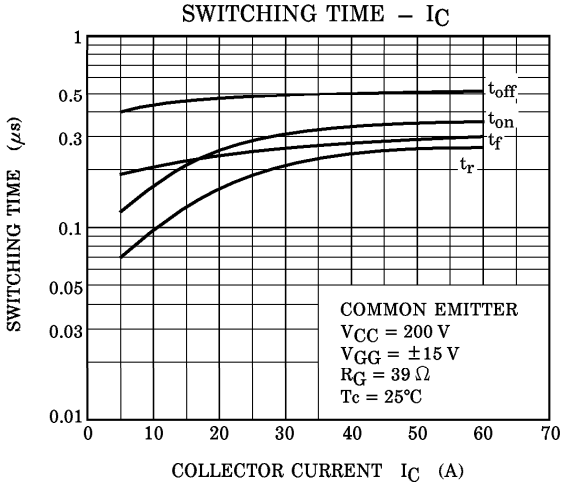
SWITCHING TIME – R_G



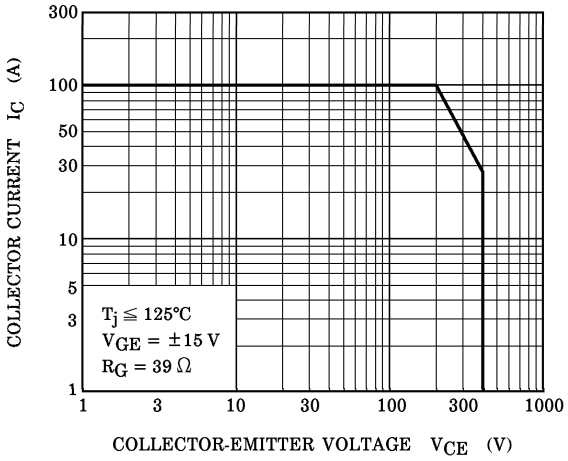
SAFE OPERATING AREA



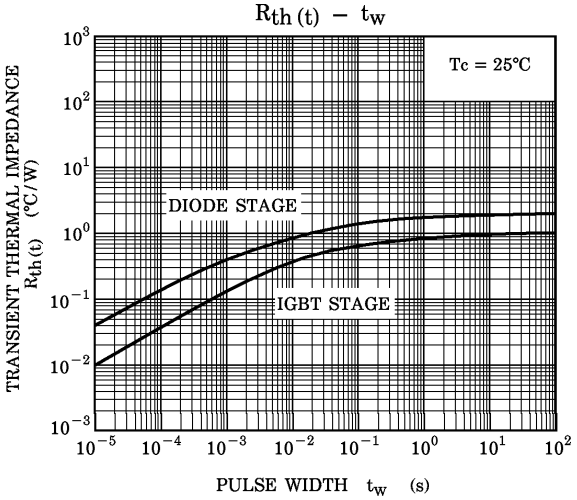
SWITCHING TIME – I_C



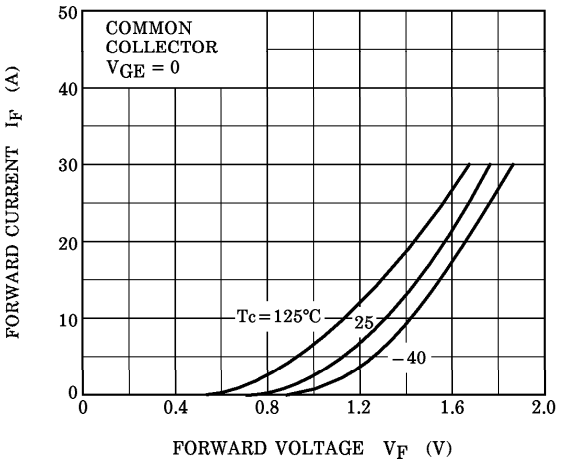
REVERSE BIAS SOA



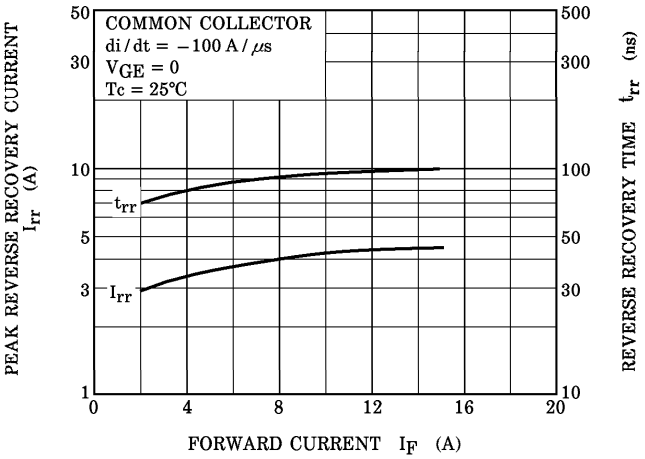
$R_{th\,(t)} - t_w$



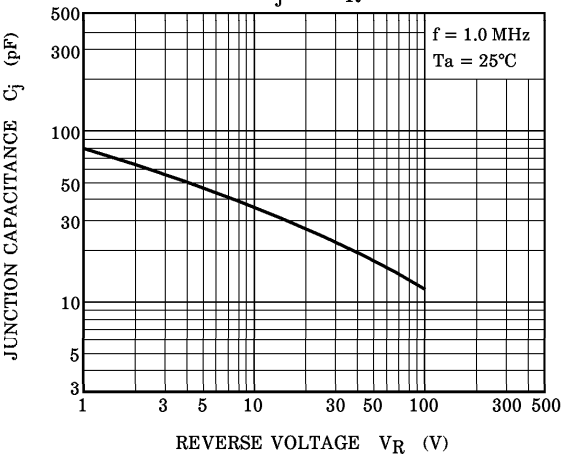
$I_F - V_F$



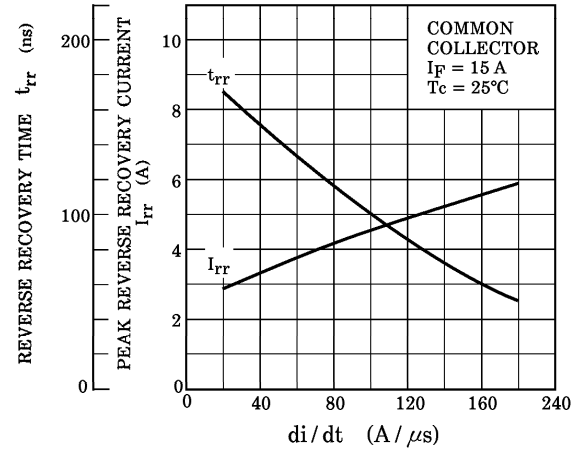
I_{rr}, t_{rr} − I_F



$C_j - V_R$



I_{rr}, t_{rr} − di/dt



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