DATA SHEET

GTL16612

18-bit GTL/GTL$^+$ to LVTTL/TTL bidirectional universal translator (3-State)

Product data
Supersedes data of 2000 Jun 19

2002 Dec 13

Philips Semiconductors

PHILIPS

18-bit GTL/GTL+ to LVTTL/TTL bidirectional universal translator (3-State)

GTL16612

FEATURES

- 18-bit bidirectional bus interface
- Translates between GTL/GTL+ logic levels (B ports) and LVTTL/TTL logic levels (A ports)
- 5 V I/O tolerant on the LVTTL/TTL side (A ports)
- No bus current loading when LVTTL/TTL output is tied to 5 V bus
- 3-State buffers
- Output capability: +64 mA/-32 mA on the LVTTL/TTL side (A ports); +40 mA on the GTL/GTL+ side (B ports)
- TTL input levels on control pins
- Power-up reset
- Power-up 3-State
- Positive edge triggered clock inputs
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101

DESCRIPTION

The GTL16612 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V with I/O compatibility up to 5 V.

This device is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch enable (LEAB and LEBA), and clock (CPAB and CPBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is High. When LEAB is Low, the A data is latched if CPAB is held at a High or Low logic level. If LEAB is Low, the A-bus data is stored in the latch/flip-flop on the Low-to-High transition of CPAB. When $\overline{OEAB}$ is Low, the outputs are active. When $\overline{OEAB}$ is High, the outputs are in the high-impedance state. The clocks can be controlled with the clock-enable inputs ($\overline{CEBA}$/$\overline{CEAB}$).

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{OEBA}$, LEBA and CPBA.

QUICK REFERENCE DATA

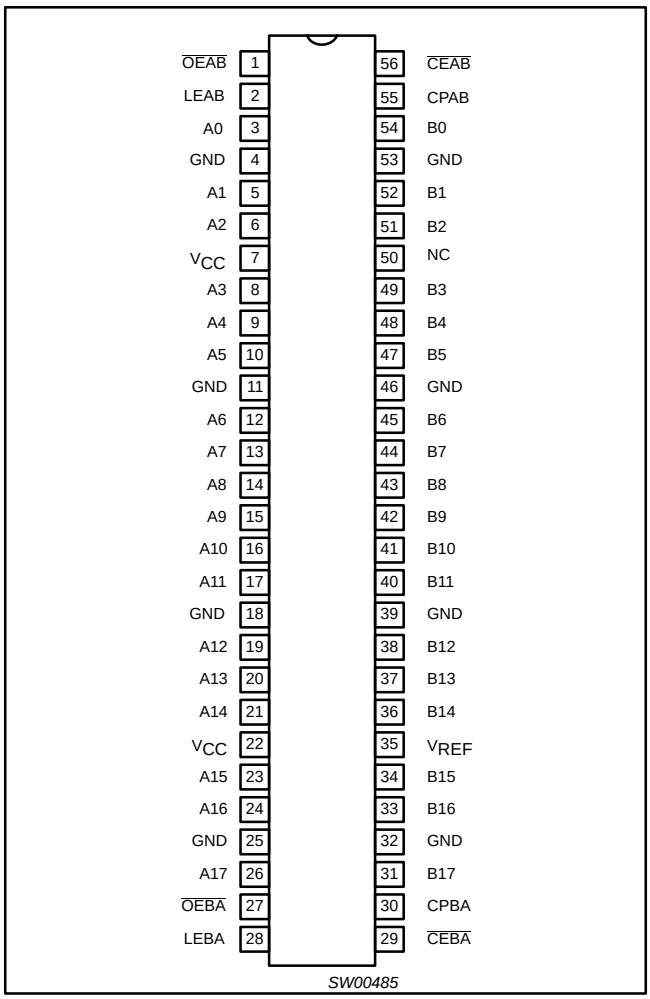
SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25 °C	TYPICAL	UNIT
			3.3 V	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50 pF	1.9	ns
C_{IN}	Input capacitance (Control pins)	V_I = 0 V or V_{CC}	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0 V or V_{CC}	8	pF
I_{CCZ}	Total supply current	Outputs disabled	12	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
56-Pin Plastic SSOP	-40 to +85 °C	GTL16612DL	SOT371-1
56-Pin Plastic TSSOP	-40 to +85 °C	GTL16612DGG	SOT364-1

Standard packing quantities and other packaging data is available at www.philipslogic.com/packaging.

PIN CONFIGURATION

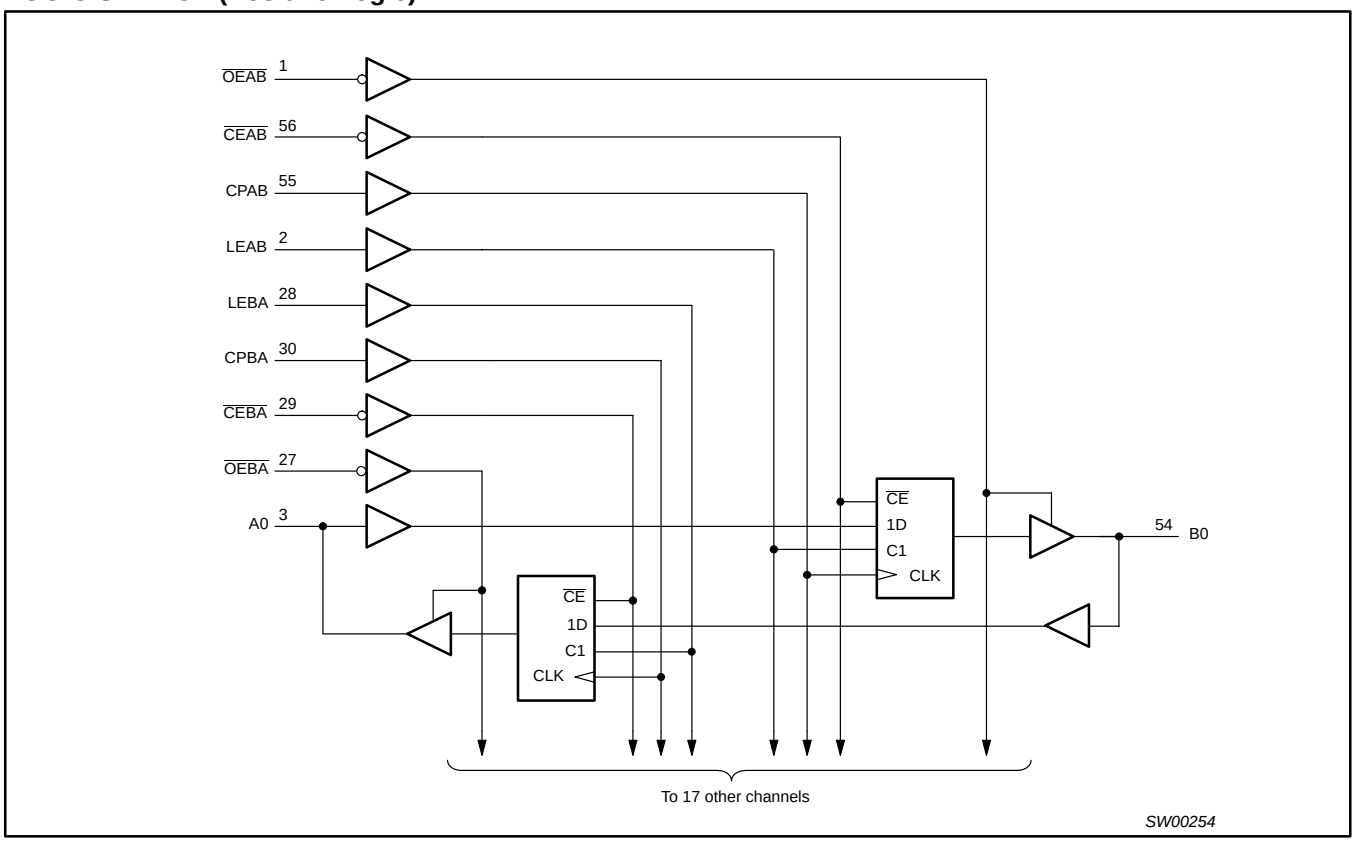


SW00485

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 27	$\overline{OEAB}$/$\overline{OEBA}$	A-to-B/ B-to-A Output enable input (active Low)
29, 56	$\overline{CEBA}$/$\overline{CEAB}$	B-to-A/A-to-B clock enable
2, 28	LEAB/LEBA	A-to-B/B-to-A Latch enable input
55,30	CPAB/CPBA	A-to-B/B-to-A Clock input (active rising edge)
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0-A17	Data inputs/outputs (A side)
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0-B17	Data inputs/outputs (B side)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0 V)
7, 22	V_{CC}	Positive supply voltage
35	V_{REF}	GTL reference voltage
50	NC	No connection

LOGIC SYMBOL (Positive Logic)



FUNCTION TABLE

INPUTS					OUTPUT B
$\overline{CEAB}$[1]	$\overline{OEAB}$[1]	LEAB[1]	CPAB[1]	A	
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_O[2]
H	L	L	X	X	B_O[2]
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	H	X	B_O[2]
L	L	L	L	X	B_O[3]

X = Don't care
H = High voltage level
L = Low voltage level
↑ = Low to High
Z = High impedance "off" state
1. A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, CPBA, and $\overline{CEBA}$.
2. Output level before the indicated steady-state input conditions were established.
3. Output level before the indicated steady-state input conditions were established, provided that CPAB was Low before LEAB went Low.

ABSOLUTE MAXIMUM RATINGS [1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage[3]	A port	-0.5 to +7.0	V
		B port	-0.5 to +4.6	
I_{OK}	DC output diode current	$V_O < 0$; A port	-50	mA
V_O	DC output voltage[3]	Output in Off or High state; A port	-0.5 to +7.0	V
		Output in Off or High state; B port	-0.5 to +4.6	V
I_{OL}	Current into any output in the LOW state	A port	128	mA
		B port	80	mA
I_{OH}	Current into any output in the HIGH state	A port	-64	mA
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	3.3 V RANGE LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		3.0	3.6	V
V_{TT}	Termination voltage	GTL	1.14	1.26	V
		GTL+	1.35	1.65	
V_{REF}	GTL reference voltage	GTL	0.74	0.87	V
		GTL+	0.9	1.10	
V_I	Input voltage	B port	0	V_{TT}	V
		Except B port	0	5.5	
V_{IH}	HIGH-level input voltage	B port	V_{REF}+50 mV		V
		Except B port	2.0		
V_{IL}	LOW-level input voltage	B port		V_{REF}-50 mV	V
		Except A port		0.8	
I_{OH}	HIGH-level output current	A port		-32	mA
I_{OL}	LOW-level output current	B port		40	mA
		A port		64	
T_{amb}	Operating free-air temperature range		-40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3 V ±0.3 V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40 to +85 °C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0 V; I_{IK} = -18 mA			-0.85	-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6 V; I_{OH} = -100 µA	A port	V_{CC}-0.2	V_{CC}		V
		V_{CC} = 3.0 V; I_{OH} = -32 mA		2.0	2.3		
V_{OL}	Low-level output voltage	V_{CC} = 3.0 V; I_{OL} = 100 µA	A port		0.07	0.2	V
		V_{CC} = 3.0 V; I_{OL} = 16 mA			0.25	0.4	
		V_{CC} = 3.0 V; I_{OL} = 32 mA			0.3	0.5	
		V_{CC} = 3.0 V; I_{OL} = 64 mA			0.4	0.55	
		V_{CC} = 3.0 V; I_{OL} = 40 mA	B port		0.4	0.5	V
I_I	Input leakage current	V_{CC} = 3.6 V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6 V; V_I = 5.5 V			0.1	10	
		V_{CC} = 3.6 V; V_I = 5.5 V	I/O Data pins[4] A port		0.1	20	µA
		V_{CC} = 3.6 V; V_I = V_{CC}			0.5	10	
		V_{CC} = 3.6 V; V_I = 0			0.1	-5	
		V_{CC} = 3.6 V; V_I = V_{TT} or GND	B port			±5	µA
I_{OFF}	Output off current	V_{CC} = 0 V; V_I or V_O = 0 to 4.5 V			0.1	±100	µA
I_{HOLD}	Bus Hold current, A outputs	V_{CC} = 3 V; V_I = 0.8 V		75	130		µA
		V_{CC} = 3 V; V_I = 2.0 V		-75	-140		
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5 V; V_{CC} = 3.0 V	A port		10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2 V; V_O = 0.5 V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$ = Don't care			1.0	±100	µA
I_{CCH}	A-Port	V_{CC} = 3.6 V	Outputs high	V_I = GND or V_{CC}, I_O = 0		5.0	9.0	mA
I_{CCL}			Outputs low			10.5	18.5	
I_{CCZ}[5]			Disabled			6.0	11.5	
I_{CCH}	B-Port		Outputs high			9.7	17.5	
I_{CCL}			Outputs low			7.0	12.0	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3 V to 3.6 V; One input at V_{CC}-0.6 V, Other inputs at V_{CC} or GND			0.04	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.
2. This is the increase in supply current for each LVTTL input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 msec. From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.

AC CHARACTERISTICS (A PORT)

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF; R_L = 500 Ω; T_{amb} = -40 to +85 °C.

GTL16612 An Port			GTL			GTL+			UNIT
			V_{CC} = 3.3 V ±0.3 V			V_{CC} = 3.3 V ±0.3 V			
			V_{REF} = 0.8 V			V_{REF} = 1.0 V			
SYMBOL	PARAMETER	WAVEFORM	MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
t_{PLH}	Bn to An	2	1.6	3.0	5.0	1.6	3.0	5.0	ns
t_{PHL}	Bn to An	2	3.0	4.9	6.3	3.0	4.9	6.3	ns
t_{PLH}	LEBA to An	3	1.6	2.7	4.2	1.6	2.7	4.2	ns
t_{PHL}	LEBA to An	3	1.6	2.8	4.3	1.6	2.8	4.3	ns
t_{PLH}	CPBA to An	1	1.9	3.4	4.7	1.9	3.4	4.7	ns
t_{PHL}	CPBA to An	1	1.8	3.8	5.2	1.8	3.8	5.2	ns
t_{PZH}	$\overline{OEBA}$ to An	5	1.5	2.6	4.2	1.5	2.6	4.2	ns
t_{PHZ}	$\overline{OEBA}$ to An	5	1.4	2.9	4.8	1.4	2.9	4.8	ns
t_{PZL}	$\overline{OEBA}$ to An	6	1.3	2.4	3.8	1.3	2.4	3.8	ns
t_{PLZ}	$\overline{OEBA}$ to An	6	1.2	2.2	3.5	1.2	2.2	3.5	ns

NOTE:
1. Typical values are at V_{CC} = 3.3 V, T_{amb} = +25 °C.

AC CHARACTERISTICS (B PORT)

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 30 pF; R_L = 25 Ω; T_{amb} = -40 to +85 °C.

GTL16612 Bn Port			GTL			GTL+			UNIT
			V_{CC} = 3.3 V ±0.3 V			V_{CC} = 3.3 V ±0.3 V			
			V_{REF} = 0.8 V			V_{REF} = 1.0 V			
SYMBOL	PARAMETER	WAVEFORM	MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
t_{PLH}	An to Bn	2	1.4	2.4	3.7	1.3	2.4	3.7	ns
t_{PHL}	An to Bn	2	1.3	2.5	4.0	1.4	2.6	4.2	ns
t_{PLH}	LEAB to Bn	3	1.7	3.0	4.4	1.8	3.0	4.6	ns
t_{PHL}	LEAB to Bn	3	2.1	3.5	5.4	2.3	3.6	5.5	ns
t_{PLH}	CPAB to Bn	1	1.8	3.1	4.5	1.9	3.1	4.8	ns
t_{PHL}	CPAB to Bn	1	2.3	3.6	5.4	2.4	3.8	5.8	ns
t_{PLH}	$\overline{OEAB}$ to Bn	7	1.1	2.1	3.3	1.4	2.0	3.5	ns
t_{PHL}	$\overline{OEAB}$ to Bn	7	1.6	2.8	4.4	1.0	2.9	4.5	ns

NOTE:
1. Typical values are at V_{CC} = 3.3 V, T_{amb} = +25 °C.

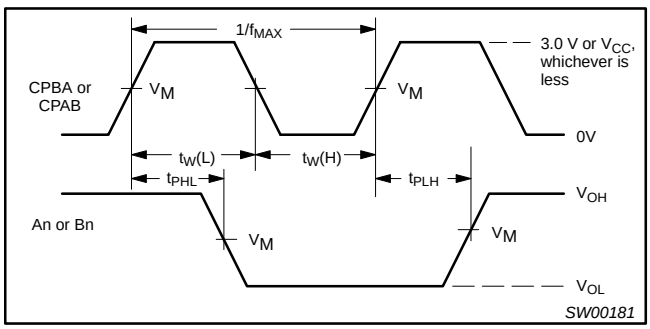
AC SETUP REQUIREMENTS (3.3 V ±0.3 V RANGE)

A Port: GND = 0 V; Input $t_r = t_f$ = 2.5 ns; C_L = 50 pF; R_L = 500 Ω; T_{amb} = -40 to +85 °C; V_{REF} = 0.8 V or 1.0 V.
B Port: GND = 0 V; Input $t_r = t_f$ = 2.5 ns; C_L = 30 pF; R_L = 25 Ω; V_{REF} = 0.8 V or 1.0 V.

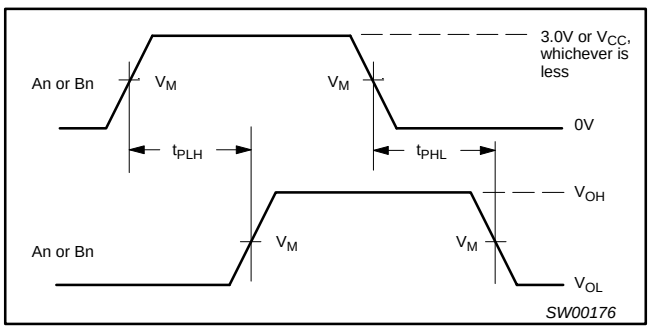
SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V_{CC} = 3.3 V ±0.3 V		
			MIN	MAX	
t_s(H)	Setup time, High or Low Bn to CPBA	4	1.5		ns
t_s(L)		4	1.5		ns
t_s(H)	Setup time, High or Low An to CPAB	4	2.0		ns
t_s(L)		4	3.0		ns
t_h(H)	Hold time, High or Low Bn to CPBA, or An to CPAB	4	1.0		ns
t_h(L)		4	1.0		ns
t_s(H)	Setup time, High or Low Bn to LEBA, or An to LEAB	4	1.0		ns
t_s(L)		4	1.0		ns
t_h(H)	Hold time, High or Low Bn to LEBA, or An to LEAB	4	1.5		ns
t_h(L)		4	1.5		ns
t_s(H)	Setup time, High or Low $\overline{CEAB}$ to CPAB, or $\overline{CEBA}$ to CPBA	4	1.0		ns
t_s(L)		4	1.0		ns
t_h(H)	Hold time, High or Low $\overline{CEAB}$ to CPAB, or $\overline{CEBA}$ to CPBA	4	1.5		ns
t_h(L)		4	1.0		ns
t_w(H)	Pulse width, High or Low CPBA or CPAB	4	2.0		ns
t_w(L)		4	2.0		ns
t_w(H)	Pulse width, High LEBA or LEAB	3	1.5		ns

AC WAVEFORMS

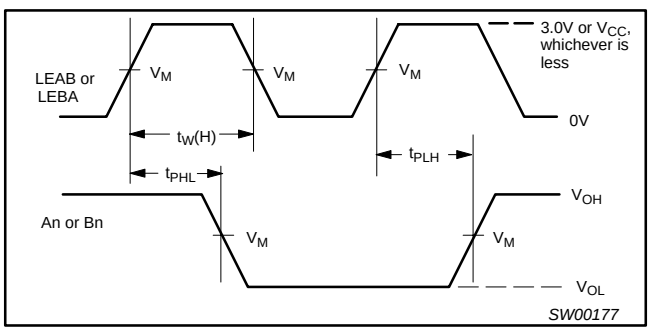
V_M = 1.5 V at $V_{CC} \geq$ 3.0 V. V_M = 1.5 V for A ports and control pins; V_M = 0.8 V for B ports in GTL mode; V_M = 1.0 V for B ports in GTL+ mode.
$V_X = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 3.0 V.
$V_Y = V_{OH}$ - 0.3 V at $V_{CC} \geq$ 3.0 V.



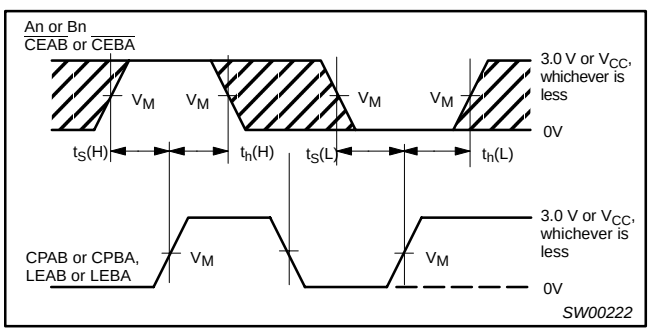
Waveform 1. Propagation delay, clock input to output, clock pulse width, and maximum clock frequency



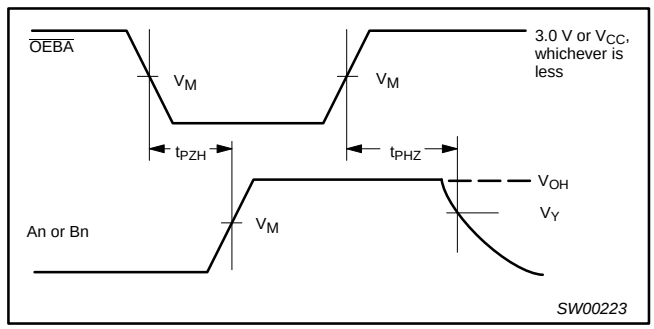
Waveform 2. Propagation delay, transparent mode



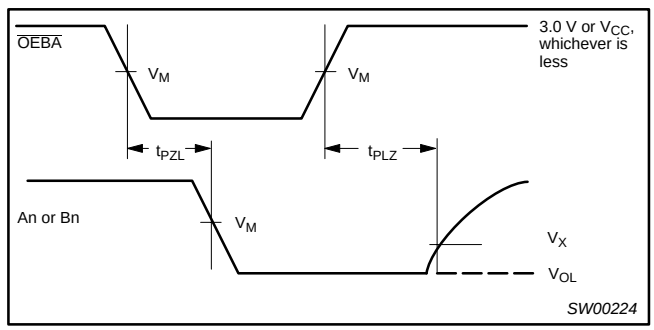
Waveform 3. Propagation delay, enable to output, and enable pulse width



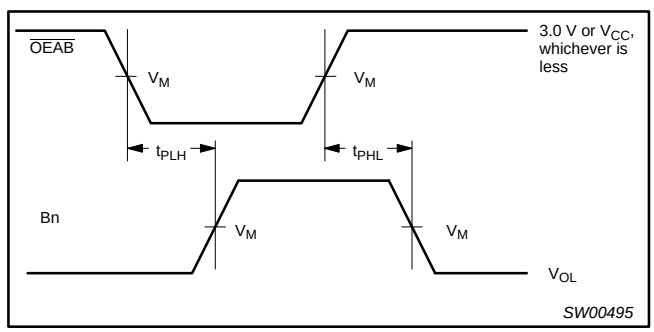
Waveform 4. Data setup and hold times



Waveform 5. 3-State output enable time to high level and output disable time from high level

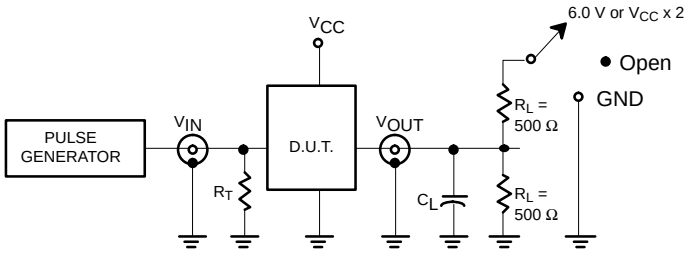


Waveform 6. 3-State output enable time to low level and output disable time from low level

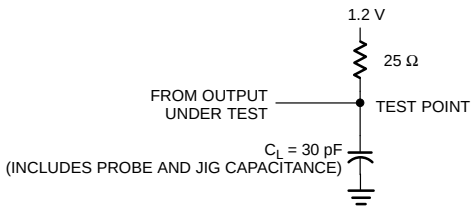


Waveform 7. Output enable time on open collector output with pullup

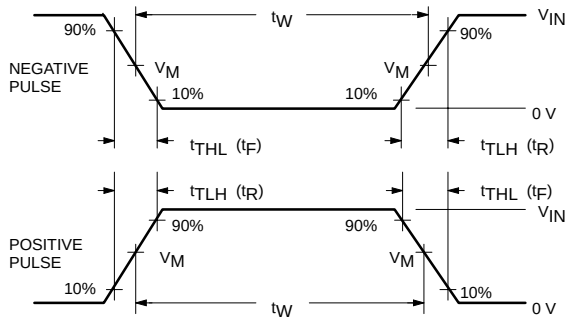
TEST CIRCUIT



Test Circuit for A Outputs



Load Circuit for B Outputs



SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6 V
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

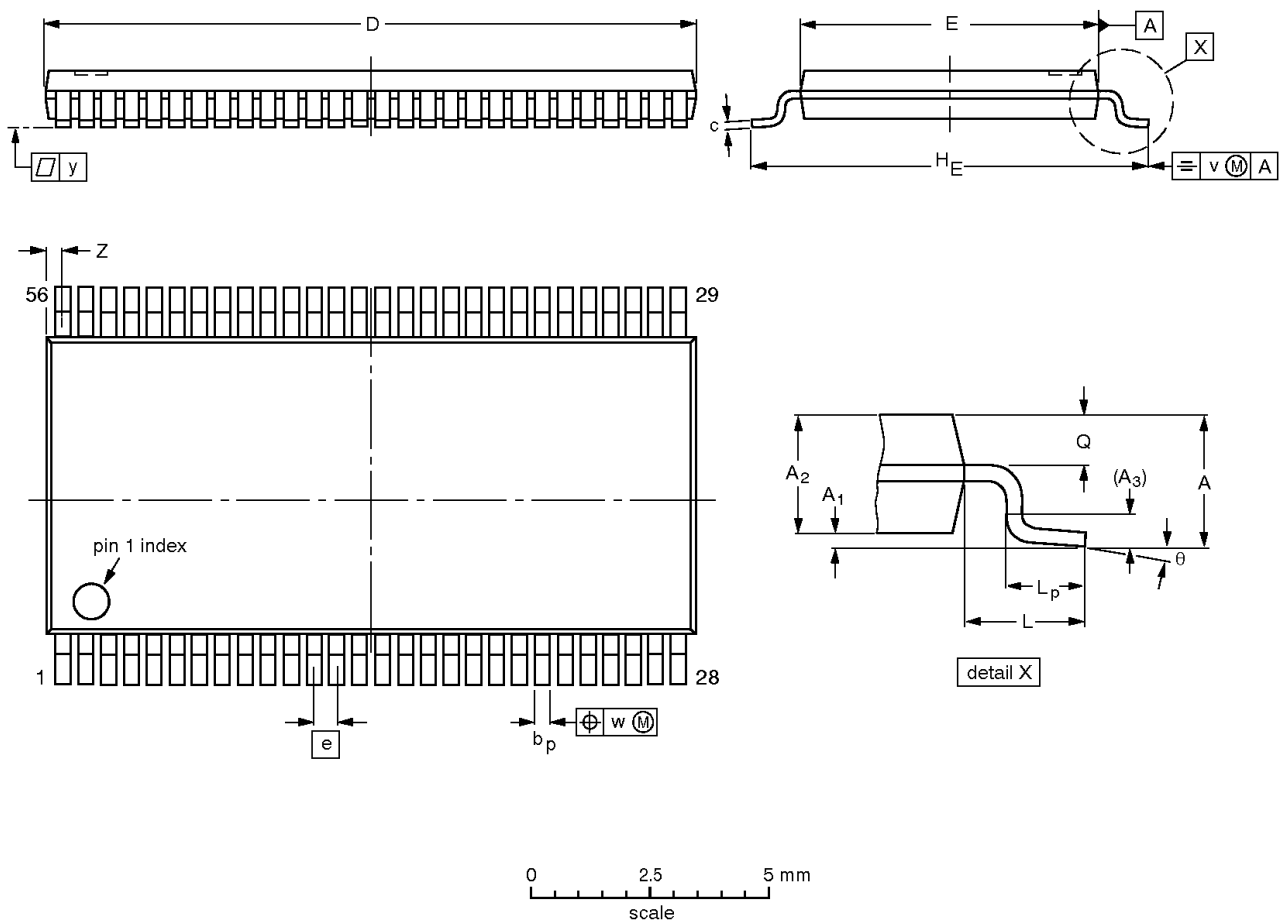
C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74GTL16	3.0 V or V_{CC} whichever is less	≤ 10 MHz	500 ns	≤ 2.5 ns	≤ 2.5 ns

SW00255

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm SOT364-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1.0	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT364-1		MO-153EE					~~93-02-03~~ 95-02-10

REVISION HISTORY

Rev	Date	Description
_4	20021213	Product data (9397 750 10862); ECN 853-2166 29245 of 03 December 2002 Modifications: • New package release.
_3	20000619	Product data (9397 750 07217); ECN 853-2166 23903 of 19 June 2000.

18-bit GTL/GTL+ to LVTTL/TTL bidirectional universal translator (3-State)

GTL16612

Data sheet status

Level	Data sheet status[1]	Product status[2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

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Contact information

For additional information please visit
http://www.semiconductors.philips.com. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to:
sales.addresses@www.semiconductors.philips.com.

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