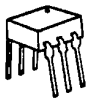
Photon Coupled Isolator H74A1

Ga As Infrared Emitting Diode & NPN Silicon Photo-Transistor

TTL Interface



The GE Solid State H74A1 provides logic to logic optical interfacing of TTL gates with *guaranteed* level compatibility in practical *specified* circuits. The H74A1 is a transistor output photo-coupled isolator specifically designed to eliminate ground loop cross talk and reflection problems when two distinct logic systems are coupled. It is guaranteed to couple 7400, 74H00 and 74S00 logic gates over the full TTL temperature and voltage ranges. This device is mounted in a dual-in-line plastic package. This device is also available in Surface-Mount packaging.

absolute maximum ratings: (25°C) (unless otherwise specified)

INFRARED EMITTING DIODE

Power Dissipation	$T_A = 25°C$	*100	milliwatts
Power Dissipation	$T_C = 25°C$	*100	milliwatts
(T_C indicates collector lead temperature 1/32" from case)			
Forward Current (Continuous)		60	milliamps
Forward Current (Peak)		3	ampere
(Pulse width 1μsec 300 pps)			
Reverse Voltage		6	volts

*Derate 2.2mW/°C above 25°C.

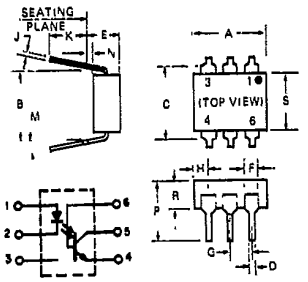
PHOTO-TRANSISTOR

Power Dissipation	$T_A = 25°C$	**300	milliwatts
Power Dissipation	$T_C = 25°C$	***500	milliwatts
(T_C indicates collector lead temperature 1/32" from case)			
V_{CEO}		15	volts
V_{CBO}		15	volts
V_{ECO}		5.5	volts
Collector Current (Continuous)		50	milliamps

**Derate 6.7mW/°C above 25°C.
***Derate 11.1mW/°C above 25°C.

TOTAL DEVICE

Storage Temperature -55 to 150°C
Operating Temperature 0 to 70°C
Lead Soldering Time (at 260°C) 10 seconds
Surge Isolation Voltage (Input to Output)
$3535V_{(peak)}$ $2500V_{(RMS)}$
Steady-State Isolation Voltage (Input to Output)
$3180V_{(peak)}$ $2250V_{(RMS)}$



SYMBOL	MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.	NOTES
A	8.38	8.89	330	.350	
B	7.62 REF		.300 REF.		1
C	–	8.64	–	340	2
D	.406	.508	.016	.020	
E	–	5.08	–	.200	3
F	1.01	1.78	.040	070	
G	2.28	2.80	090	.110	
H	–	2.16	–	.085	4
J	.203	.305	.008	012	
K	2.54	–	.100	–	
M	–	15	–	15	
N	.381	–	.015	–	
P	–	9.53	–	.375	
R	2.92	3.43	.115	.135	
S	6.10	6.86	.240	.270	

NOTES
1 INSTALLED POSITION LEAD CENTERS
2 OVERALL INSTALLED DIMENSION.
3. THESE MEASUREMENTS ARE MADE FROM THE SEATING PLANE.
4. FOUR PLACES.

VDE Approved to 0883/6.80 0110b Certificate # 35025
Covered under U.L. component recognition program, reference file E51868

T-41-83

Electrical Characteristics of H74A1*

*All specifications refer to the following bias configuration (Figure 1) over the full operating temperature (0°C to 70°C) and logic supply voltage range (4.5 to 5.5V_{DC}) unless otherwise noted.

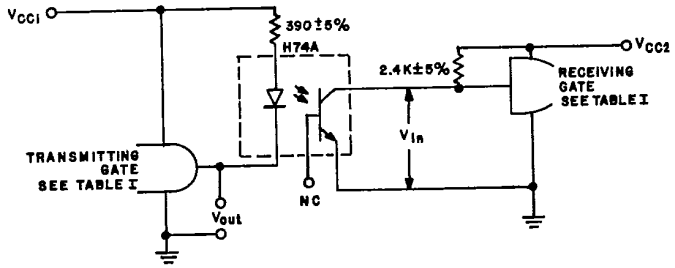


Figure 1. H74A1 BIAS CIRCUIT

V_{in} (0), Receiving Gate For $V_{OUT(0)}$ from Transmitting Gate	0.8	V Max.
V_{in} (1), Receiving Gate for $V_{OUT(1)}$ from Transmitting Gate	2.4	V Min.
t_p (0), Transmitting Gate to Receiving Gate Propagation Time	20	μsec. Typ.
t_p (1), Transmitting Gate to Receiving Gate Propagation Time	4	μsec. Typ.
Isolation Resistance (Input to Output = 500V_{DC})	100	gigaohms Min.
Input to Output Capacitance (Input to Output Voltage = O, f = 1 MHz)	2.5	pF Max.

TABLE I.

CHARACTERISTICS REQUIRED OF TTL GATES WHICH ARE TO BE INTERFACED BY H74A1

PARAMETER	TEST CONDITIONS, FIGURE 2						LIMITS		
	V_{CC}		I_{IN}		I_{SINK}				
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
V_{OUT} (1)	4.5V					-0.4mA	2.4		Volts
V_{OUT} (0)	4.5V				12.0mA			0.4	Volts
V_{IN} (1)		5.5V		1.0mA			2.0		Volts
V_{IN} (0)		5.5V	-1.6mA					0.8	Volts

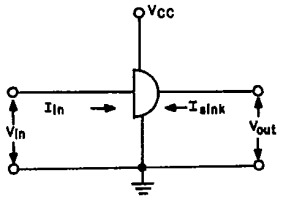


Figure 2.

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