RENESAS

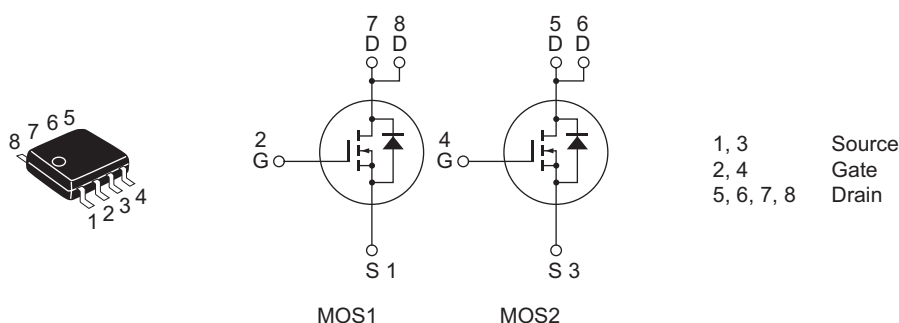# HAT2220R

Silicon N Channel MOS FET
High Speed Power Switching

Features

- Low on-resistance
- Low drive current
- High density mounting

Outline

RENESAS Package code: PRSP0008DD-D
(Package name: SOP-8 <FP-8DAV>)

1, 3	Source
2, 4	Gate
5, 6, 7, 8	Drain

MOS1   MOS2

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	450	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D [Note1]	0.7	A
Drain peak current	$I_{D(pulse)}$ [Note2]	2.1	A
Body-drain diode reverse drain current	I_{DR}	0.7	A
Avalanche current	I_{AP} [Note3]	0.7	A
Channel dissipation	Pch [Note4]	2	W
Channel dissipation	Pch [Note5]	3	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	−55 to +150	°C

Notes: 1. PW ≤ 1 s

2. PW ≤ 10 µs, duty cycle ≤ 1%

3. STch = 25 °C, Tch ≤ 150 °C

4. 1 Drive operation : When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10 s

5. 2 Drive operation : When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10 s

Electrical Characteristics

(Ta = 25°C)
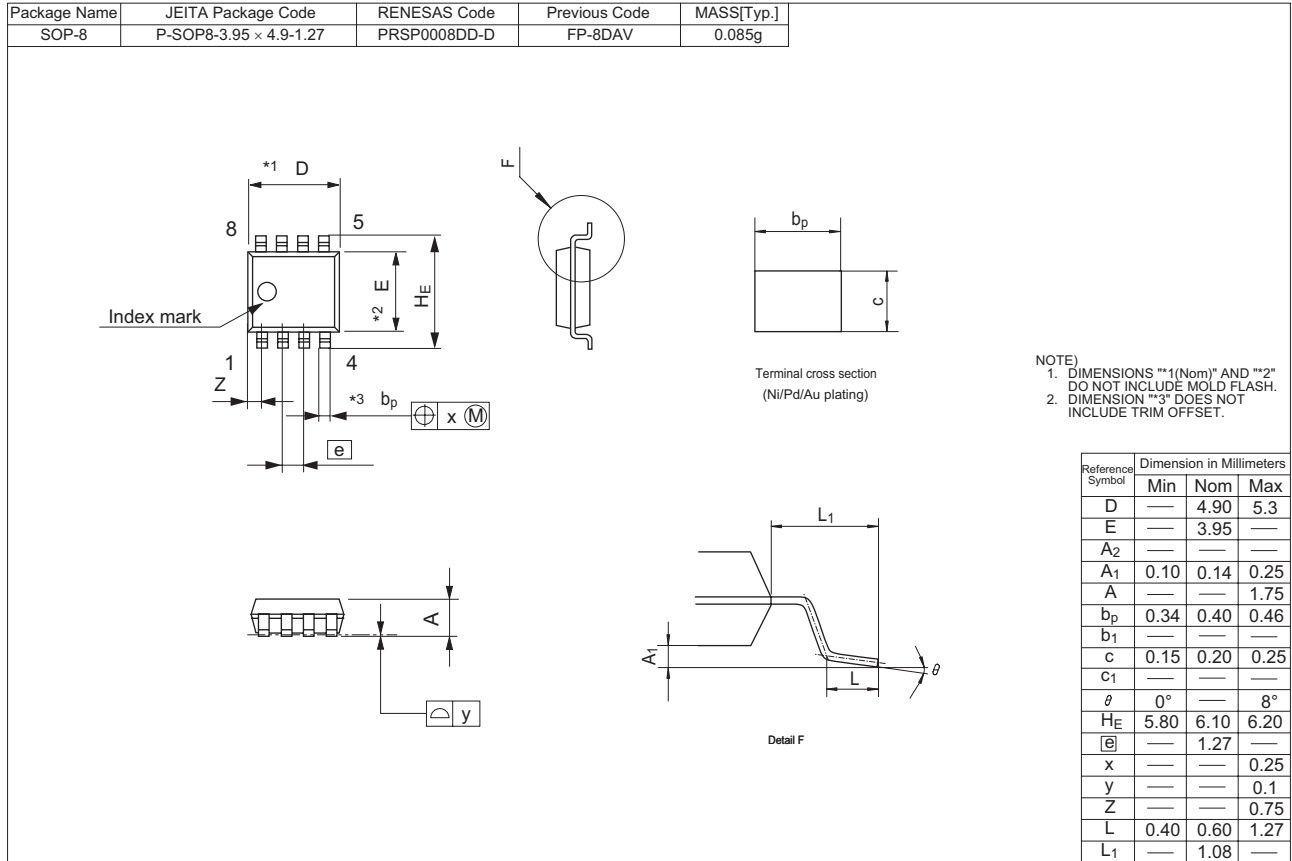
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	V_{DS} = 450 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±0.1	μA	V_{GS} = ±30 V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	3.0	—	4.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward transfer admittance	$\|y_{fs}\|$	0.55	0.95	—	S	I_D = 0.4 A, V_{DS} = 10 V [Note6]
Static drain to source on state resistance	$R_{DS(on)}$	—	5.5	6.5	Ω	I_D = 0.4 A, V_{GS} = 10 V [Note6]
Input capacitance	Ciss	—	140	—	pF	V_{DS} = 25 V
Output capacitance	Coss	—	17	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	5	—	pF	f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	22	—	ns	I_D = 0.4 A
Rise time	t_r	—	12	—	ns	V_{GS} = 10 V
Turn-off delay time	$t_{d(off)}$	—	38	—	ns	R_L = 562 Ω
Fall time	t_f	—	47	—	ns	Rg = 10 Ω
Total gate charge	Qg	—	4.9	—	nC	V_{DD} = 360 V
Gate to source charge	Qgs	—	0.6	—	nC	V_{GS} = 10 V
Gate to drain charge	Qgd	—	3.2	—	nC	I_D = 0.7 A
Body–drain diode forward voltage	V_{DF}	—	0.84	1.24	V	I_F = 0.7 A, V_{GS} = 0 [Note6]
Body–drain diode reverse recovery time	t_{rr}	—	120	—	ns	I_F = 0.7 A, V_{GS} = 0 di_F/dt = 100 A/ μs

Notes: 6. Pulse test

7. Since this device includes two high voltage Power MOS FET chips (V_{DSS} ≥ 450 V), high voltage margin may occur. (Between No.6 pin and No.7 pin in the outline fig.) Therefore, please be sure to confirm about Electric discharge between No.6 pin and No.7 pin in the equivalent circuit.

RENESAS

Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
SOP-8	P-SOP8-3.95 × 4.9-1.27	PRSP0008DD-D	FP-8DAV	0.085g

Index mark

Terminal cross section
(Ni/Pd/Au plating)

Detail F

NOTE)
1. DIMENSIONS "*1(Nom)" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	4.90	5.3
E	——	3.95	——
A_2	——	——	——
A_1	0.10	0.14	0.25
A	——	——	1.75
b_p	0.34	0.40	0.46
b_1	——	——	——
c	0.15	0.20	0.25
c_1	——	——	——
θ	0°	——	8°
H_E	5.80	6.10	6.20
e	——	1.27	——
x	——	——	0.25
y	——	——	0.1
Z	——	——	0.75
L	0.40	0.60	1.27
L_1	——	1.08	——

Ordering Information

Part No.	Quantity	Shipping Container
HAT2220R-EL-E	2500 pcs	Taping

Renesas Technology Corp. Sales Strategic Planning Div.   Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

http://www.renesas.com