
HD74AC195

4-bit Parallel-Access Shift Register

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Description

This shift register features parallel inputs, parallel outputs, J- \bar{K} serial inputs, Shift/Load control input, and a direct overriding clear. This shift register can operate in two modes: Parallel load; Shift from Q_0 towards Q_3 .

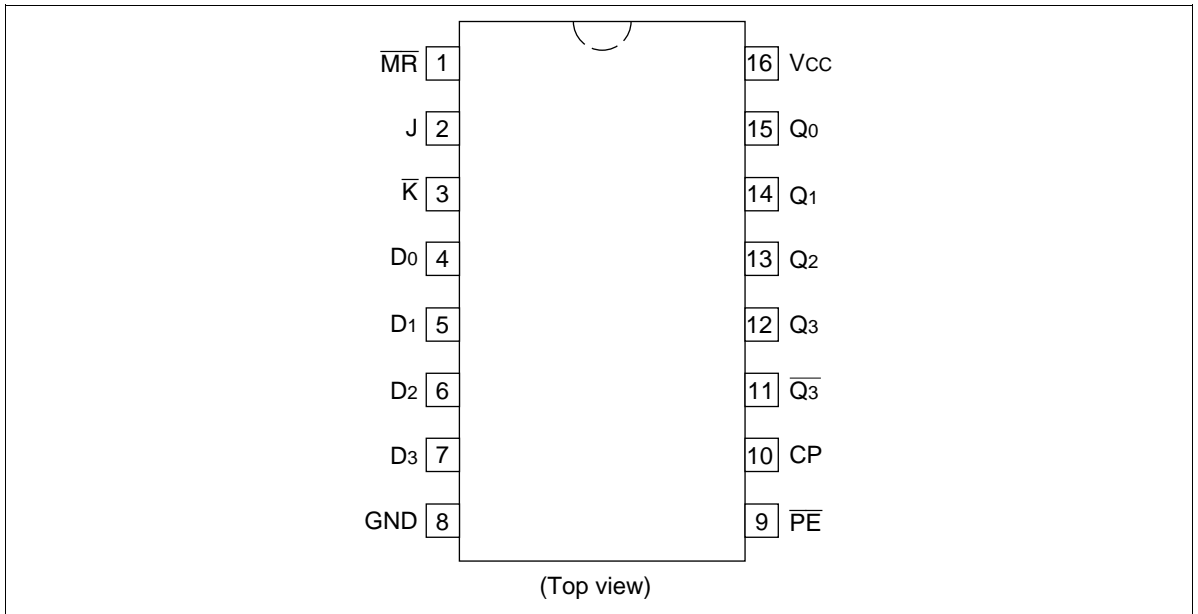
Parallel loading is accomplished by applying the four bits of data, and taking the \overline{PE} Input low. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the CP input. During parallel loading, serial data flow is inhibited. Serial shifting occurs synchronously when the \overline{PE} input is high. Serial data for this mode is entered at the J- \bar{K} inputs. These inputs allow the first stage to perform as a J- \bar{K} or toggle flip-flop as shown in the function table.

Features

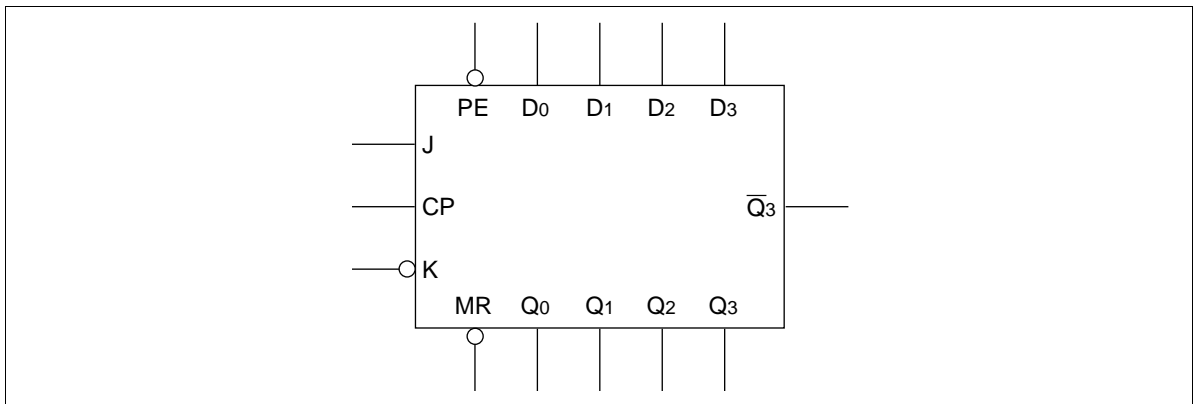
- Shift Right and Parallel Load Capability
- J- \bar{K} (D-Type) Inputs to First Stage
- Complement Output from Last Stage
- Asynchronous Master Reset
- Outputs Source/Sink 24 mA

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Pin Arrangement



Logic Symbol

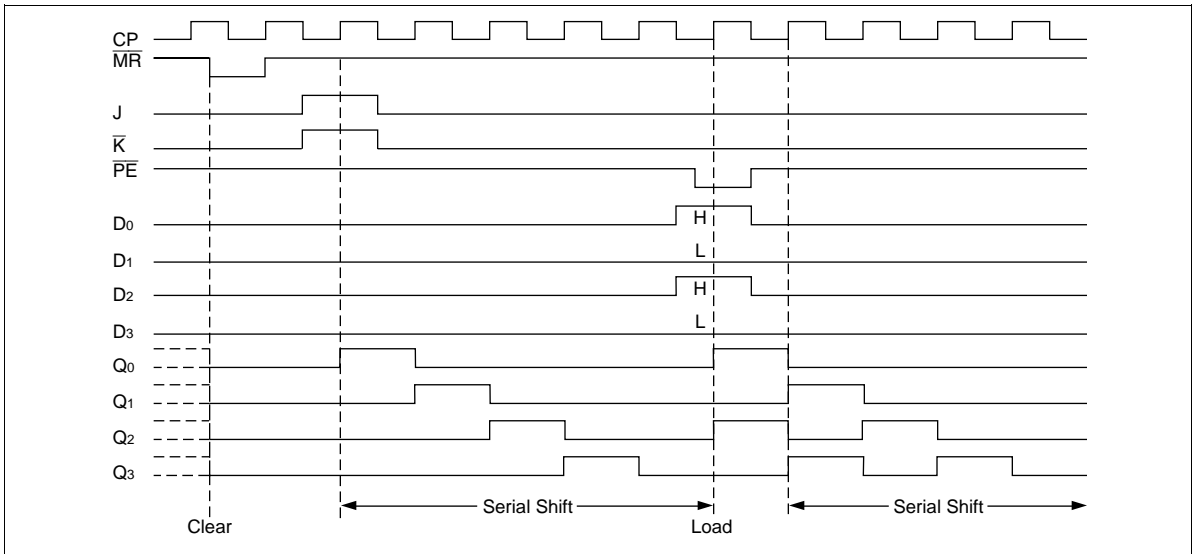


Pin Names

CP	Clock Pulse Input (Active Rising Edge)
D ₀ to D ₃	Parallel Data Inputs
\overline{PE}	Parallel Enable Input
\overline{MR}	Asynchronous Master Reset
J, \overline{K}	J- \overline{K} or D Type Serial Inputs
Q ₀ to Q ₃ , \overline{Q}_3	Outputs

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Timing Diagram



Mode Select-Function Table

Operating Modes	Inputs					Outputs					
	\overline{MR}	CP	\overline{PE}	J	\overline{K}	D_n	Q_0	Q_1	Q_2	Q_3	\overline{Q}_3
Asynchronous Reset	L	X	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	\lrcorner	H	H	H	X	H	q_0	q_1	q_2	\overline{q}_2
Shift, Reset First Stage	H	\lrcorner	H	L	L	X	L	q_0	q_1	q_2	\overline{q}_2
Shift, Toggle First Stage	H	\lrcorner	H	H	L	X	\overline{q}_0	q_0	q_1	q_2	\overline{q}_2
Shift, Retain First Stage	H	\lrcorner	H	L	H	X	q_0	q_0	q_1	q_2	\overline{q}_2
Parallel Load	H	\lrcorner	L	X	X	d_n	d_0	d_1	d_2	d_3	\overline{d}_3

H : HIGH Voltage Level

L : LOW Voltage Level

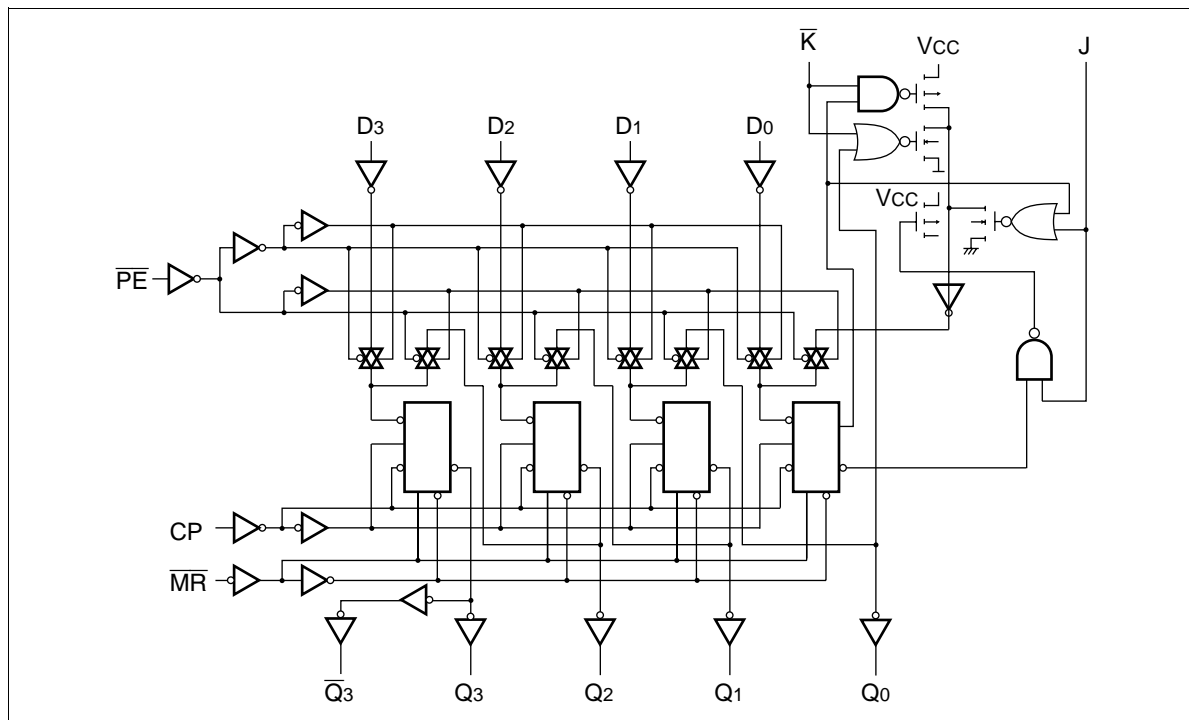
X : Immaterial

Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH transition.

\lrcorner : LOW-to-HIGH clock transition.

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Logic Diagram



DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	I_{CC}	80	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$, $T_a = \text{Worst case}$
Maximum quiescent supply current	I_{CC}	8.0	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$, $T_a = 25^\circ C$

AC Characteristics: HD74AC195

Item	Symbol	V _{cc} (V)* ¹	Ta = +25°C C _L = 50 pF			Ta = -40°C to +85°C C _L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum clock frequency	f _{max}	3.3	75	—	—	65	—	MHz
		5.0	100	—	—	85	—	
Propagation delay CP to Q _n or Q ₃	t _{PLH}	3.3	1.0	9.0	13.0	1.0	15.0	ns
		5.0	1.0	5.5	10.0	1.0	11.5	
Propagation delay CP to Q _n or Q ₂	t _{PHL}	3.3	1.0	9.0	13.0	1.0	15.0	ns
		5.0	1.0	6.5	10.0	1.0	11.5	
Propagation delay MR to Q ₂	t _{PLH}	3.3	1.0	7.5	10.5	1.0	12.0	ns
		5.0	1.0	5.5	8.0	1.0	9.5	
Propagation delay MR to Q _n	t _{PHL}	3.3	1.0	6.0	9.0	1.0	10.5	ns
		5.0	1.0	5.0	7.0	1.0	8.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements: HD74AC195

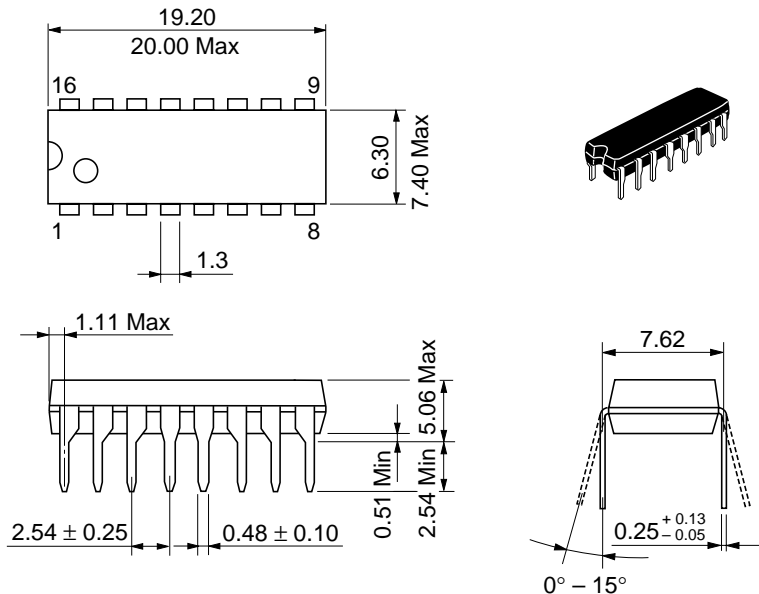
Item	Symbol	V _{cc} (V)* ¹	Ta = +25°C C _L = 50 pF		Ta = -40°C to +85°C C _L = 50 pF		Unit
			Typ	Guaranteed Minimum	Guaranteed Minimum	Guaranteed Minimum	
Setup time, HIGH or LOW J, K or D _n to CP	t _{su}	3.3	3.0	5.5	7.0	ns	
		5.0	2.0	4.0	5.0		
Hold time, HIGH or LOW J, K or D _n to CP	t _h	3.3	-0.5	2.0	3.6	ns	
		5.0	0.5	1.5	2.0		
Setup time, HIGH or LOW PE to CP	t _{su}	3.3	3.5	5.0	7.0	ns	
		5.0	2.5	4.0	5.0		
Hold time, HIGH or LOW PE to CP	t _h	3.3	-2.0	0.0	0.0	ns	
		5.0	-1.5	0.0	0.0		
Recovery time MR to CP	t _{rec}	3.3	-1.5	0.5	0.5	ns	
		5.0	-1.0	0.5	0.5		
Pulse width	t _w	3.3	-3.0	5.5	7.0	ns	
		5.0	-3.0	4.5	5.0		

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

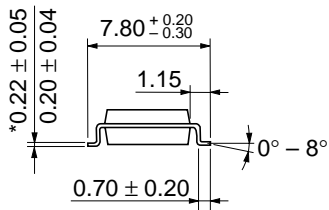
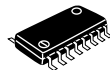
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Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C_{IN}	4.5	pF	$V_{CC} = 5.5 \text{ V}$
Power dissipation capacitance	C_{PD}	125	pF	$V_{CC} = 5.0 \text{ V}$



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



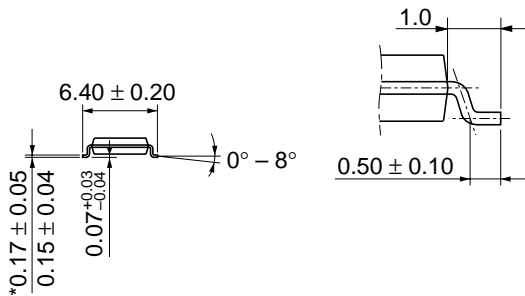
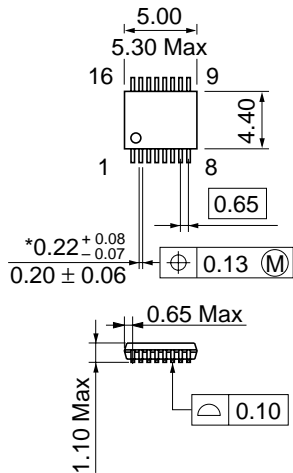
*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g



*Dimension including the plating thickness
 Base material dimension

Hitachi Code	TTP-16DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g

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