HD74AC4024

7-State Binary Counter

HITACHI

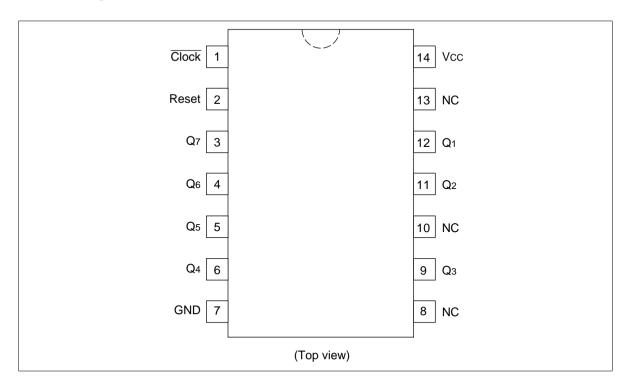
Description

The HD74AC4024 is a 4-stage counter. This device is incremented on the falling edge (negative transition) of the input clock, and all its output is reset to a low level by applying a logical high on its reset input.

Feature

• Outputs Source/Sink 24 mA

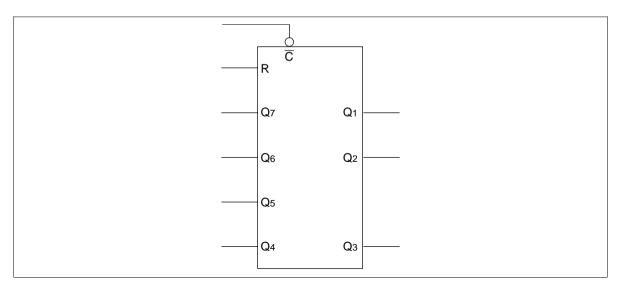
Pin Arrangement





HD74AC4024

Logic Symbol



Pin Names

Clock Input (Active Falling Edge)

Reset Master Reset Input

 Q_1 to Q_7 Outputs

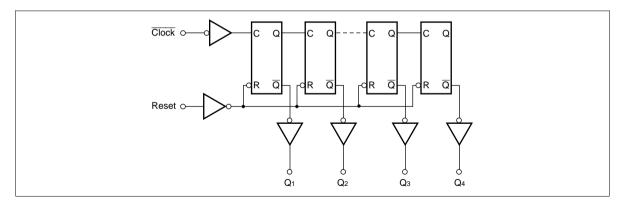
Function Table

Clock	Reset	Outputs State
L	L	No change
L	Н	All outputs are low
Н	L	No change
Н	Н	All outputs are low
	L	No change
	Н	All outputs are low
	L	Advance to next state
	Н	All outputs are low

H: High voltage level
L: Low voltage level

∴ Low-to-High Clock Transition∴ High-to-Low Clock Transition

Logic Diagram



DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	I _{cc}	80	μΑ	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 \text{ V}$, Ta = Worst case
Maximum quiescent supply current	I _{cc}	8.0	μΑ	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 \text{ V}$, $Ta = 25^{\circ}\text{C}$

AC Characteristics

			$Ta = +25^{\circ}C$ $C_{L} = 50 \text{ pF}$		Ta = -40° C to $+85^{\circ}$ C C _L = 50 pF			
Item	Symbol	V _{cc} (V)*1	Min	Тур	Max	Min	Max	Unit
Maximum clock	f _{max}	3.3	70	_	_	60	_	MHz
frequency		5.0	110	_	_	95	_	_
Propagation delay	t _{PLH}	3.3	1.0	9.5	12.5	1.0	13.5	ns
Clock to Q ₁		5.0	1.0	7.0	9.0	1.0	9.5	_
Propagation delay	t _{PHL}	3.3	1.0	9.5	12.0	1.0	13.0	ns
Clock to Q ₁		5.0	1.0	6.5	9.0	1.0	10.0	_
Propagation delay	t _{PHL}	3.3	1.0	10.5	12.5	1.0	13.5	ns
Reset to outputs		5.0	1.0	7.5	10.0	1.0	11.0	_

Note: 1. Voltage Range 3.3 is $3.3 \text{ V} \pm 0.3 \text{ V}$ Voltage Range 5.0 is $5.0 \text{ V} \pm 0.5 \text{ V}$

HD74AC4024

AC Operating Requirements

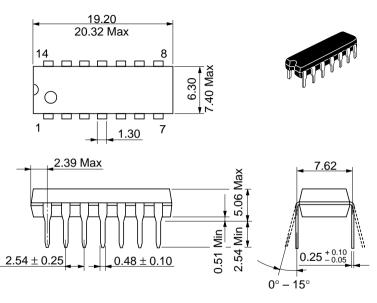
			Ta = +25°C C _L = 50 pF		Ta = -40°C to +85°C C _L = 50 pF	
Item	Symbol	V _{cc} (V)*1	Тур	Guarante	eed Minimum	Unit
Reset to Clock	t _{rec}	3.3	-2.5	0.0	0.0	ns
		5.0	-1.5	0.0	0.0	_
Pulse width Clock	t _w	3.3	3.0	4.0	4.5	ns
		5.0	2.0	3.0	3.5	

Note: 1. Voltage Range 3.3 is $3.3 \text{ V} \pm 0.3 \text{ V}$ Voltage Range 5.0 is $5.0 \text{ V} \pm 0.5 \text{ V}$

Capacitance

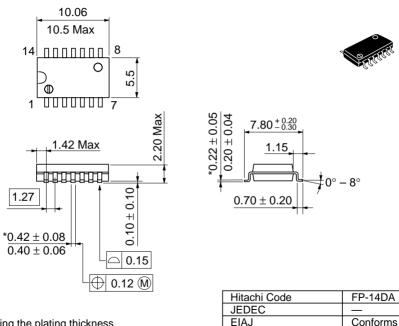
Item	Symbol	Тур	Unit	Condition
Input capacitance	C _{IN}	4.5	pF	V _{CC} = 5.5 V
Power dissipation capacitance	C_{PD}	60	pF	V _{CC} = 5.0 V

Unit: mm



Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g

Unit: mm

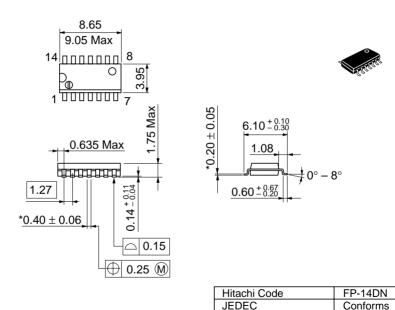


Weight (reference value)

0.23 g

*Dimension including the plating thickness
Base material dimension

Unit: mm



EIAJ

Weight (reference value)

Conforms

0.13 g

*Pd plating

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