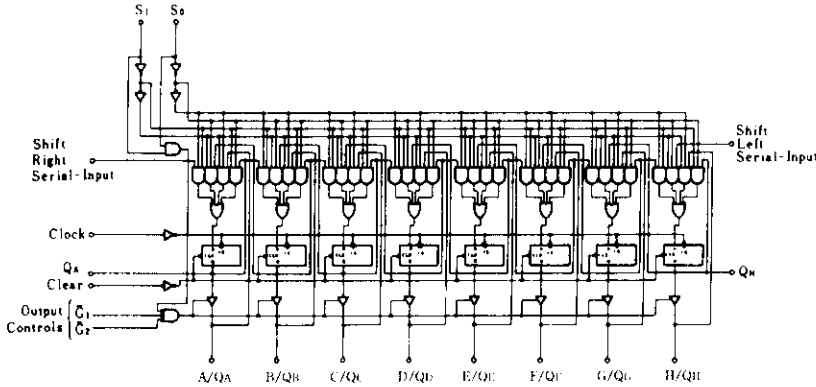


# HD74LS299 • 8-bit Universal Shift/Storage Registers (with three-state outputs)

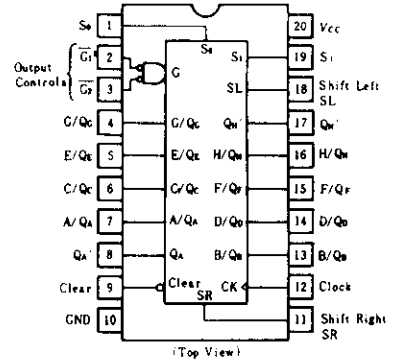
This eight-bit universal register features multiplexed inputs/outputs to achieve full eight bit data. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table. Synchronous parallel loading is accomplished by taking both function select lines,  $S_0$  and  $S_1$ , high. This places the three-

state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

## ■ BLOCK DIAGRAM



## ■ PIN ARRANGEMENT



## ■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	7.0	V
Input voltage	$V_{IN}$	7.0	V
Output voltage (off-state)	$V_{O(off)}$	5.5	V
Operating temperature range	$T_{op}$	-20 ~ +75	°C
Storage temperature range	$T_{stg}$	-65 ~ +150	°C

## ■ FUNCTION TABLE

Mode	Inputs						Inputs/Outputs								Outputs			
	Clear	Function Select		Output Control		Clock	Serial		A/Q <sub>A</sub>	B/Q <sub>B</sub>	C/Q <sub>C</sub>	D/Q <sub>D</sub>	E/Q <sub>E</sub>	F/Q <sub>F</sub>	G/Q <sub>G</sub>	H/Q <sub>H</sub>	Q <sub>A</sub> '	Q <sub>H</sub> '
		S <sub>1</sub>	S <sub>0</sub>	$\bar{G}_1 \uparrow$	$\bar{G}_2 \uparrow$		S <sub>L</sub>	S <sub>R</sub>										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q <sub>E0</sub>	Q <sub>F0</sub>	Q <sub>G0</sub>	Q <sub>H0</sub>	Q <sub>A0</sub>	Q <sub>H0</sub>
	H	X	X	L	L	L	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q <sub>E0</sub>	Q <sub>F0</sub>	Q <sub>G0</sub>	Q <sub>H0</sub>	Q <sub>A0</sub>	Q <sub>H0</sub>
Shift Right	H	L	H	L	L	↑	X	H	H	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	H	Q <sub>Gn</sub>
	H	L	H	L	L	↑	X	L	L	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	L	Q <sub>Cn</sub>
Shift Left	H	H	L	L	L	↑	H	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	Q <sub>Hn</sub>	H	Q <sub>Bn</sub>	H
	H	H	L	L	L	↑	L	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	Q <sub>Hn</sub>	L	Q <sub>Bn</sub>	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	b

- Notes) 1. H; high level, L; low level, X; irrelevant  
 2. ↑; transition from low to high level  
 3. a~h; the level of steady-state input at inputs A through H, respectively. These data are loaded into the flip-flop outputs are isolated from the input/output terminals.  
 4. Q<sub>A0</sub>~Q<sub>H0</sub>; the level of Q<sub>A</sub> through Q<sub>H</sub>, respectively, before the indicated steady-state input conditions were established.

5. Q<sub>An</sub>~Q<sub>Hn</sub>; the level of Q<sub>A</sub> through Q<sub>H</sub>, respectively, before the most-recent ↑ transition of the clock.  
 6. † =; When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state, however, sequential operation or clearing of the register is not affected.

## RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Output current	$Q_A \sim Q_H$	—	—	-2.6	mA
	$Q_A' \text{ or } Q_H'$	—	—	-0.4	
Output current	$Q_A \sim Q_H$	—	—	24	mA
	$Q_A' \text{ or } Q_H'$	—	—	8	
Clock frequency	$f_{max}$	0	—	25	MHz
Clock pulse width	Clock high	30	—	—	ns
	Clock low	10	—	—	
Clear pulse width	Clear low	20	—	—	ns
Setup time	Select	35 †	—	—	ns
	High-level data	20 †	—	—	
	Low-level data	20 †	—	—	
	Clear inactive-state	20 †	—	—	
Hold time	Select	10 †	—	—	ns
	Data	10 †	—	—	

† The arrow indicates the rising edge.

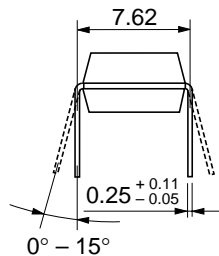
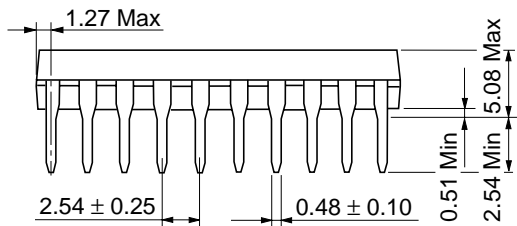
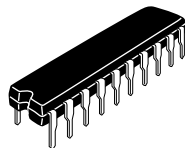
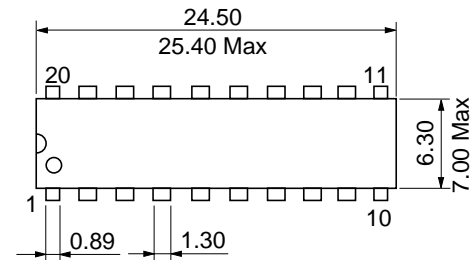
## ELECTRICAL CHARACTERISTICS ( $T_a = -20 \sim +75^\circ\text{C}$ )

Item	Symbol	Test Conditions	min	typ*	max	Unit		
Input voltage	$V_{IH}$		2.0	—	—	V		
	$V_{IL}$		—	—	0.8	V		
Output voltage	$Q_A$ thru $Q_H$	$V_{OH}$	$V_{CC}=4.75\text{V}, V_{IH}=2\text{V}, V_{IL}=0.8\text{V}$	$I_{OH}=-2.6\text{mA}$	2.4	—	V	
	$Q_A' \text{ or } Q_H'$			$I_{OH}=-400\mu\text{A}$	2.7	—		
	$Q_A$ thru $Q_H$	$V_{OL}$	$V_{CC}=4.75\text{V}, V_{IH}=2\text{V}, V_{IL}=0.8\text{V}$	$I_{OL}=12\text{mA}$	—	—	V	
	$Q_A' \text{ or } Q_H'$			$I_{OL}=24\text{mA}$	—	—		0.5
				$I_{OL}=4\text{mA}$	—	—	0.4	
				$I_{OL}=8\text{mA}$	—	—	0.5	
Output current	$Q_A$ thru $Q_H$	$I_{OZH}$	$V_{CC}=5.25\text{V}, V_{IH}=2\text{V}, V_O=2.7\text{V}$	—	—	40	$\mu\text{A}$	
	$Q_A$ thru $Q_H$	$I_{OZL}$	$V_{CC}=5.25\text{V}, V_{IH}=2\text{V}, V_O=0.4\text{V}$	—	—	-400	$\mu\text{A}$	
Input current	$S_0, S_1, A \sim H$	$I_{IN}$	$V_{CC}=5.25\text{V}, V_I=2.7\text{V}$	—	—	40	$\mu\text{A}$	
	Any other			—	—	20		
	$S_0, S_1$	$I_{IL}$	$V_{CC}=5.25\text{V}, V_I=0.4\text{V}$	—	—	-0.8	mA	
	Any other			—	—	-0.4		
	$S_0, S_1$	$I_I$	$V_{CC}=5.25\text{V}$	$V_I=7\text{V}$	—	—	0.2	mA
	$A \sim H$			$V_I=5.5\text{V}$	—	—	0.1	
Any other	$V_I=7\text{V}$			—	—	0.1		
Short-circuit output current	$Q_A$ thru $Q_H$	$I_{OS}$	$V_{CC}=5.25\text{V}$	-30	—	-130	mA	
	$Q_A' \text{ or } Q_H'$			-20	—	-100		
Supply current	$I_{CC}$	$V_{CC}=5.25\text{V}$	—	33	53	mA		
Input clamp voltage	$V_{IK}$	$V_{CC}=4.75\text{V}, I_{IN}=-18\text{mA}$	—	—	-1.5	V		

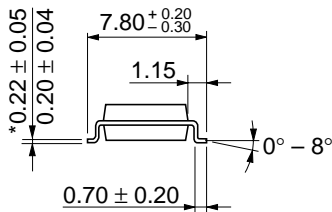
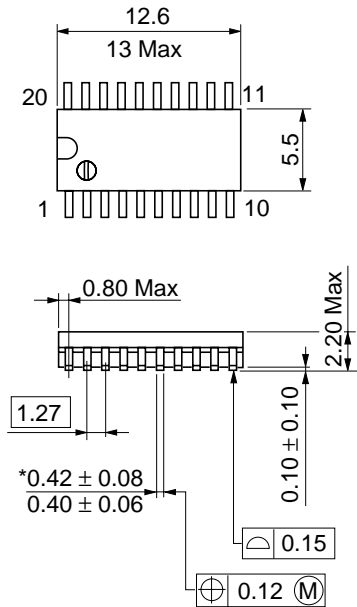
\*  $V_{CC}=5\text{V}, T_a=25^\circ\text{C}$

## SWITCHING CHARACTERISTICS ( $V_{CC}=5\text{V}, T_a=25^\circ\text{C}$ )

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	$f_{max}$				25	35	—	MHz
Propagation delay time	$t_{PLH}$	Clock	$Q_A' \text{ or } Q_H'$	$C_L=15\text{pF}, R_L=2\text{k}\Omega$	—	22	33	ns
	$t_{PHL}$				—	26	39	
	$t_{PHL}$	Clear	$Q_A' \text{ or } Q_H'$		—	27	40	
	$t_{PLH}$				—	17	25	
Output enable time	$t_{PHL}$	Clock	$Q_A \sim Q_H$	$C_L=45\text{pF}, R_L=665\Omega$	—	26	39	ns
	$t_{PHL}$				—	26	40	
	$t_{ZH}$	Clear	$Q_A \sim Q_H$		—	13	21	
	$t_{ZL}$				$\bar{G}_1, \bar{G}_2$	—	19	
Output disable time	$t_{HZ}$	$\bar{G}_1, \bar{G}_2$	$Q_A \sim Q_H$	$C_L=5\text{pF}, R_L=665\Omega$	—	10	15	ns
	$t_{LZ}$				—	10	15	

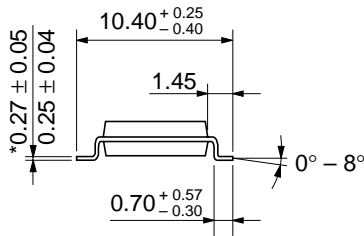
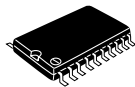
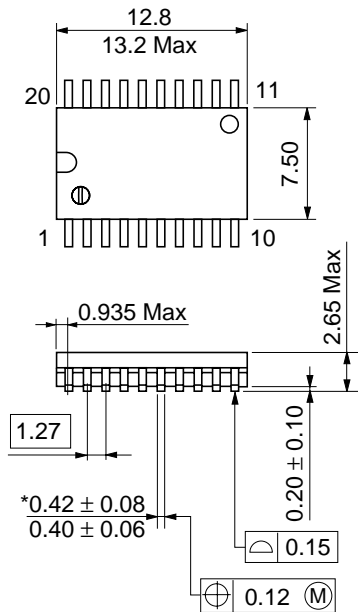


Hitachi Code	DP-20N
JEDEC	—
EIAJ	Conforms
Weight (reference value)	1.26 g



Hitachi Code	FP-20DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.31 g

\*Dimension including the plating thickness  
Base material dimension



Hitachi Code	FP-20DB
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.52 g

\*Dimension including the plating thickness  
 Base material dimension

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