HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6501

256 x 4 CMOS RAM

JULY 1978

Features

- LOW STANDBY POWER . . . . . 55μW MAX
- LOW OPERATING POWER . . . . . 22mW/MHz MAX
- FAST ACCESS TIME . . . . . 220nsec MAX
- DATA RETENTION VOLTAGE . . . . . 2.0 VOLTS MIN.
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE - 2 TTL LOADS
- HIGH NOISE IMMUNITY
- ON CHIP ADDRESS REGISTERS
- THREE STATE OUTPUTS
- EASY MICROPROCESSOR INTERFACING
- LATCHED OUTPUTS
- MILITARY AND INDUSTRIAL TEMPERATURE RANGES

Description

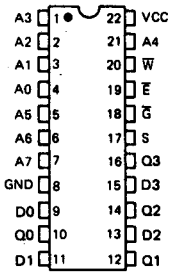
The HM-6501 is a 256 by 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6501 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

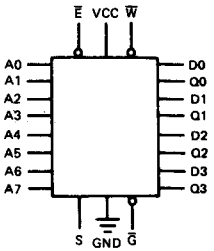
Pinout

TOP VIEW

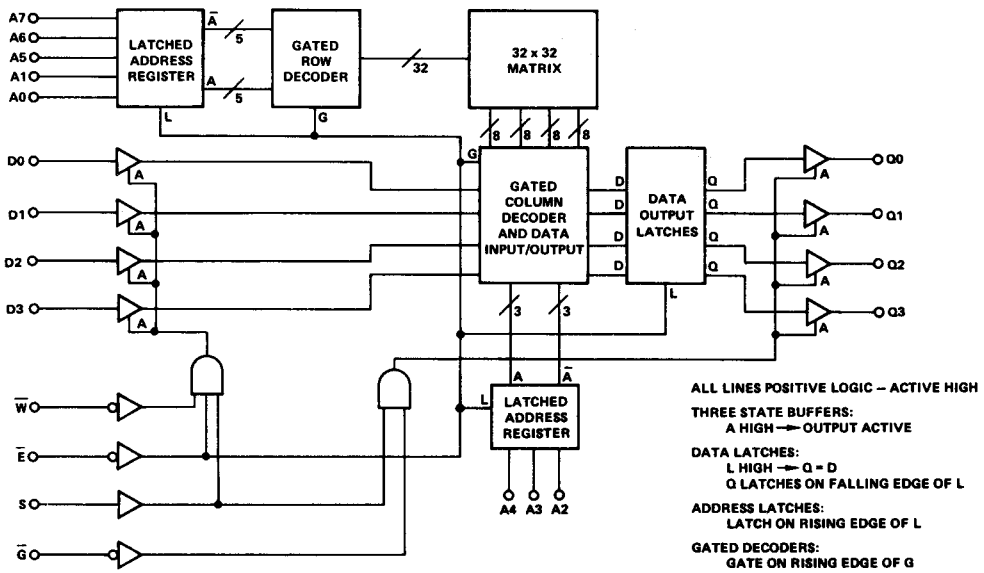


A - ADDRESS INPUT
E - CHIP ENABLE
W - WRITE ENABLE
G - OUTPUT ENABLE
S - CHIP SELECT
D - DATA INPUT
Q - DATA OUTPUT

Logic Symbol



Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage -VCC	+8.0V
Applied Input or Output Voltage	GND -0.3V VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

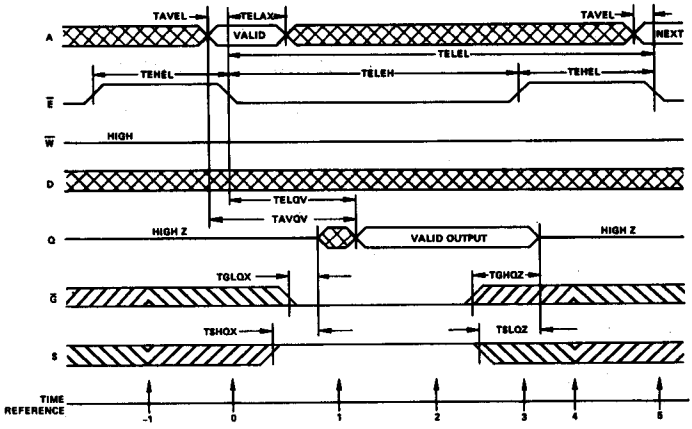
Operating Supply Voltage -VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10 1(+25°C)		0.1	1	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10		0.01	1	µA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.4mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		220		120	170	ns	④
	TAVQV	Address Access Time		220		110	170	ns	④
	TSHQX	Chip Select Output Enable Time		130		50	90	ns	④
	TGLQX	Output Enable Output Enable Time		130		50	90	ns	④
	TSLQZ	Chip Select Output Disable Time		130		50	90	ns	④
	TGHQZ	Output Enable Output Disable Time		130		50	90	ns	④
	TELEH	Chip Enable Pulse Negative Width	220		170	120		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		70	50		ns	④
	TAVEL	Address Setup Time	0		0	-10		ns	④
	TELAX	Address Hold Time	40		30	20		ns	④
	TDVWH	Data Setup Time	100		80	50		ns	④
	TWHDX	Data Hold Time	0		0	-10		ns	④
	TWLSL	Chip Select Write Pulse Setup Time	120		100	60		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	120		100	60		ns	④
	TSHWH	Chip Select Write Pulse Hold Time	120		100	60		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	120		100	60		ns	④
	TWLWH	Write Enable Pulse Width	120		100	60		ns	④
	TELEL	Read or Write Cycle Time	320		240	170		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

Read Cycle



TRUTH TABLE

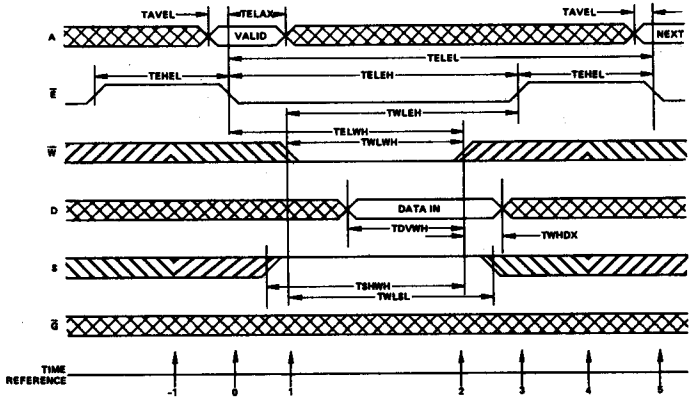
TIME REFERENCE	INPUTS Ē	S	Ḡ	W̄	A	D	OUTPUT Q	FUNCTION
-1	H	L	H	X	X	X	Z	MEMORY DISABLED
0	↘	L	H	H	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	L	H	X	X	X	OUTPUT ENABLED
2	L	H	L	H	X	X	V	OUTPUT VALID
3	↗	H	L	H	X	X	V	OUTPUT LATCHED
4	H	L	H	X	X	X	Z	DEVICE DISABLED, PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	L	H	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The read cycle is initiated by the falling edge of Ē. This signal latches the input address word into on chip registers providing that minimum address setup and hold times are met. After the required hold time, the address inputs may change state without affecting device operation. For the output to be read, Ḡ and Ē must be low; W̄ and S must be high. The output data will be valid at accesss time (TELQV) or at one output enable time (TSHQX or TGLQX), whichever is the latter occuring signal.

S and Ḡ are complementary signals which simplify the external logic required for decoding in expanded memory arrays. Either or both of these signals may be used to disable the outputs when or-tying several memories in an array. The HM-6501 has output data latches that are controlled by Ē.

When Ē goes high the outputs are latched to contain the present data. The output buffers can be forced to a high impedance state by either Ḡ or S but the latches will only unlatch on the falling edge of Ē.

Write Cycle



ABSOLUTE MAXIMUM RATINGS

Supply Voltage -VCC	+8.0V
Applied Input or Output Voltage	GND -0.3V VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC Commercial	4.75V to 5.25V
Operating Temperature Commercial	0°C to 75°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100		10	100	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0			V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ⩽ VI ⩽ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ⩽ VO ⩽ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 1.6mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.2mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		350		200	300	ns	④
	TAVQV	Address Access Time		360		200	310	ns	④
	TSHQX	Chip Select Output Enable Time		180		80	160	ns	④
	TGLQX	Output Enable Output Enable Time		180		80	160	ns	④
	TSLQZ	Chip Select Output Disable Time		180		80	160	ns	④
	TGHQZ	Output Enable Output Disable Time		180		80	160	ns	④
	TELEH	Chip Enable Pulse Negative Width	350		300	200		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		130	90		ns	④
	TAVEL	Address Setup Time	10		10	0		ns	④
	TELAX	Address Hold Time	70		50	40		ns	④
	TDVWH	Data Setup Time	170		140	120		ns	④
	TWHDX	Data Hold Time	0		0	-10		ns	④
	TWLSL	Chip Select Write Pulse Setup Time	210		170	150		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	210		170	150		ns	④
	TSHWH	Chip Select Write Pulse Hold Time	210		170	150		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	210		170	150		ns	④
	TWLWH	Write Enable Pulse Width	210		170	150		ns	④
	TELEL	Read or Write Cycle Time	500		430	290		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply Voltage -VCC	
		Military (-2)	4.5V to 5.5V
Applied Input or Output Voltage	GND -0.3V VCC +0.3V	Industrial (-9)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	-65°C to +150°C	Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10 1(+25°C)		1.0	1	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10		0.1	1	µA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.4mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300		160	240	ns	④
	TAVQV	Address Access Time		300		150	240	ns	④
	TSHQX	Chip Select Output Enable Time		150		60	120	ns	④
	TGLQX	Output Enable Output Enable Time		150		60	120	ns	④
	TSLQZ	Chip Select Output Disable Time		150		60	120	ns	④
	TGHQZ	Output Enable Output Disable Time		150		60	120	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		240	160		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		70	50		ns	④
	TAVEL	Address Setup Time	0		0	-10		ns	④
	TELAX	Address Hold Time	50		40	30		ns	④
	TDVWH	Data Setup Time	150		120	100		ns	④
	TWHDX	Data Hold Time	0		0	-10		ns	④
	TWLSL	Chip Select Write Pulse Setup Time	180		150	120		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	180		150	120		ns	④
	TSHWH	Chip Select Write Pulse Hold Time	180		150	120		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	180		150	120		ns	④
	TWLWH	Write Enable Pulse Width	180		150	120		ns	④
	TELEL	Read or Write Cycle Time	400		310	210		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	S	$\overline{G}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	L	X	X	X	X	SEE NOTE	MEMORY DISABLED
0	↘	X	X	X	V	X		CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	↘	X	X		WRITE PERIOD BEGINS
2	L	H	X	↗	X	V		DATA IN IS WRITTEN
3	↗	X	X	H	X	X		WRITE IS COMPLETED
4	H	L	X	X	X	X		PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	X	X	V	X		CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

NOTE: IF $\overline{G}$ IS HIGH, THE OUTPUT WILL BE HIGH IMPEDANCE.
IF $\overline{G}$ IS LOW, THE INPUT DATA WILL PROPAGATE TO THE OUTPUT.

As in the read mode, the write cycle is initiated by the falling edge of $\overline{E}$ which latches the addresses. The write portion of the cycle is defined as $\overline{E}$ and $\overline{W}$ being low simultaneously with S high. If the inputs and outputs are tied together, $\overline{G}$ must be high. The write portion of the cycle is terminated on the first rising edge of $\overline{E}$, $\overline{W}$, or the falling edge of S. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the rising edge of $\overline{E}$ or to the falling edge of S, whichever occurs first. By positioning the $\overline{W}$ pulse at different times within the $\overline{E}$ low time (TELEH) various types of write cycles may be performed.

If the $\overline{E}$ low time (TELEH) is greater than the $\overline{W}$ pulse (TWLWH) plus an output enable time (TSHQX or TGLQX) a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

The data inputs and data outputs may be tied together for use with a common I/O bus structure is the system control line $\overline{G}$ ($\overline{G}$ NOT) is NAND-ed with $\overline{W}$ to produce the device $\overline{G}$ signal. This will force the output buffers to a high impedance state during write operations so input data can be applied to the bus. A minimum delay of one output disable time must be allowed before applying input data to the bus. This will insure that the output buffers are not active.

Battery Backup Applications

The HM-6501 is especially well suited for use in battery backup systems. Data retention supply voltage and supply current are guaranteed over the full temperature range.

When designing the backup system, the following suggestions should be considered:

1.) As RAM VCC drops, the input logical one voltages should follow so as not to exceed VCC +0.3. It is suggested to use CMOS drivers, operating at CMOS VCC, such as the HD-6495, HD-6432, and HD-6433. Anther approach is the use of open collector or open drain buffers pulled up to CMOS VCC.

2.) $\overline{E}$ must be held high at CMOS VCC and S must be held low at ground. $\overline{W}$, $\overline{G}$, address, and data inputs should be held at GND or CMOS VCC.

3.) When exiting from the battery backup mode, VCC should ramp without ring or discontinuities.

4.) The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 or 4.75V).

A very simple battery backup system is shown in Figure 1. When system power is available, diode D1 is forward biased and supplies current to the CMOS devices. Upon loss of system power, diode D1 is reverse biased and only CMOS devices are consuming battery power. A disadvantage to this method is that CMOS VCC is one diode drop, .7V, below TTL VCC. There is a possibility that a TTL output signal could rise higher than CMOS VCC and cause possible latch problems. This possibility can be reduced by incorporating a system similar to that shown in Figure 2. Other alternatives include using a germanuin diode yielding a VF $\approx$ .2V or adding diode D2 in the TTL supply and raising VCC to account for the drop. A PNP transistor is substituted for the diode in Figure 2. The saturation drop of the transistor, 0.2V, is less than the 0.7V drop of the diode giving more margin against latch-up. A power fail output signal is available to disable the chip enable circuitry. Open collector TTL with pullups to CMOS VCC or LS type TTL should be used as memory drivers. This will insure that the CMOS inputs are not floating during the backup period. When system power is restored, operation continues as normal and the NI-CAD battery pack is trickle charged through RC.

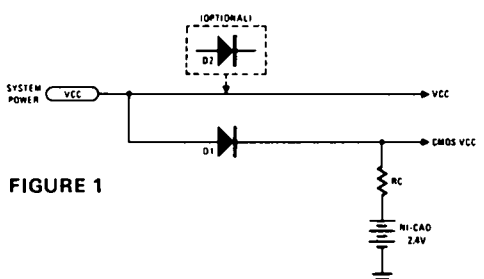


FIGURE 1

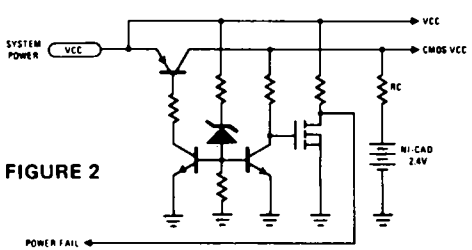


FIGURE 2