FAIRCHILD
SEMICONDUCTOR®

April 2005

HUFA76404DK8T
N-Channel Dual MOSFET

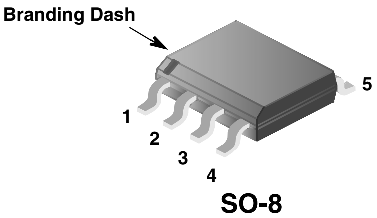
62V, 3.2A, 132mΩ

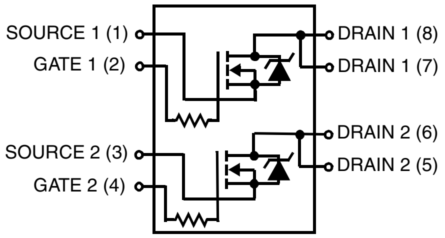
Features

- $r_{DS(ON)}$ = 110mΩ (Typ.), V_{GS} = 5V, I_D = 3.2A
- $Q_{g(tot)}$ = 3.8nC (Typ.), V_{GS} = 5V
- Low Miller Charge
- Low Q_{RR} Body Diode
- Optimized efficiency at high frequencies
- UIS Capability (Single Pulse and Repetitive Pulse)
- Internal R_G = 100Ω
- Qualified to AEC Q101

Applications

- Motor / Body Load Control
- ABS Systems
- Powertrain Management
- Injection Systems
- DC-DC converters and Off-line UPS
- Distributed Power Architectures and VRMs
- Primary Switch for 12V and 24V systems





MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	62	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current Continuous (T_A = 25°C, V_{GS} = 10V, $R_{\theta JA}$ = 50°C/W)	3.6	A
	Continuous (T_A = 25°C, V_{GS} = 5V, $R_{\theta JA}$ = 50°C/W)	3.2	A
	Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	128	mJ
P_D	Power dissipation	2.5	W
	Derate above 25°C	20	mW/°C
T_J, T_{STG}	Operating and Storage Temperature	-55 to 150	°C

Thermal Characteristics

$R_{\theta JA}$	Pad Area = 0.50 in^2 (323 mm^2) (Note 2)	50	°C/W
$R_{\theta JA}$	Pad Area = 0.027 in^2 (17.4 mm^2) (Note 3)	170	°C/W
$R_{\theta JA}$	Pad Area = 0.006 in^2 (3.87 mm^2) (Note 4)	183	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
76404DK8	HUFA76404DK8T	SO-8	330mm	12mm	2500 units

Electrical Characteristics T_A = 25°C unless otherwise noted

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	62	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 55V, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 50V, V_{GS} = 0V, T_A = 150°C	-	-	250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V	-	-	±100	nA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(TH)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	1	-	3	V
$r_{DS(ON)}$	Drain to Source On Resistance	I_D = 3.6A, V_{GS} = 10V	-	0.088	0.110	Ω
		I_D = 3.2A, V_{GS} = 5V	-	0.110	0.132	

Dynamic Characteristics

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
C_{ISS}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	250	-	pF
C_{OSS}	Output Capacitance			-	80	-	pF
C_{RSS}	Reverse Transfer Capacitance			-	7	-	pF
R_G	Gate Resistance	V_{GS} = 0.5V, f = 1MHz		-	100	-	Ω
$Q_{g(tot)}$	Total Gate Charge at 5V	V_{GS} = 0V to 5V	V_{DD} = 30V I_D = 3.6A I_g = 1.0mA	-	3.8	4.9	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0V to 1V		-	0.3	0.4	nC
Q_{gs}	Gate to Source Gate Charge			-	0.8	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau			-	0.5	-	nC
Q_{gd}	Gate to Drain “Miller” Charge			-	1.7	-	nC

Switching Characteristics ($V_{GS} = 10V$)

t_{ON}	Turn-On Time	$V_{DD} = 30V$, $I_D = 3.6A$ $V_{GS} = 10V$, $R_{GS} = 47\Omega$	-	-	65	ns
$t_{d(ON)}$	Turn-On Delay Time		-	13	-	ns
t_r	Rise Time		-	26	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	145	-	ns
t_f	Fall Time		-	53	-	ns
t_{OFF}	Turn-Off Time		-	-	330	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 3.6A$	-	-	1.25	V
		$I_{SD} = 1.8A$	-	-	1.0	V
t_{rr}	Reverse Recovery Time	$I_{SD}= 3.6A$, $dI_{SD}/dt= 100A/\mu s$	-	-	37	ns
Q_{RR}	Reverse Recovered Charge	$I_{SD}= 3.6A$, $dI_{SD}/dt= 100A/\mu s$	-	-	38	nC

Notes:

1: Starting $T_J = 25°C$, $L = 41mH$, $I_{AS} = 2.5A$, $V_{DD} = 62V$, $V_{GS} = 10V$.

2: $50^oC/W$ measured using FR-4 board with 0.50 in^2 (323 mm^2) copper pad at 1 second.

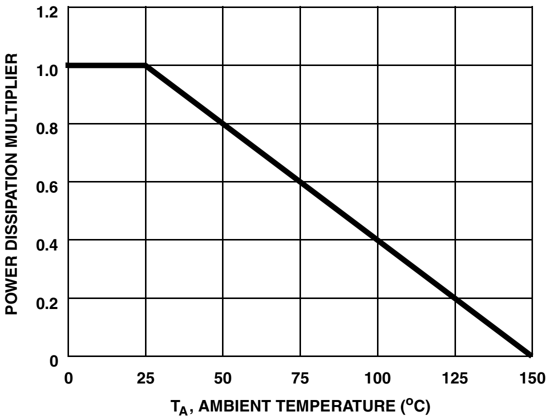
3: $170^oC/W$ measured using FR-4 board with 0.027 in^2 (17.4 mm^2) copper pad at 1000 seconds.

4: $183^oC/W$ measured using FR-4 board with 0.006 in^2 (3.87 mm^2) copper pad at 1000 seconds.

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: http://www.aecouncil.com/

All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

Typical Characteristics T_A = 25°C unless otherwise noted



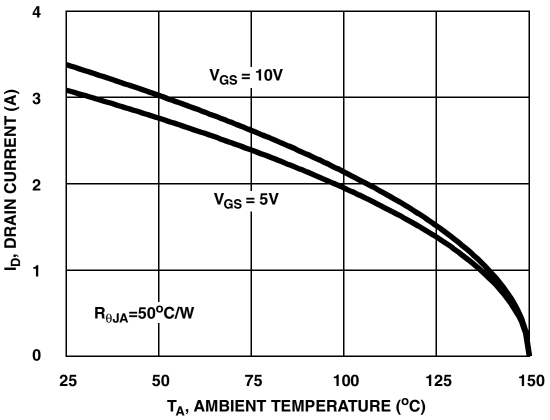


Figure 1. Normalized Power Dissipation vs Ambient Temperature

Figure 2. Maximum Continuous Drain Current vs Ambient Temperature

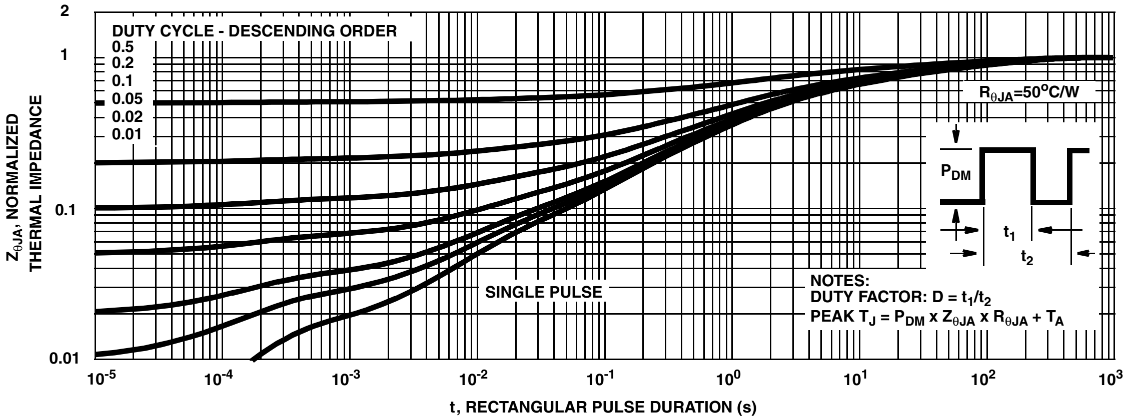


Figure 3. Normalized Maximum Transient Thermal Impedance

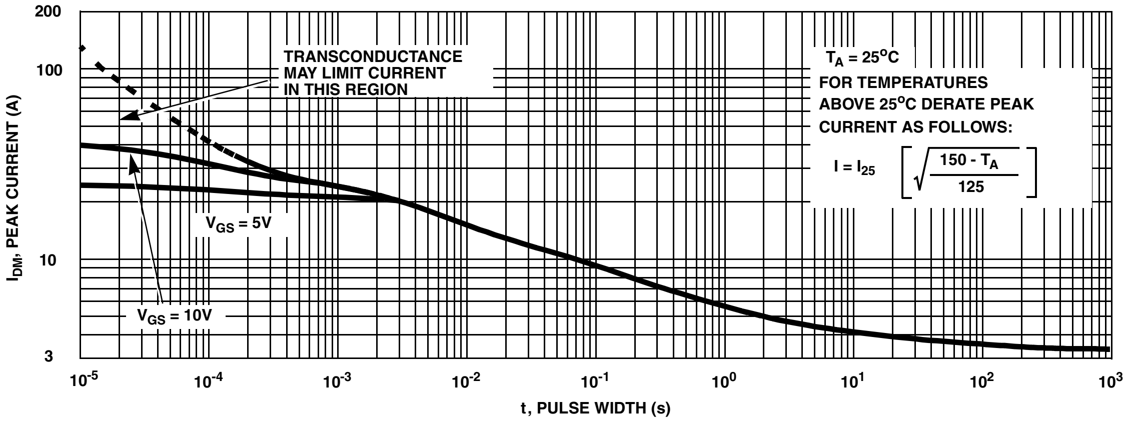


Figure 4. Peak Current Capability

Typical Characteristics T_A = 25°C unless otherwise noted

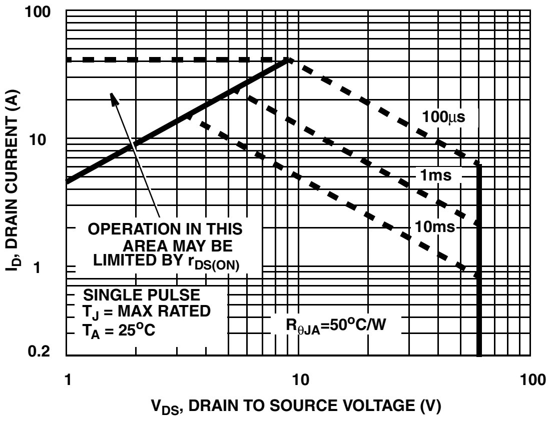


Figure 5. Forward Bias Safe Operating Area

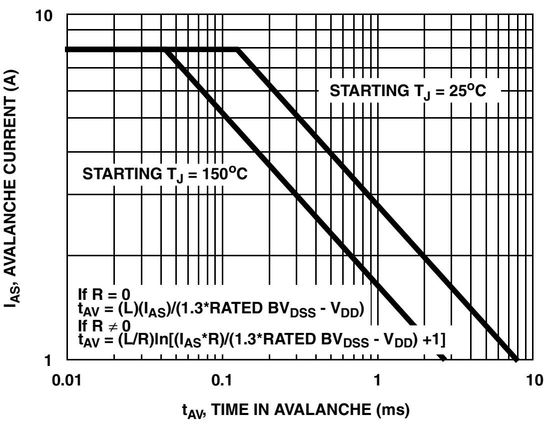


Figure 6. Unclamped Inductive Switching Capability

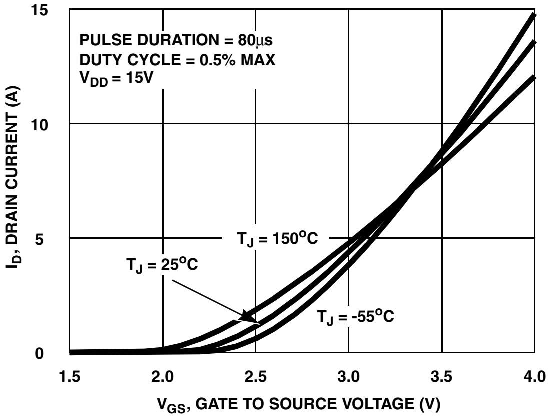


Figure 7. Transfer Characteristics

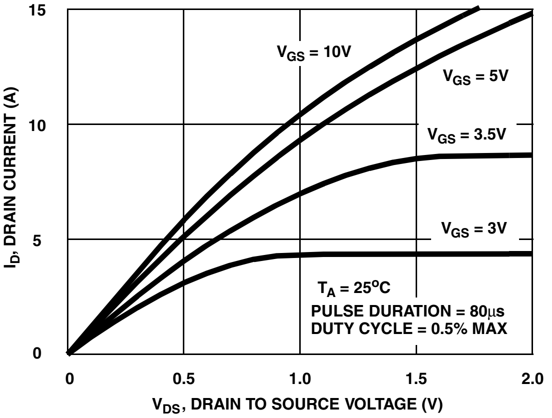


Figure 8. Saturation Characteristics

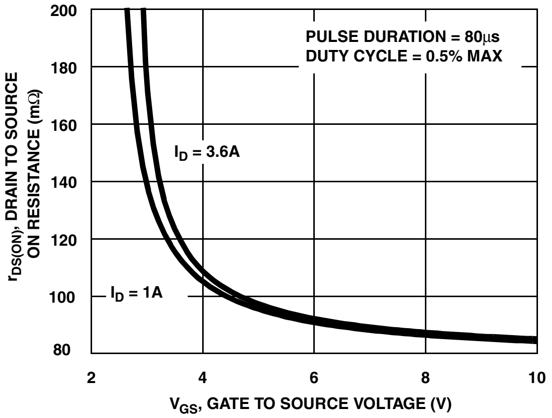


Figure 9. Drain to Source On Resistance vs Gate Voltage and Drain Current

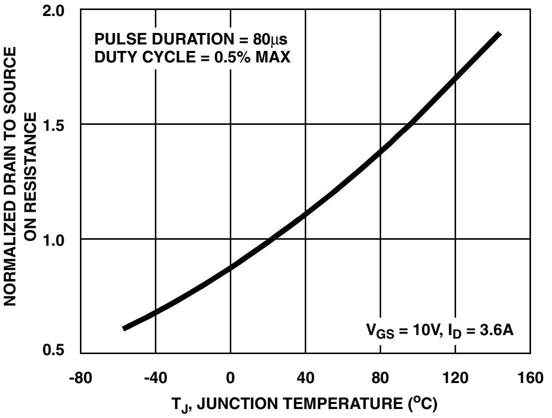


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics T_A = 25°C unless otherwise noted

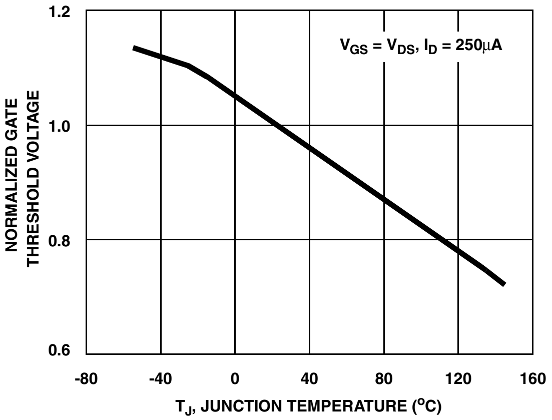


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

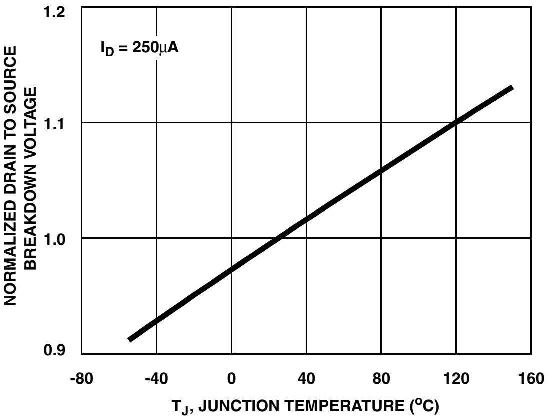


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

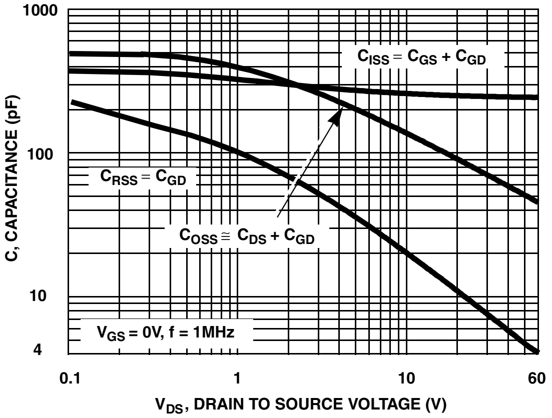


Figure 13. Capacitance vs Drain to Source Voltage

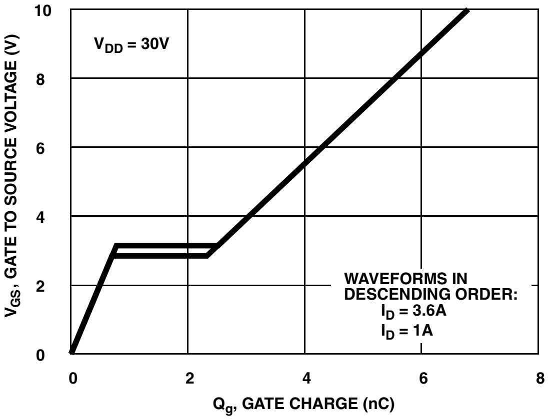


Figure 14. Gate Charge Waveforms for Constant Gate Currents

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM}, and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM}, in an application. Therefore the application's ambient temperature, T_A (^oC), and thermal resistance $R_{\theta JA}$ ($^oC/W$) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \qquad \text{(EQ. 1)}$$

In using surface mount devices such as the SO8 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2. The area, in square inches is the top copper area including the gate and source pads.

$$R_{\theta JA} = 79.9 + \frac{15}{0.14 + Area} \qquad \text{(EQ. 2)}$$

The transient thermal impedance ($Z_{\theta JA}$) is also effected by varied top copper board area. Figure 22 shows the effect of copper pad area on single pulse transient thermal impedance. Each trace represents a copper pad area in square inches corresponding to the descending list in the graph. Spice and SABER thermal models are provided for each of the listed pad areas.

Copper pad area has no perceivable effect on transient thermal impedance for pulse widths less than 100ms. For pulse widths less than 100ms the transient thermal impedance is determined by the die and package. Therefore, CTHERM1 through CTHERM5 and RTHERM1 through RTHERM5 remain constant for each of the thermal models. A listing of the model component values is available in Table 1.

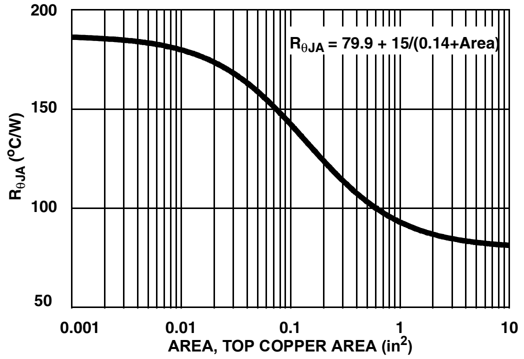


Figure 21. Thermal Resistance vs Mounting Pad Area

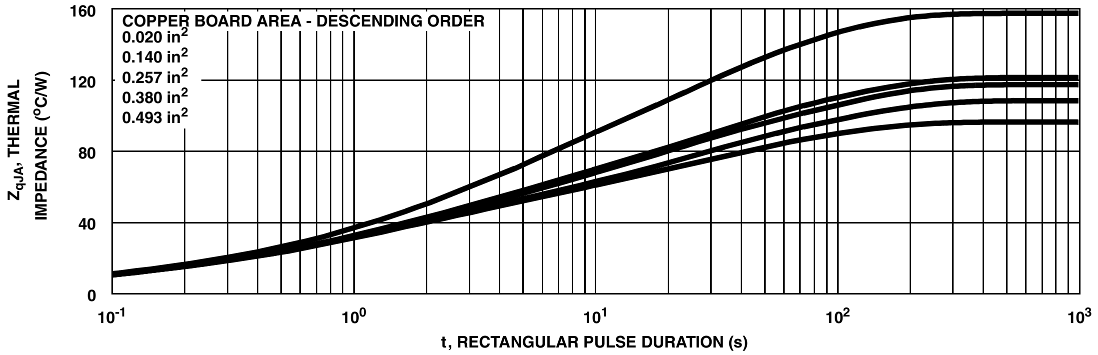


Figure 22. Thermal Impedance vs Mounting Pad Area

Test Circuits and Waveforms

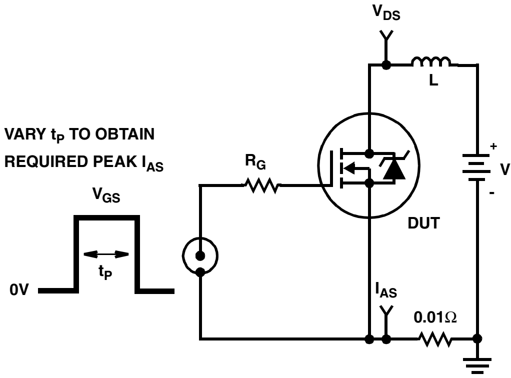


Figure 15. Unclamped Energy Test Circuit

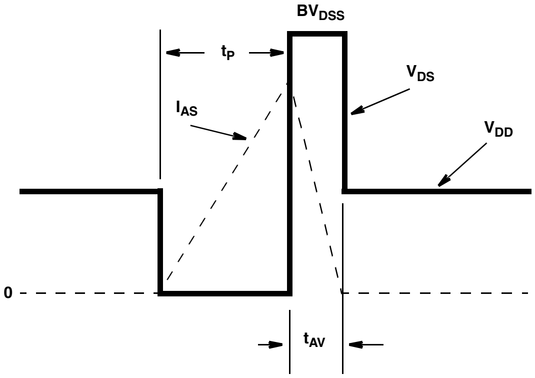


Figure 16. Unclamped Energy Waveforms

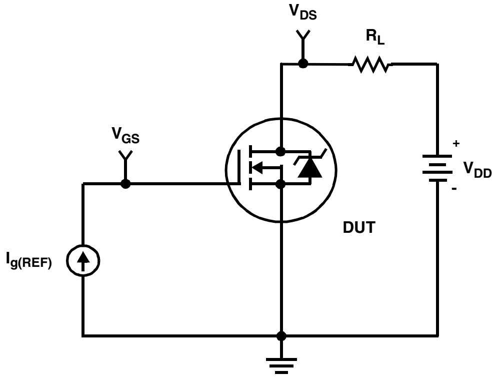


Figure 17. Gate Charge Test Circuit

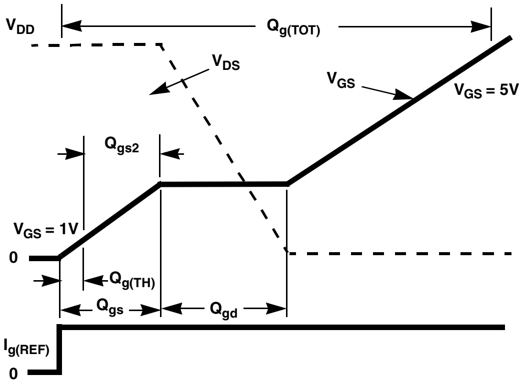


Figure 18. Gate Charge Waveforms

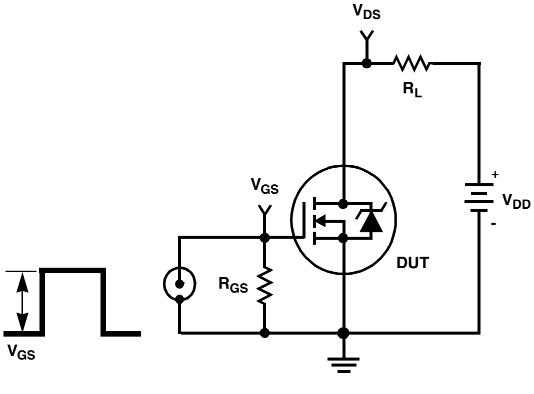


Figure 19. Switching Time Test Circuit

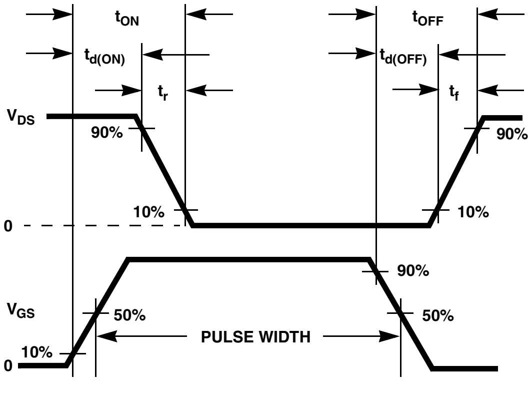
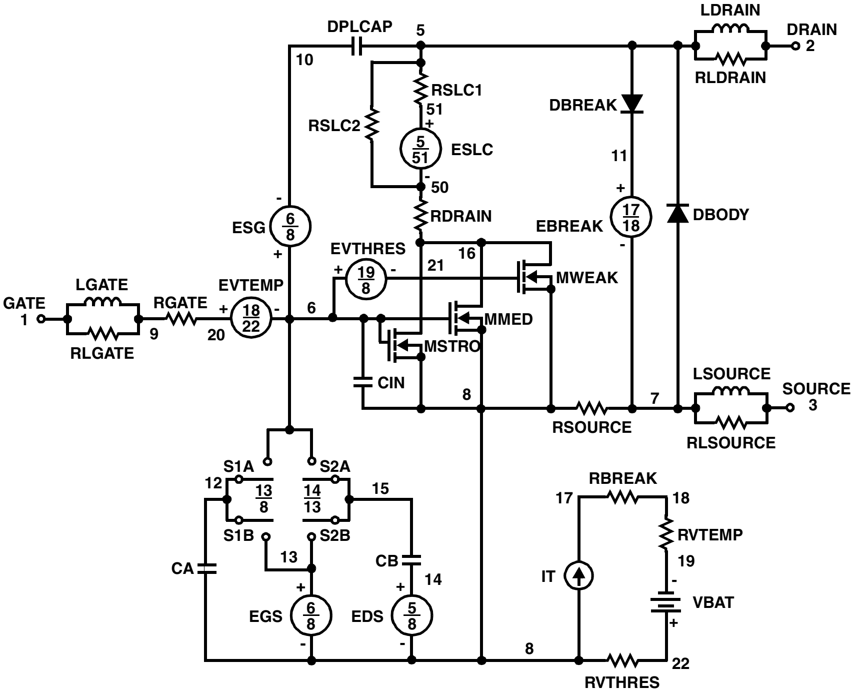


Figure 20. Switching Time Waveforms

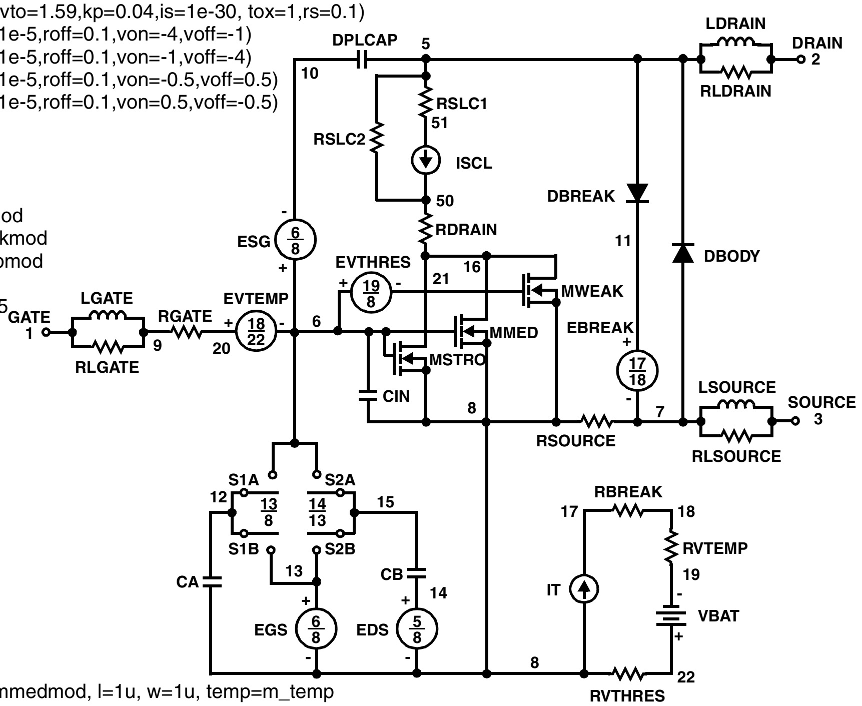
PSPICE Electrical Model



```
.SUBCKT HUFA76404DK8T 2 1 3 ;        rev March 2004
Ca 12 8 3.8e-10
Cb 15 14 3.8e-10
Cin 6 8 2.6e-10

Dbody 7 5 DbodyMOD
Dbreak 5 11 DbreakMOD
Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 62.5
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evthres 6 21 19 8 1
Evtemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 2.22e-9
Ldrain 2 5 1.0e-9
Lsource 3 7 0.93e-9

RLgate 1 9 22.2
RLdrain 2 5 10
RLsource 3 7 9.3

Mmed 16 6 8 8 MmedMOD
Mstro 16 6 8 8 MstroMOD
Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1
Rdrain 50 16 RdrainMOD 2.4e-2
Rgate 9 20 103.3
RSLC1 5 51 RSLCMOD 1.0e-6
RSLC2 5 50 1.0e3
Rsource 8 7 RsourceMOD 5.4e-2
Rvthres 22 8 RvthresMOD 1
Rvtemp 18 19 RvtempMOD 1
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50  VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*18),3.7))}

.MODEL DbodyMOD D (IS=1.1E-12 N=1.03 RS=2.7e-2 TRS1=5.0e-4 TRS2=1.3e-6
+ CJO=6.82e-10 M=0.85 TT=1.6e-8 XTI=4.0)
.MODEL DbreakMOD D (RS=1.65 TRS1=1.0e-3 TRS2=-9e-6)
.MODEL DplcapMOD D (CJO=1.7e-10 IS=1.0e-30 N=10 M=0.85)

.MODEL MstroMOD NMOS (VTO=2.13 KP=19 IS=1e-30 N=10 TOX=1 L=1u W=1u T_ABS=25)
.MODEL MmedMOD NMOS (VTO=1.81 KP=1.08 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=103.3 T_ABS=25)
.MODEL MweakMOD NMOS (VTO=1.59 KP=0.04 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=103.3e1 RS=0.1 T_ABS=25)

.MODEL RbreakMOD RES (TC1=1.12e-3 TC2=-3e-7)
.MODEL RdrainMOD RES (TC1=1.0e-2 TC2=5e-5)
.MODEL RSLCMOD RES (TC1=2.8e-3 TC2=1.9e-5)
.MODEL RsourceMOD RES (TC1=4e-3 TC2=1e-6)
.MODEL RvthresMOD RES (TC1=-2.1e-3 TC2=-3.3e-6)
.MODEL RvtempMOD RES (TC1=-1.6e-3 TC2=1.0e-6)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4 VOFF=-1)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1 VOFF=-4)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.5 VOFF=0.5)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=0.5 VOFF=-0.5)

.ENDS
```

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model



```
REV March 2004
template HUFA76404DK8T n2,n1,n3=m_temp
number m_temp=25
electrical n2,n1,n3
{
var i iscl
dp..model dbodymod =  (isl=1.1e-12,nl=1.03,rs=2.7e-2,trs1=5.0e-4,trs2=1.3e-6,cjo=6.82e-10,m=0.85,tt=1.6e-8,xti=4.0)
dp..model dbreakmod = (rs=1.65,trs1=1.0e-3,trs2=-9e-6)
dp..model dplcapmod =  (cjo=1.7e-10,isl=10.0e-30,nl=10,m=0.85)
m..model mstrongmod = (type=_n,vto=2.13,kp=19,is=1e-30, tox=1)
m..model mmedmod = (type=_n,vto=1.81,kp=1.08,is=1e-30, tox=1)
m..model mweakmod = (type=_n,vto=1.59,kp=0.04,is=1e-30, tox=1,rs=0.1)
sw_vcsp..model s1amod =  (ron=1e-5,roff=0.1,von=-4,voff=-1)
sw_vcsp..model s1bmod =  (ron=1e-5,roff=0.1,von=-1,voff=-4)
sw_vcsp..model s2amod =  (ron=1e-5,roff=0.1,von=-0.5,voff=0.5)
sw_vcsp..model s2bmod =  (ron=1e-5,roff=0.1,von=0.5,voff=-0.5)
c.ca n12 n8 = 3.8e-10
c.cb n15 n14 = 3.8e-10
c.cin n6 n8 = 2.6e-10

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod

spe.ebreak n11 n7 n17 n18 = 62.5
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1

i.it n8 n17 = 1

l.lgate n1 n9 = 2.22e-9
l.ldrain n2 n5 = 1.0e-9
l.lsource n3 n7 = 0.93e-9

res.rlgate n1 n9 = 22.2
res.rldrain n2 n5 = 10
res.rlsource n3 n7 = 9.3

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u, temp=m_temp
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u, temp=m_temp
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u, temp=m_temp

res.rbreak n17 n18  = 1, tc1=1.12e-3,tc2=-3e-7
res.rdrain n50 n16  = 2.4e-2, tc1=1.8e-2,tc2=5e-5
res.rgate n9 n20 = 103.3
res.rslc1 n5 n51  = 1.0e-6, tc1=2.8e-3,tc2=1.9e-5
res.rslc2 n5 n50 = 1.0e3
res.rsource n8 n7  = 5.4e-2, tc1=4e-3,tc2=1e-6
res.rvthres n22 n8  = 1, tc1=-2.1e-3,tc2=-3.3e-6
res.rvtemp n18 n19  = 1, tc1=-1.6e-3,tc2=1e-6
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1
equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/18))** 3.7))
}
```

SPICE Thermal Model

```
REV March 2004
HUFA76404DK8T
Copper Area =0.5 in2

CTHERM1 TH 8 1.2e-4
CTHERM2 8 7 4.6e-3
CTHERM3 7 6 5.0e-3
CTHERM4 6 5 1.6e-2
CTHERM5 5 4 4.5e-2
CTHERM6 4 3 1.3e-1
CTHERM7 3 2 6.7e-1
CTHERM8 2 TL 5.5

RTHERM1 TH 8 1.55
RTHERM2 8 7 1.9
RTHERM3 7 6 2.8
RTHERM4 6 5 9.8
RTHERM5 5 4 19
RTHERM6 4 3 22
RTHERM7 3 2 23
RTHERM8 2 TL 24
```

SABER Thermal Model

```
Copper Area = 0.5 in2
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 8 =1.2e-4
ctherm.ctherm2 8 7 =4.6e-3
ctherm.ctherm3 7 6 =5.0e-3
ctherm.ctherm4 6 5 =1.6e-2
ctherm.ctherm5 5 4 =4.5e-2
ctherm.ctherm6 4 3 =1.3e-1
ctherm7 3 2 6.7e-1
ctherm8 2 tl 5.5

rtherm.rtherm1 th 8 =1.55
rtherm.rtherm2 8 7 =1.9
rtherm.rtherm3 7 6 =2.8
rtherm.rtherm4 6 5 =9.8
rtherm.rtherm5 5 4 =19
rtherm.rtherm6 4 3 =22
rtherm.rtherm7 3 2 =23
rtherm.rtherm8 2 tl  =24
}
```

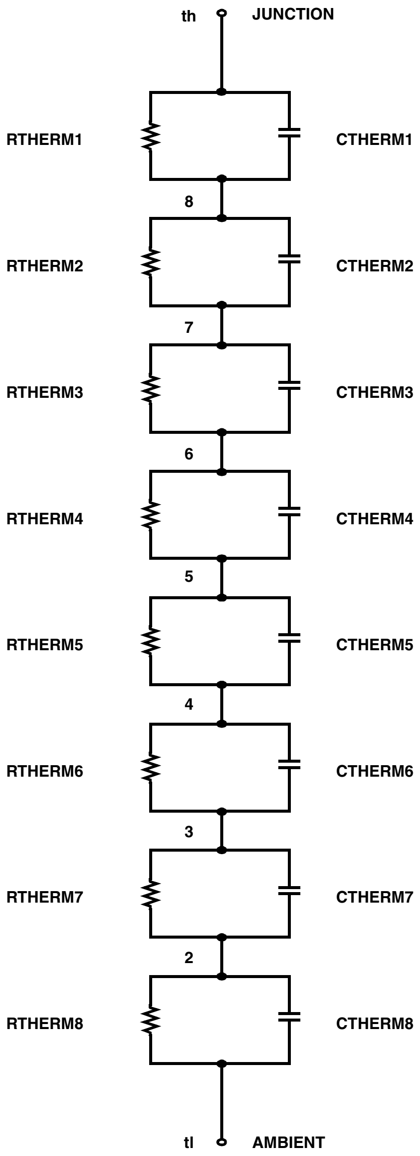


Table 1. Thermal Models

COMPONENT	0.02 in^2	0.14 in^2	0.257 in^2	0.38 in^2	0.493 in^2
CTHERM6	9.0e-1	1.3e-1	1.5e-1	1.5e-1	1.3e-1
CTHERM7	4.0e-1	6.0e-1	4.5e-1	6.5e-1	6.7e-1
CTHERM8	1.4	2.5	2.2	3.0	5.5
RTHERM6	39	26	20	20	22
RTHERM7	42	32	31	29	23
RTHERM8	48	35	38	31	24

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™
ActiveArray™
Bottomless™
CoolFET™
CROSSVOLT™
DOME™
EcoSPARK™
E^2CMOS™
EnSigna™
FACT™
FACT Quiet Series™
FAST®
FASTr™
FPS™
FRFET™
GlobalOptoisolator™
GTO™
HiSeC™
I^2C™
i-Lo™

Across the board. Around the world.™
The Power Franchise®
Programmable Active Droop™

ImpliedDisconnect™
IntelliMAX™
ISOPLANAR™
LittleFET™
MICROCOUPLER™
MicroFET™
MicroPak™
MICROWIRE™
MSX™
MSXPro™
OCX™
OCXPro™
OPTOLOGIC®
OPTOPLANAR™
PACMAN™
POP™
Power247™
PowerEdge™
PowerSaver™
PowerTrench®
QFET®
QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
RapidConnect™
µSerDes™
SILENT SWITCHER®
SMART START™
SPM™
Stealth™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SyncFET™
TinyLogic®
TINYOPTO™
TruTranslation™
UHC™
UltraFET®
UniFET™
VCX™

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. I15