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ICS843251I-12
FEMTOCLOCKS™ CRYSTAL-TO-3.3V, 2.5V LVPECL CLOCK GENERATOR

GENERAL DESCRIPTION

The ICS843251I-12 is a 10Gb Ethernet Clock Generator and a member of the HiPerClocks™ family of high performance devices from ICS. The ICS843251I-12 uses an 18pF parallel resonant crystal over the range of 23.2MHz - 30MHz. For Ethernet applications, a 25MHz crystal is used. The device has excellent <1ps phase jitter performance, over the 1.875MHz - 20MHz integration range. The ICS843251I-12 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

FEATURES

- One Differential LVPECL output

- Crystal oscillator interface, 18pF parallel resonant crystal (23.2MHz - 30MHz)

- Output frequency range: 290MHz - 750MHz

- VCO range: 580MHz - 750MHz

- RMS phase jitter @ 312.5MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.36ps (typical)

- 3.3V or 2.5V operating supply

- -40°C to 85°C ambient operating temperature

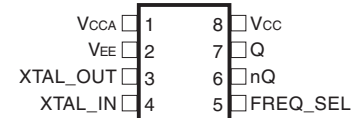- Available in both standard and lead-free RoHS-compliant packages

COMMON CONFIGURATION TABLE

Inputs					Output Frequency (MHz)
Crystal Frequency (MHz)	FREQ_SEL	M	N	Multiplication Value M/N	
25	0	25	1	25	625
25	1	25	2	12.5	312.5

BLOCK DIAGRAM
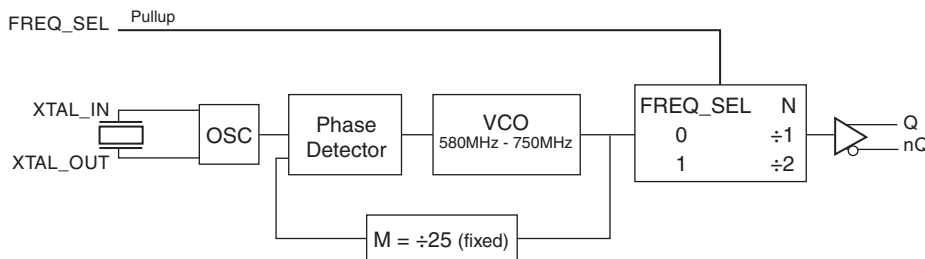
PIN ASSIGNMENT

ICS843251I-12
8-Lead TSSOP
4.4mm x 3.0mm x 0.925mm
package body
G Package
Top View

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TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{CCA}	Power		Analog supply pin.
2	V_{EE}	Power		Negative supply pin.
3, 4	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
5	FREQ_SEL	Input	Pullup	Frequency select pin. LVCMOS/LVTTL interface levels.
6, 7	nQ, Q	Output		Differential clock outputs. LVPECL interface levels.
8	V_{CC}	Power		Core supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	101.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V\pm5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current			TBD		mA

TABLE 3B. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA} = 2.5V\pm5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.375	2.5	2.625	V
V_{CCA}	Analog Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current			TBD		mA

TABLE 3C. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V\pm5\%$ OR $2.5V\pm5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	V_{CC} = 3.3V	2		V_{CC} + 0.3	V
		V_{CC} = 2.5V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	V_{CC} = 3.3V	-0.3		0.8	V
		V_{CC} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	V_{CC} = V_{IN} = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA

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TABLE 3D. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V\pm5\%$ OR $2.5V\pm5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.4		V_{CC} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		23.2		30	MHz
Equivalent Series Resistance (ESR)				TBD	Ω
Shunt Capacitance				7	pF
Drive Level				TBD	mW

TABLE 5A. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V\pm5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL = 1		312.5		MHz
		F_SEL = 0		625		MHz
$t$jit(Ø)	RMS Phase Jitter (Random); NOTE 1	312.5MHz @ Integration Range: 1.875MHz - 20MHz		0.36		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		325		ps
odc	Output Duty Cycle			50		%

NOTE 1: Please refer to the Phase Noise Plots following this section.

TABLE 5B. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = 2.5V\pm5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL = 1		312.5		MHz
		F_SEL = 0		625		MHz
$t$jit(Ø)	RMS Phase Jitter (Random); NOTE 1	312.5MHz @ Integration Range: 1.875MHz - 20MHz		0.38		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		325		ps
odc	Output Duty Cycle			50		%

NOTE 1: Please refer to the Phase Noise Plots following this section.

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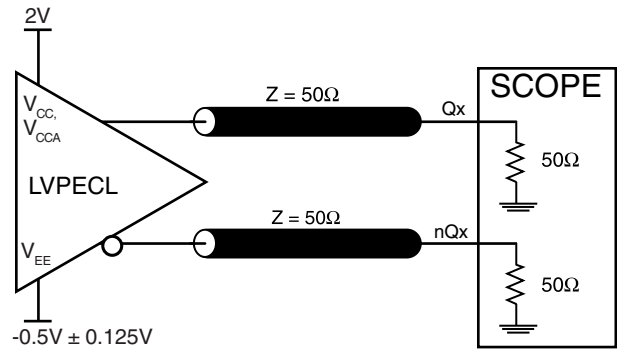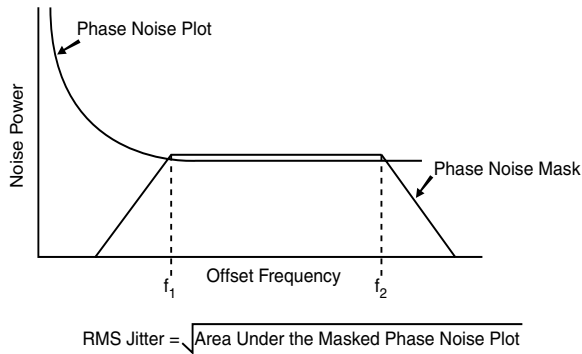## LVPECL Clock Generator

Typical Phase Noise at 312.5MHz (3.3V)

10GigE Filter

312.5MHz
RMS Phase Jitter (Random)
1.875Mhz to 20MHz = 0.36ps (typical)

Raw Phase Noise Data

**Phase Noise Result by adding
10GigE Filter to raw data**

Noise Power $\dfrac{dBc}{Hz}$

Offset Frequency

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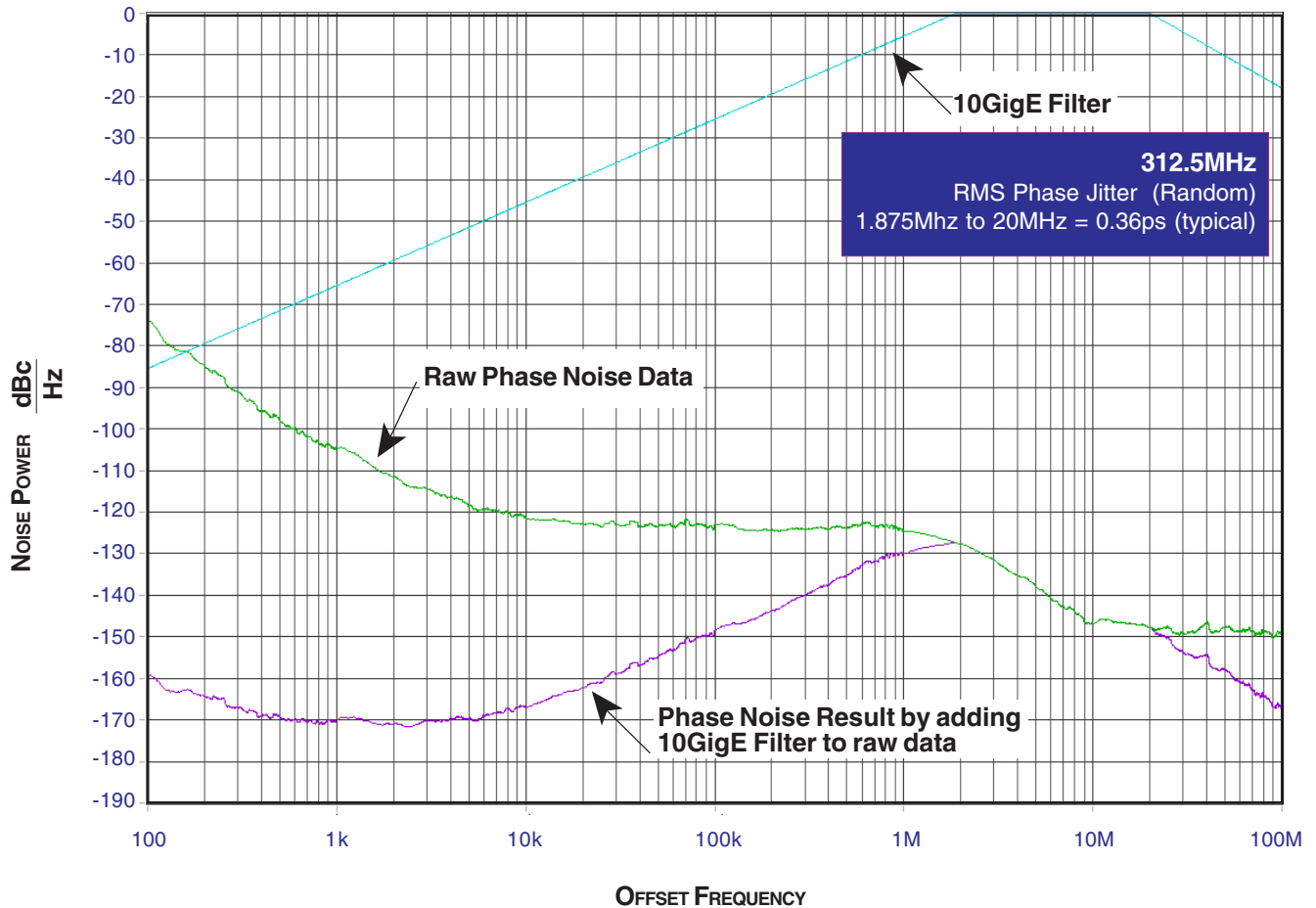
PARAMETER MEASUREMENT INFORMATION
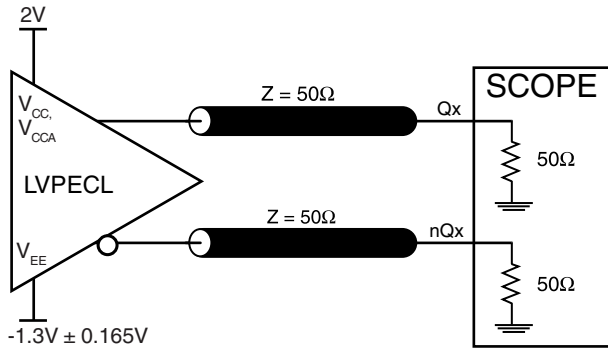
LVPECL 3.3V OUTPUT LOAD AC TEST CIRCUIT

LVPECL 2.5V OUTPUT LOAD AC TEST CIRCUIT

$$\text{RMS Jitter} = \sqrt{\text{Area Under the Masked Phase Noise Plot}}$$

RMS PHASE JITTER

$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$
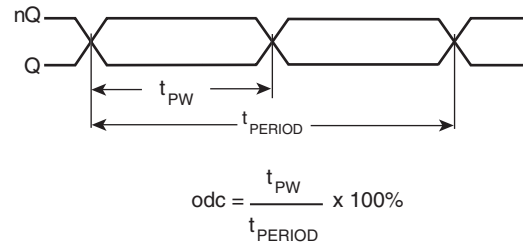
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

OUTPUT RISE/FALL TIME

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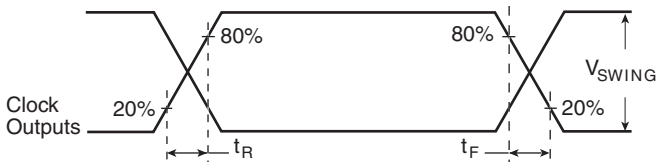
APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS843251I-12 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC} and V_{CCA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA} pin. The 10Ω resistor can also be replaced by a ferrite bead.
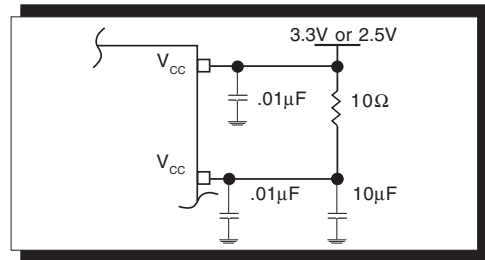
FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS843251I-12 has been characterized with 18pF parallel resonant crystals. The capacitor values (TBD), C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.
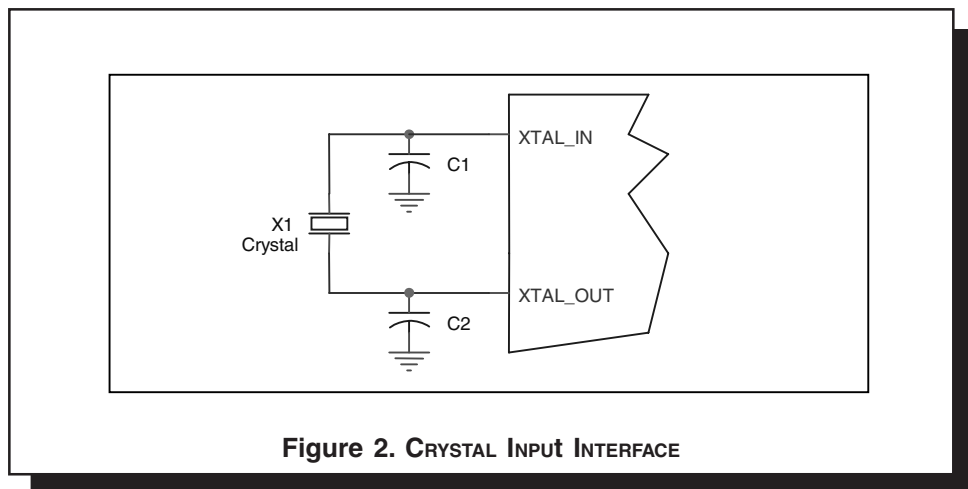

Figure 2. CRYSTAL INPUT INTERFACE

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TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

$$RTT = \left[\frac{1}{((V_{OH} + V_{OL}) / (V_{CC} - 2)) - 2} \right] Z_o$$
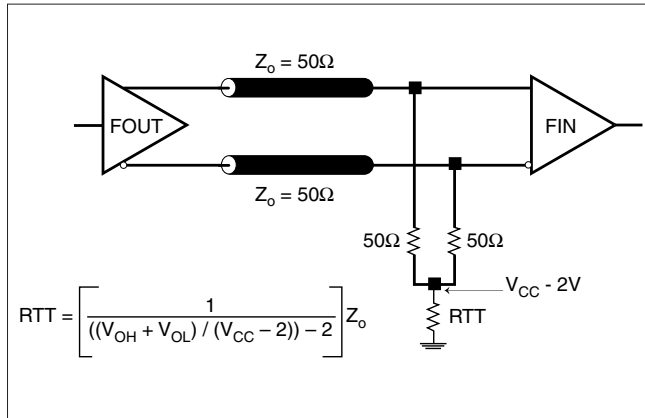
FIGURE 3A. LVPECL OUTPUT TERMINATION

FIGURE 3B. LVPECL OUTPUT TERMINATION

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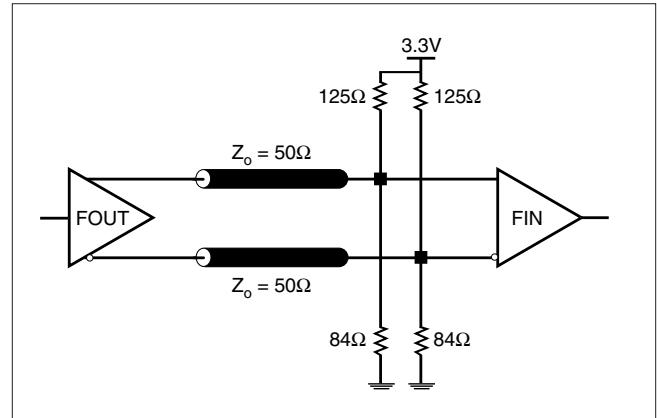Systems, Inc.

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TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 4A and *Figure 4B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 4B can be eliminated and the termination is shown in *Figure 4C*.
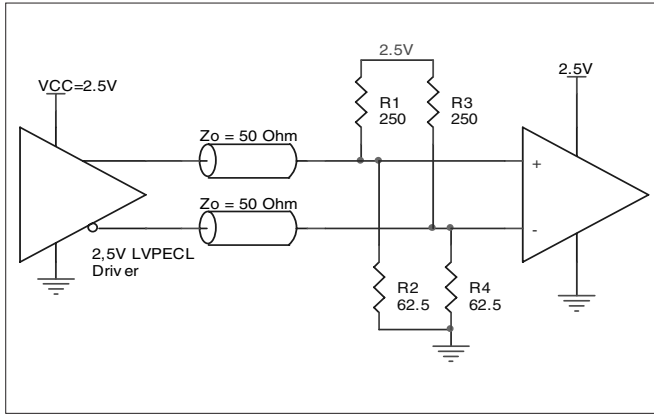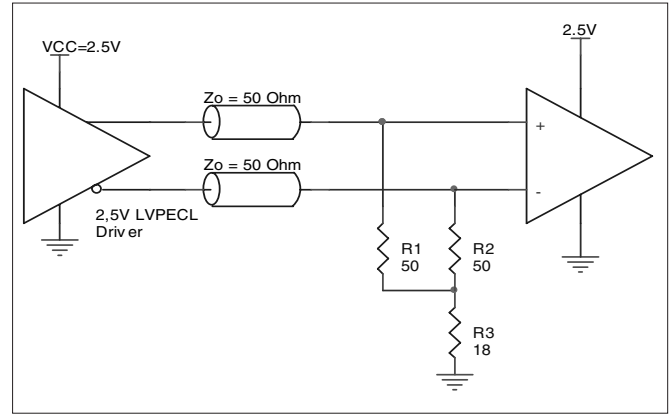
FIGURE 4A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

FIGURE 4B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE
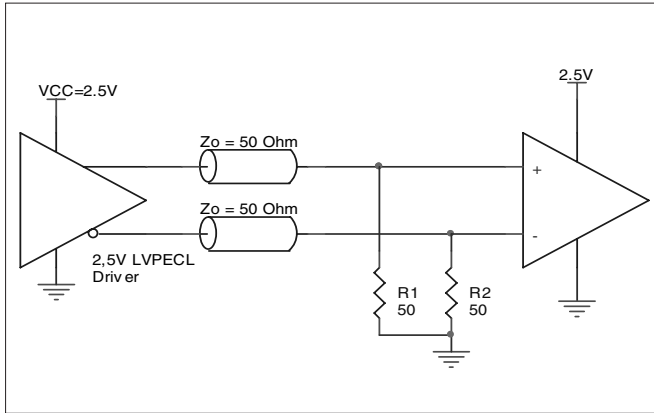
FIGURE 4C. 2.5V LVPECL TERMINATION EXAMPLE

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RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

TRANSISTOR COUNT

The transistor count for ICS843251I-12 is: 2377

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PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP
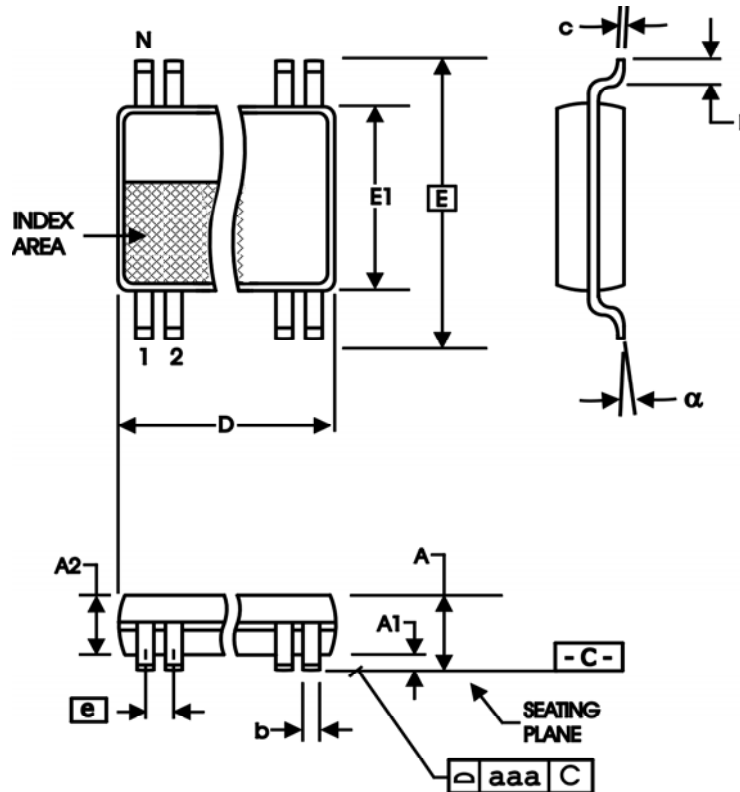
TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

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TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS843251BGI-12	TBD	8 Lead TSSOP	tube	-40°C to 85°C
ICS843251BGI-12T	TBD	8 Lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS843251BGI-12LF	BI12L	8 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS843251BGI-12FT	BI12L	8 Lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.