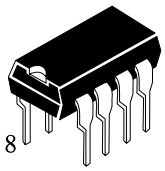
Low Power J-FET DUAL OPERATIONAL AMPLIFIERS

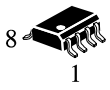
IL072

The IL072 are high speed J–FET input dual operational amplifiers incorporating well matched, high voltage J–FET and bipolar transistors in a monolithic integrated circuit.
The devices feature high slew rates, low input bias and offset current, and low offset voltage temperature coefficient.

- Low power consumption
- Wide common-mode and differential voltage range
- Low input bias and offset currents
- Low noise e_n=18 nV/√Hz (typ)
- Output short-circuit protection
- High input impedance J-FET input stage
- Low harmonic distortion: 0.01% (typ)
- Internal frequency compensation
- Latch up free operation
- High slew rate: 13 V/μs (typ)



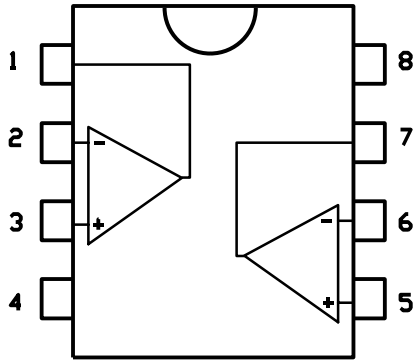
N SUFFIX
PLASTIC



D SUFFIX
SOIC

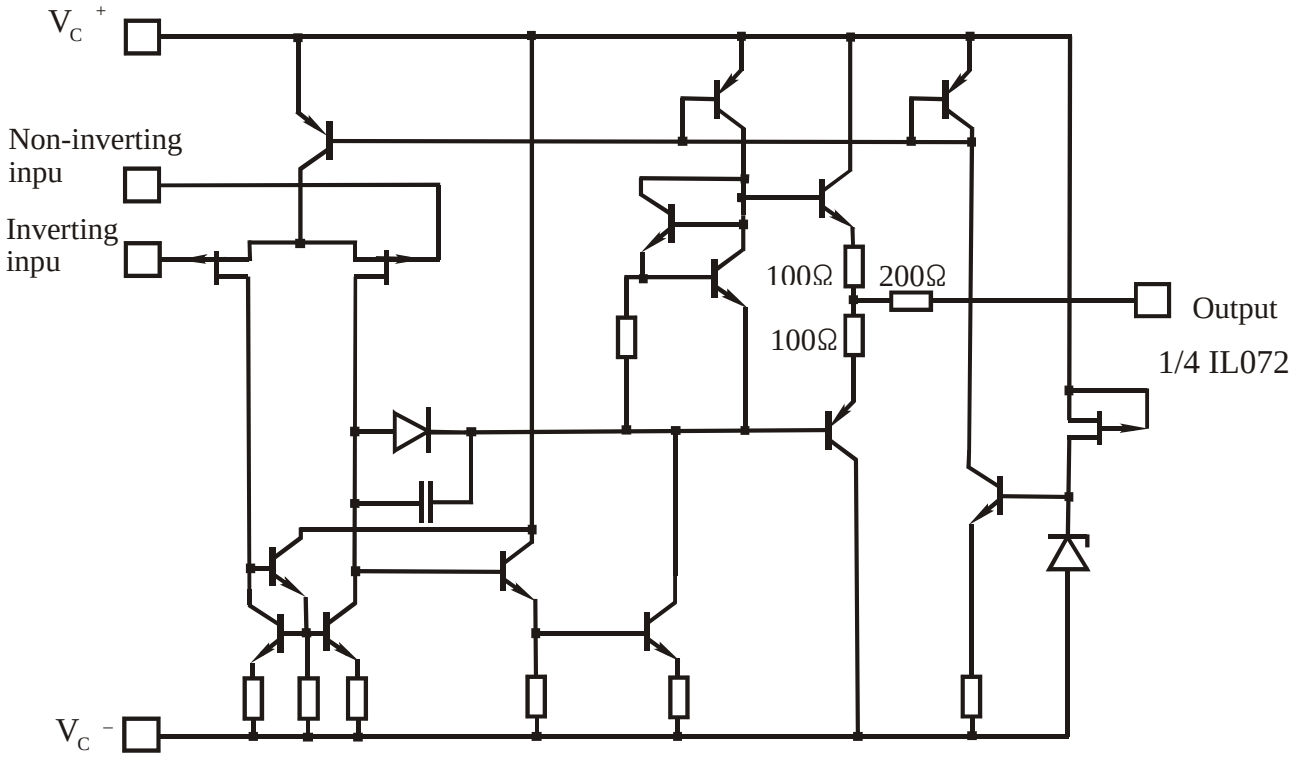
ORDERING INFORMATION
IL072N Plastic
IL072D SOIC
T_A = -40° to 85° C for package

Pin Connections (top view)



1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC} -
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC} +

SCHEMATIC DIAGRAM



MAXIMUM RATING

Symbol	Parameter	IL072	Unit
V_{CC}	Supply Voltage – (note 1)	±18	V
V_i	Input Voltage – (note 3)	±15	V
V_{id}	Differential Input Voltage – (note 2)	±30	V
P_{tot}	Power Dissipation	680	mW
	Output Short-Circuit Duration (Note 4)	Infinite	
T_{oper}	Operating Free-Air Temperature Range	-40 to 85	^{0}C
T_{stg}	Storage Temperature Range	-65 to +150	^{0}C

Notes.

1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.
2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

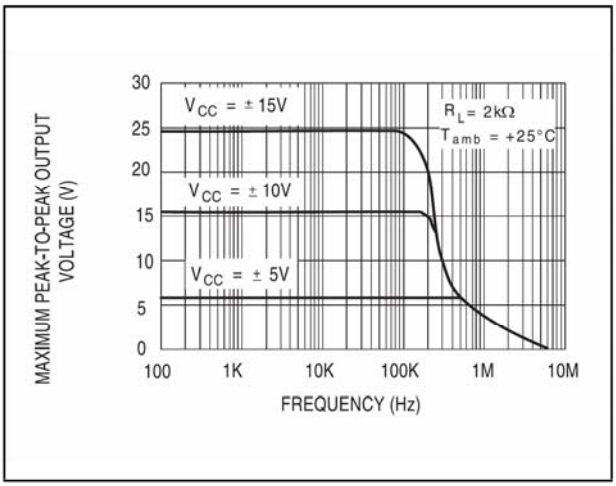
ELECTRICAL CHARACTERISTICS

V_{CC} = ± 15V, T_{AMB} = 25°C (unless otherwise specified)

Symbol	ParametersI	IL072			Unit
		Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage (R_S = 50Ω, V_0=0) T_{amb} =25°C $T_{min.} \le T_{amb.} \le T_{max.}$		3	10 13	mV
DV_{IO}	Input Offset Voltage Drift		18		µV/°C
I_{IO}	Input Offset Current* T_{amb} =25°C $T_{min.} \le T_{amb.} \le T_{max.}$		5	100 10	pA nA
I_{IB}	Input Bias Current* T_{amb} =25°C $T_{min.} \le T_{amb.} \le T_{max.}$		65	200 20	pA nA
A_{VD}	Large Signal Voltage Gain (R_L = 2kΩ, V_O =± 10V) T_{amb} =25°C $T_{min.} \le T_{amb.} \le T_{max.}$	25 15	200		V/mV
SVR	Supply Voltage Rejection Ratio (R_S = 50Ω, V_0=0) T_{amb} =25°C $T_{min.} \le T_{amb.} \le T_{max.}$	70 70	86		dB
I_{CC}	Supply Current (Per Amplifier) T_{amb} =25°C $T_{min.} \le T_{amb.} \le T_{max}$		1.4	2.5 2.5	mA
V_{ICM}	Input Common Mode Voltage Range	±11	+15 -12		V
CMR	Common Mode Rejection Ratio (R_S = 50Ω, V_0=0) T_{amb} =25°C	70	86		dB
$\pm V_{OPP}$	Output Voltage Swing T_{amb} =25°C R_L=10kΩ $T_{min.} \le T_{amb.} \le T_{max.}$ R_L=2kΩ R_L=10kΩ	12 10 12	13.5		V
SR	Slew Rate (V_i = 10V, R_L= 2kΩ, C_L = 100pF, T_{amb} =25°C, unity gain)	8	13		V/µs
t_r	Rise Time (V_i = 20mV, R_L= 2kΩ, C_L =100pF, T_{amb} =25°C, unity gain)		0.1		µs
K_{OV}	Overshoot (V_i = 20mV, R_L= 2kΩ, C_L =100pF, T_{amb} =25°C, unity gain)		20		%
GBP	Gain Bandwidth Product		3		MHz
R_I	Input Resistance		10^{12}		Ω
THD	Total Harmonic Distortion (f=1kHz, R_L= 2kΩ, T_{amb} =25°C)		0.01		%
e_n	Equivalent input Noise Voltage (R_S = 100Ω, f = 1KHz)		18		$\frac{nV}{\sqrt{Hz}}$
V_{O1}/V_{O2}	Channel Separation (A_V =100)		120		dB

* The Input bias currents are junction leakage currents which approximately double for every 10^0C increase in the junction temperature.

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE versus FREQUENCY



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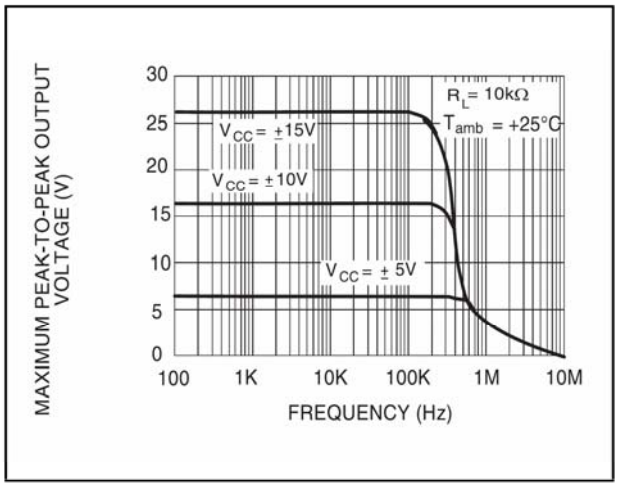
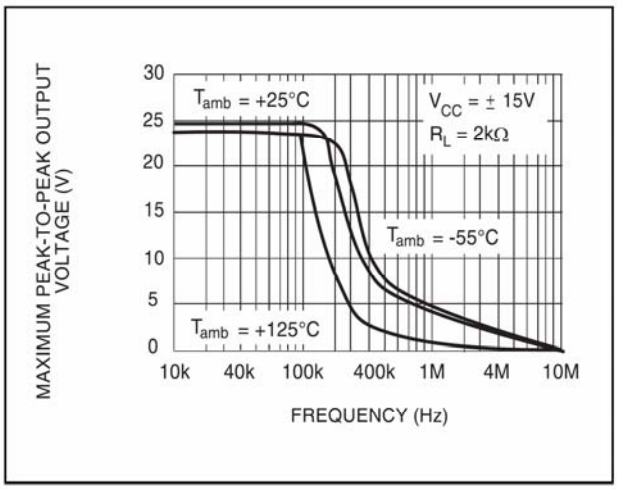
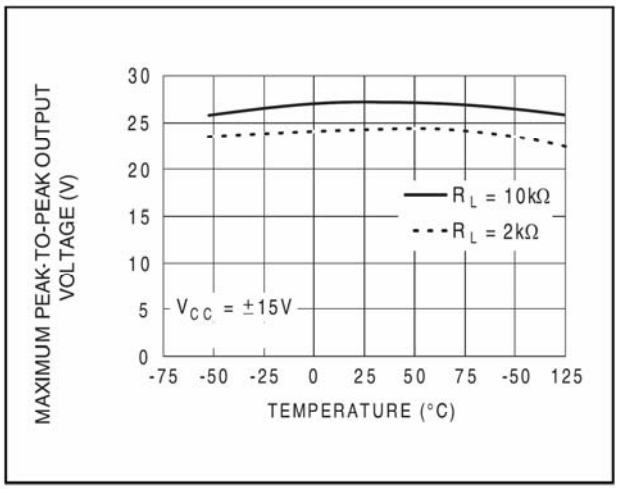


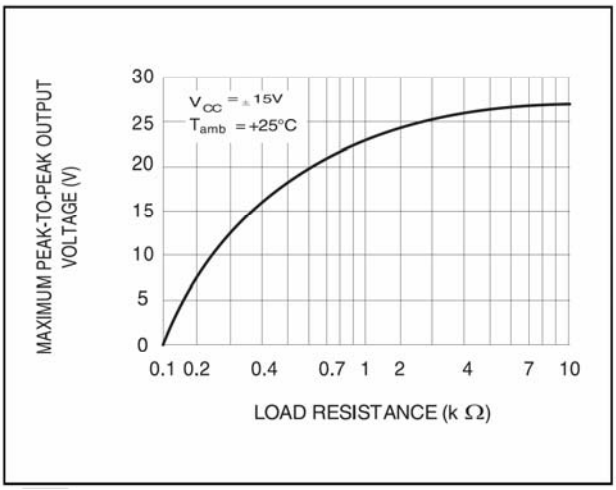
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE versus FREQUENCY



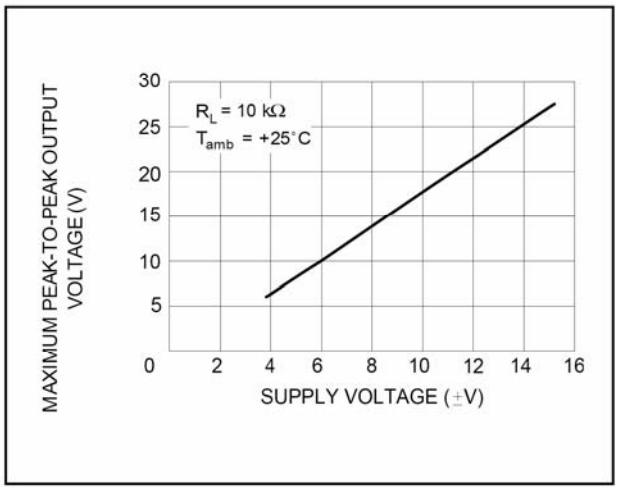
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE versus FREE AIR TEMP.



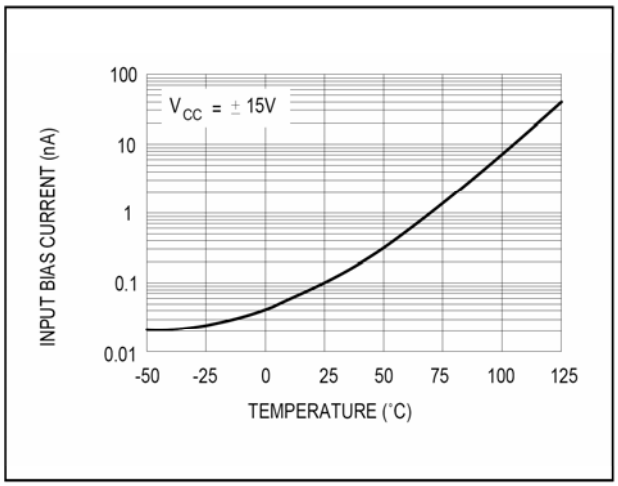
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE versus LOAD RESISTANCE



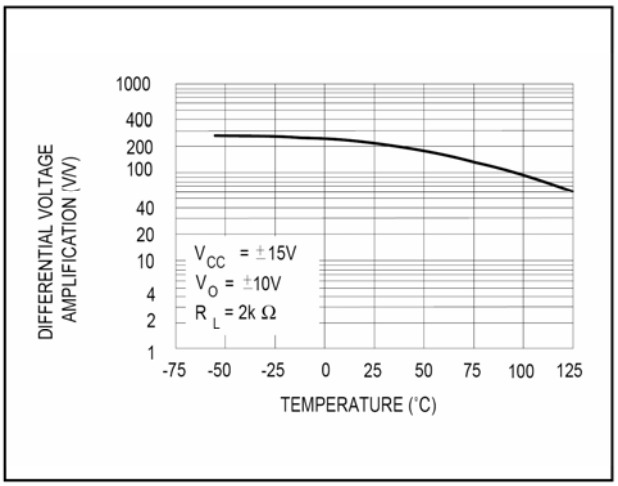
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE versus SUPPLY VOLTAGE



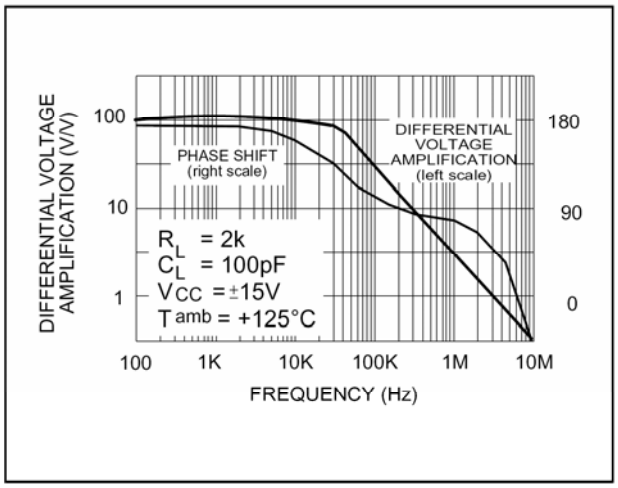
INPUT BIAS CURRENT versus FREE AIR TEMPERATURE



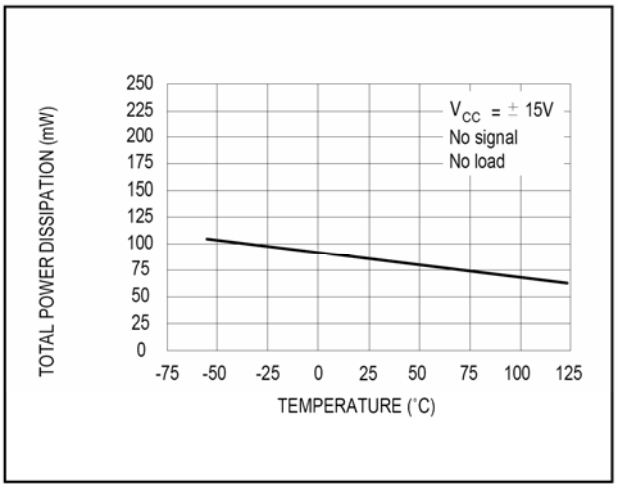
LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION versus FREE AIR TEMP.



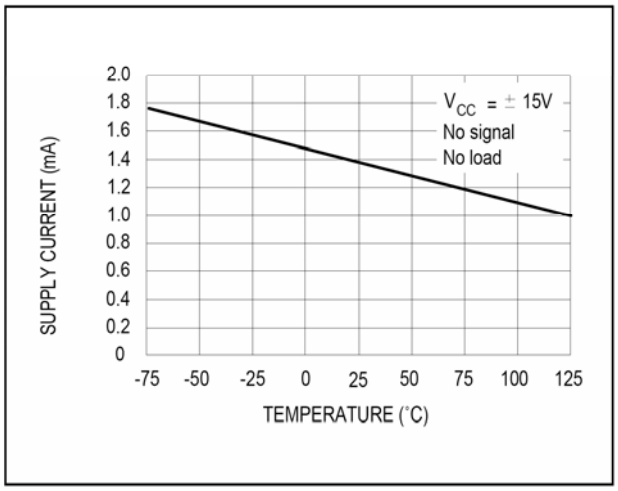
LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT versus FREQUENCY



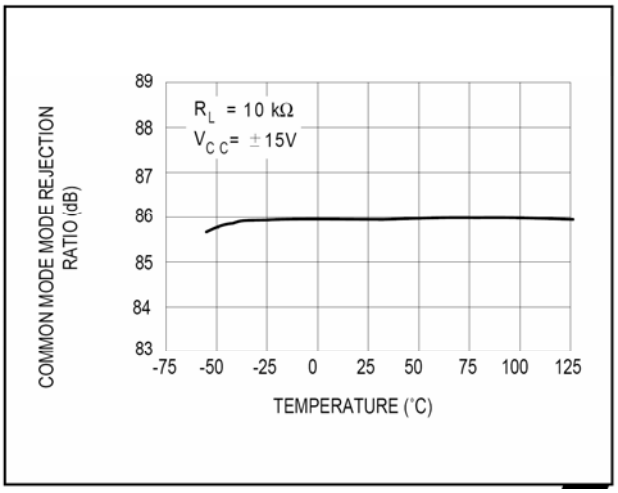
TOTAL POWER DISSIPATION versus FREE AIR TEMPERATURE



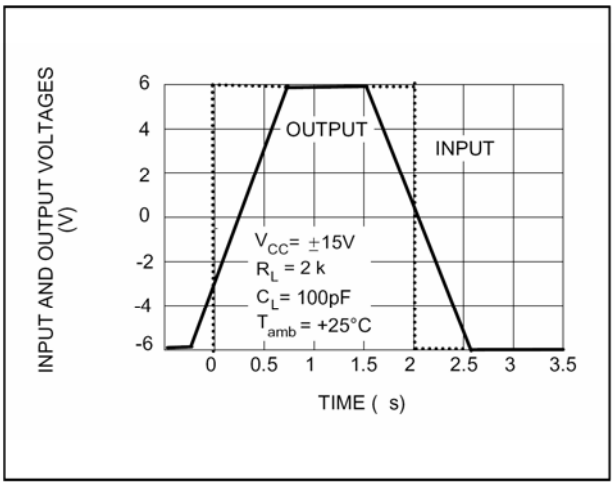
SUPPLY CURRENT PER AMPLIFIER versus FREE AIR TEMPERATURE



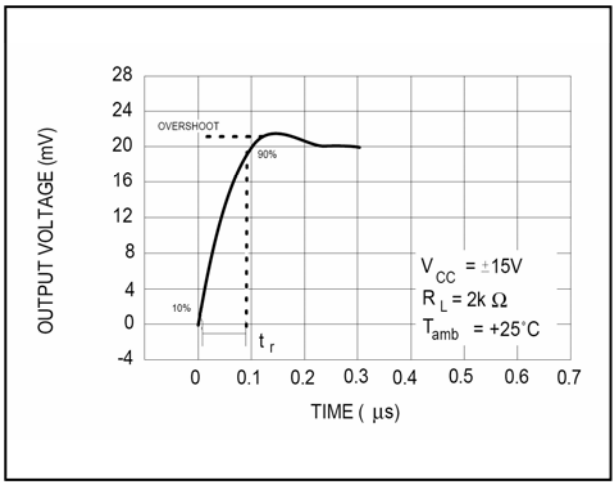
COMMON MODE REJECTION RATIO versus FREE AIR TEMPERATURE



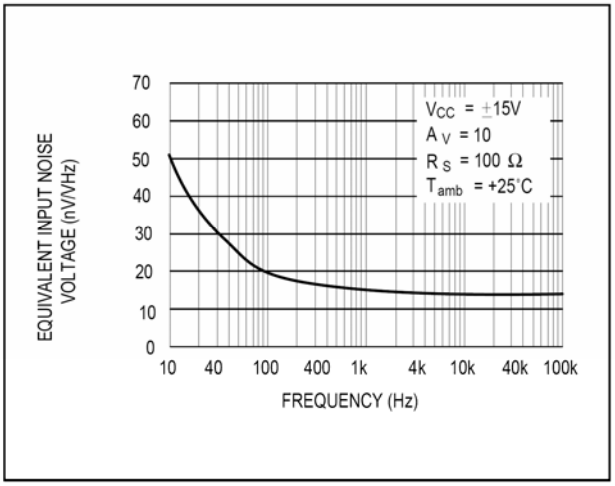
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



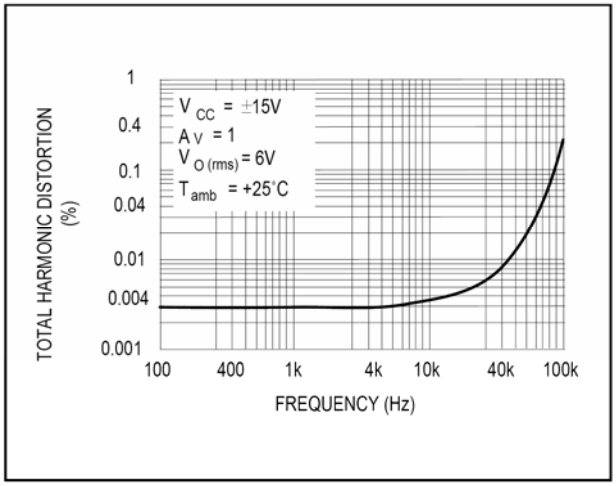
OUTPUT VOLTAGE versus ELAPSED TIME



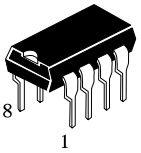
EQUIVALENT INPUT NOISE VOLTAGE versus FREQUENCY

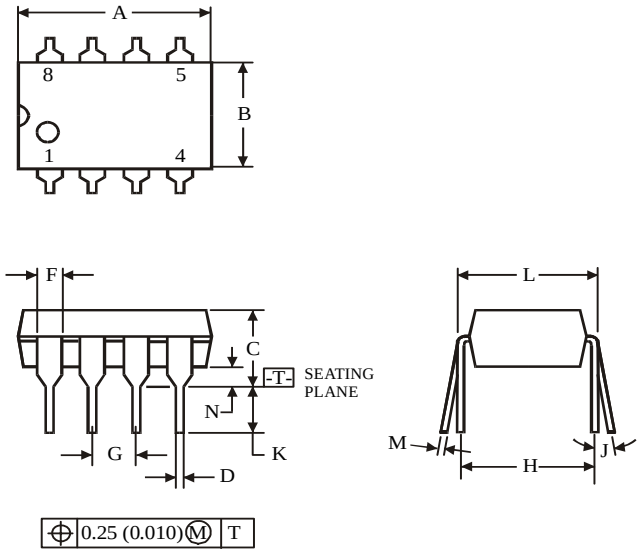


TOTAL HARMONIC DISTORTION versus FREQUENCY



N SUFFIX PLASTIC DIP
(MS – 001BA)



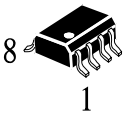


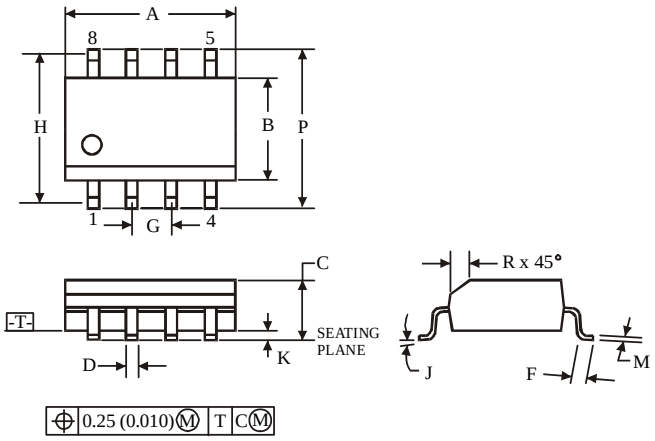
	Dimension, mm	
Symbol	**MIN**	**MAX**
A	8.51	10.16
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

NOTES:

1. Dimensions “A”, “B” do not include mold flash or protrusions.
   Maximum mold flash or protrusions 0.25 mm (0.010) per side.

D SUFFIX SOIC
(MS - 012AA)





	Dimension, mm	
Symbol	**MIN**	**MAX**
A	4.8	5
B	3.8	4
C	1.35	1.75
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	5.72	
J	0°	8°
K	0.1	0.25
M	0.19	0.25
P	5.8	6.2
R	0.25	0.5

NOTES:

1. Dimensions A and B do not include mold flash or protrusion.
2. Maximum mold flash or protrusion 0.15 mm (0.006) per side
   for A; for B – 0.25 mm (0.010) per side.