OCTAL 3-STATE BUS TRANSCEIVERS AND D FLIP-FLOPS

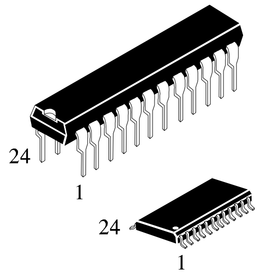
High-Performance Silicon-Gate CMOS

The IN74HC652 is identical in pinout to the LS/ALS652. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

These devices consists of bus transceiver circuits, D-type flip-flop, and control circuitry arranged for multiplex transmission of data directly from the data bus or from the internal storage registers. Direction and Output Enable are provided to select the read-time or stored data function. Data on the A or B Data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (A-to-B Clock or B-to-A Clock) regardless of the select or enable or enable control pins. When A-to-B Source and B-to-A Source are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simulta-neously enabling Direction and Output Enable. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The IN74HC652 has noninverted outputs.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices



N SUFFIX PLASTIC

DW SUFFIX SOIC

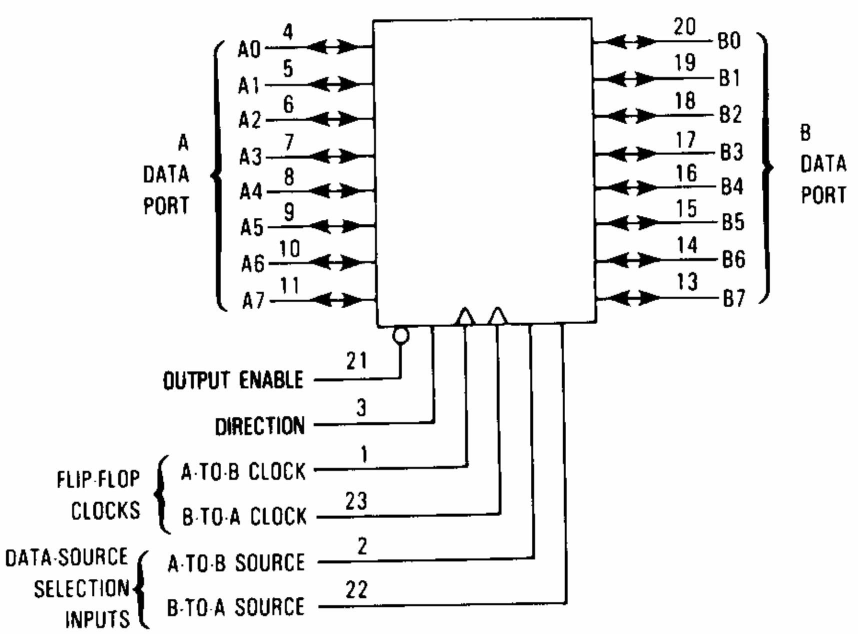
ORDERING INFORMATION

IN74HC651N Plastic
IN74HC651DW SOIC
T_A = -55° to 125° C for all packages

PIN ASSIGNMENT

A-TO-B CLOCK	1	24	V_{CC}
A-TO-B SOURCE	2	23	B-TO-A CLOCK
DIRECTION	3	22	B-TO-A SOURCE
A0	4	21	OUTPUT ENABLE
A1	5	20	B0
A2	6	19	B1
A3	7	18	B2
A4	8	17	B3
A5	9	16	B4
A6	10	15	B5
A7	11	14	B6
GND	12	13	B7

LOGIC DIAGRAM



PIN 24=V_{CC}
PIN 12 = GND

INTEGRAL

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V_{CC} +1.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figures2,3) V_{CC} =2.0 V V_{CC} =4.5 V V_{CC} =6.0 V	0 0 0	1000 500 400	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low - Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0 4.5 6.0	0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 6.0$ mA $\lvert I_{OUT}\rvert \leq 7.8$ mA	 4.5 6.0	 3.98 5.48	 3.84 5.34	 3.7 5.2	
V_{OL}	Maximum Low-Level Output Voltage	$V_{IN}= V_{IL}$ or V_{IH} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 6.0$ mA $\lvert I_{OUT}\rvert \leq 7.8$ mA)	 4.5 6.0	 0.26 0.26	 0.33 0.33	 0.4 0.4	
I_{IN}	Maximum Input Leakage Current	$V_{IN}=V_{CC}$ or GND (Pins 1,2,3,21,22,and 23)	6.0	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{IN}= V_{IL}$ or V_{IH} $V_{OUT}=V_{CC}$ or GND, I/O Pins	6.0	±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$	6.0	8.0	80	160	μA

AC ELECTRICAL CHARACTERISTICS(C_L=50pF,Input t_r=t_f=6.0 ns)

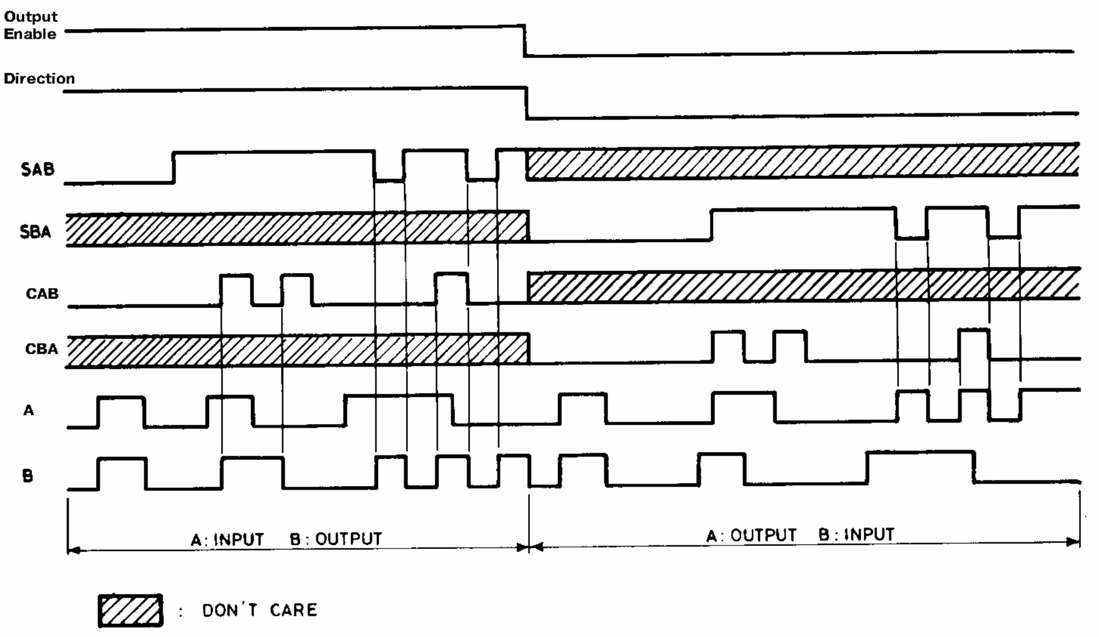
Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125 °C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Output B (or Input B to Output A) (Figures 2,3 and 9)	2.0 4.5 6.0	180 36 31	225 45 38	270 54 46	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A-to-B Clock to Output B (or B-to-A Clock to Output A) (Figures 1 and 9)	2.0 4.5 6.0	240 48 41	300 60 51	360 72 61	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A-to-B Source to Output B (or B-to-A Source to Output A) (Figures 4 and 9)	2.0 4.5 6.0	220 44 37	275 55 47	330 66 56	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay , Direction or Output Enable to Output A or B (Figures 5,6 and 10)	2.0 4.5 6.0	170 34 29	215 43 37	255 51 43	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay , Direction or Output Enable to Output A or B (Figures 5,6 and 10)	2.0 4.5 6.0	180 36 31	225 45 38	270 54 46	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figure 2)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C_{IN}	Maximum Input Capacitance	-	10	10	10	pF
C_{OUT}	Maximum Three-State I/O Capacitance (Output in High-Impedance State	-	15	15	15	pF

C_{PD}	Power Dissipation Capacitance (Per Channel) Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	Typical @25°C,V_{CC}=5.0 V 60	pF

TIMING REQUIREMENTS(Input t_r=t_f=6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25 °C to-55°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, Input A to A-to-B Clock (or Input B to B-to-A Clock) (Figure 7)	2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns
t_h	Minimum Hold Time, A-to-B Clock to Input A (or B-to-A Clock to Input B) (Figure 7)	2.0 4.5 6.0	25 5 5	30 6 5	40 8 7	ns
t_w	Minimum Pulse Width, A-to-B Clock (or B-to-A Clock) (Figure 7)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figures 2 and 3)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

TIMING DIAGRAM



FUNCTION TABLE

Dir.	OE	CAB	CBA	SAB	SBA	A	B	FUNCTION
						INPUTS	INPUTS	Both the A bus and the B bus are inputs.
L	H	X	X	X	X	Z	Z	The output functions of the A and B bus are disabled.
		$\uparrow$	$\uparrow$	X	X	INPUTS	INPUTS	Both the A and B bus are used for inputs to the internal flip-flops. Data at the bus will be stored on low to high transition of the clock inputs.
						OUTPUTS	INPUTS	The A bus are outputs and the B bus are inputs.
		X*	X	X	L	L H	L H	The data at the B bus are displayed at the A bus.
L	L	X*	$\uparrow$	X	L	L H	L H	The data at the B bus are displayed at the A bus. The data of the B bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X*	X	X	H	Qn	X	The data stored to the internal flip-flops, are displayed at the A bus.
		X*	$\uparrow$	X	H	H L	H L	The data at the B bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the A bus.
						INPUTS	OUTPUTS	The A bus are inputs and the B bus are outputs.
		X	X*	L	X	L H	L H	The data at the A bus are displayed at the B bus.
H	H	$\uparrow$	X*	L	X	L H	L H	The data at the B bus are displayed at the A bus. The data of the B bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X	X*	H	X	X	Qn	The data stored to the internal flip-flops are displayed at the B bus.
		$\uparrow$	X*	H	X	L H	L H	The data at the A bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the B bus.
						OUTPUTS	OUTPUTS	Both the A bus and the B bus are outputs
H	L	X	X	H	H	Qn	Qn	The data stored to the internal flip-flops are displayed at the A and B bus respectively.
		$\uparrow$	$\uparrow$	H	H	Qn	Qn	The output at the A bus are displayed at the B bus, the output at the B bus are displayed at the A bus respec.

X : DON'T CARE
Z : HIGH IMPEDANCE
Qn : THE DATA STORED TO THE INTERNAL FLIP-FLOPS BY MOST RECENT LOW TO HIGH TRANSITION OF THE CLOCK INPUTS
* : THE DATA AT THE A AND B BUS WILL BE STORED TO THE INTERNAL FLIP-FLOPS ON EVERY LOW TO TRANSITION OF THE CLOCK INPUTS

SWITCHING DIAGRAMS

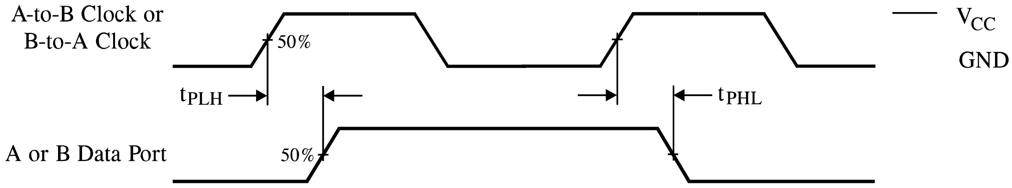


Figure 1. Switching Waveforms

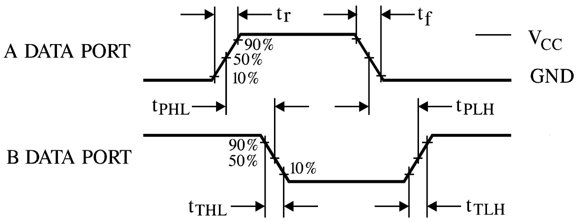


Figure 2. A Data Port = Input, B Data Port = Output

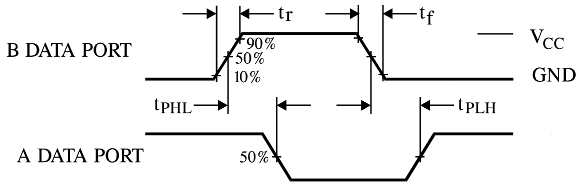


Figure 3. A Data Port = Output, B Data Port = Input

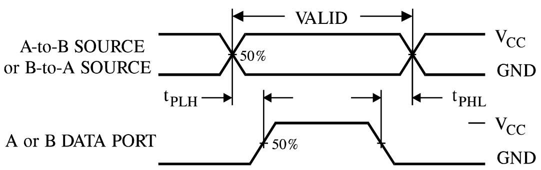


Figure 4. Switching Waveforms

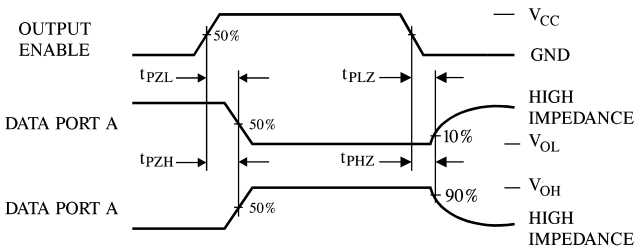


Figure 5. Switching Waveforms

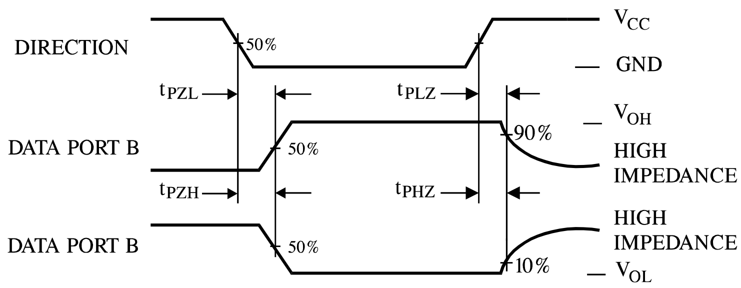
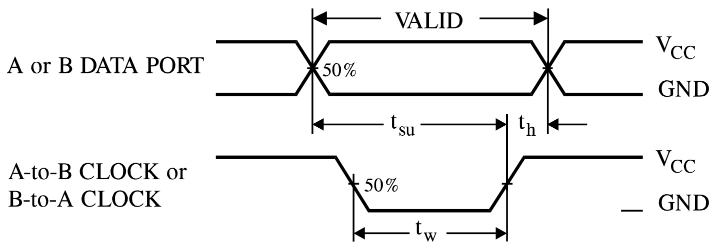


Figure 6. Switching Waveforms



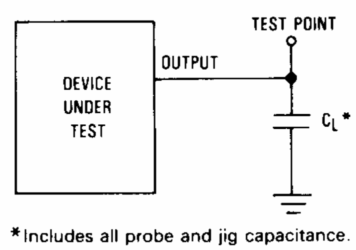


Figure 9. Test Circuit

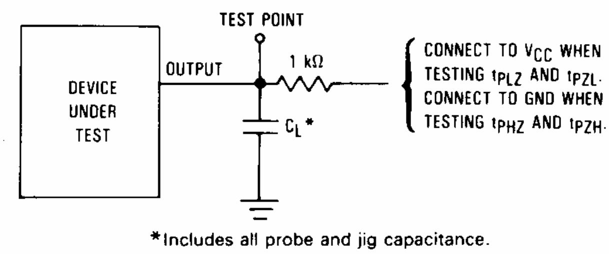


Figure 10. Test Circuit

EXPANDED LOGIC DIAGRAM