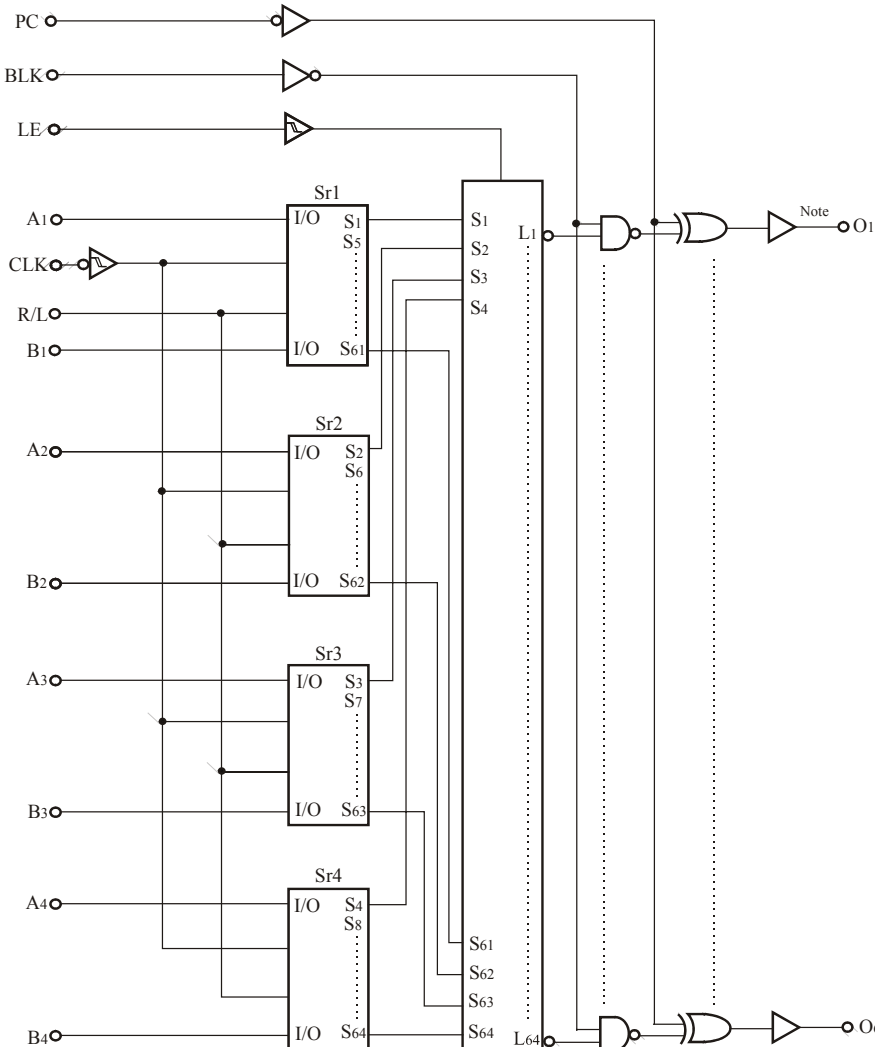
IND16337
64-BIT AC-PDP DRIVER

The IND16337 is a high-voltage CMOS driver designed for flat display panels such as PDPs, VFDs and ELs. It consists of a 64-bit bi-directional shift register (16 bit □ 4 circuits), 64-bit latch and high-voltage CMOS driver. The logic block is designed to operate at 5-V power supply, enabling direct connection to a microcontroller. In addition, the IND16337 achieves low power dissipation by employing CMOS structure while having a high withstand voltage output (150 V, 40 mA MAX.)

FEATURES

- Built in four 16-bit bi-directional shift register circuits
- Data control with transfer clock (external) and latch
- High-speed data transfer (fmax. = 20 MHz MIN. at cascade connection)
- Wide operating temperature range (TA = –40 to +85°C)
- High withstand output voltage (150 V, 40 mA MAX.)
- 5-V CMOS input interface
- High withstand voltage CMOS structure
- Capable of reversing all driver outputs by PC pin

BLOCK DIAGRAM

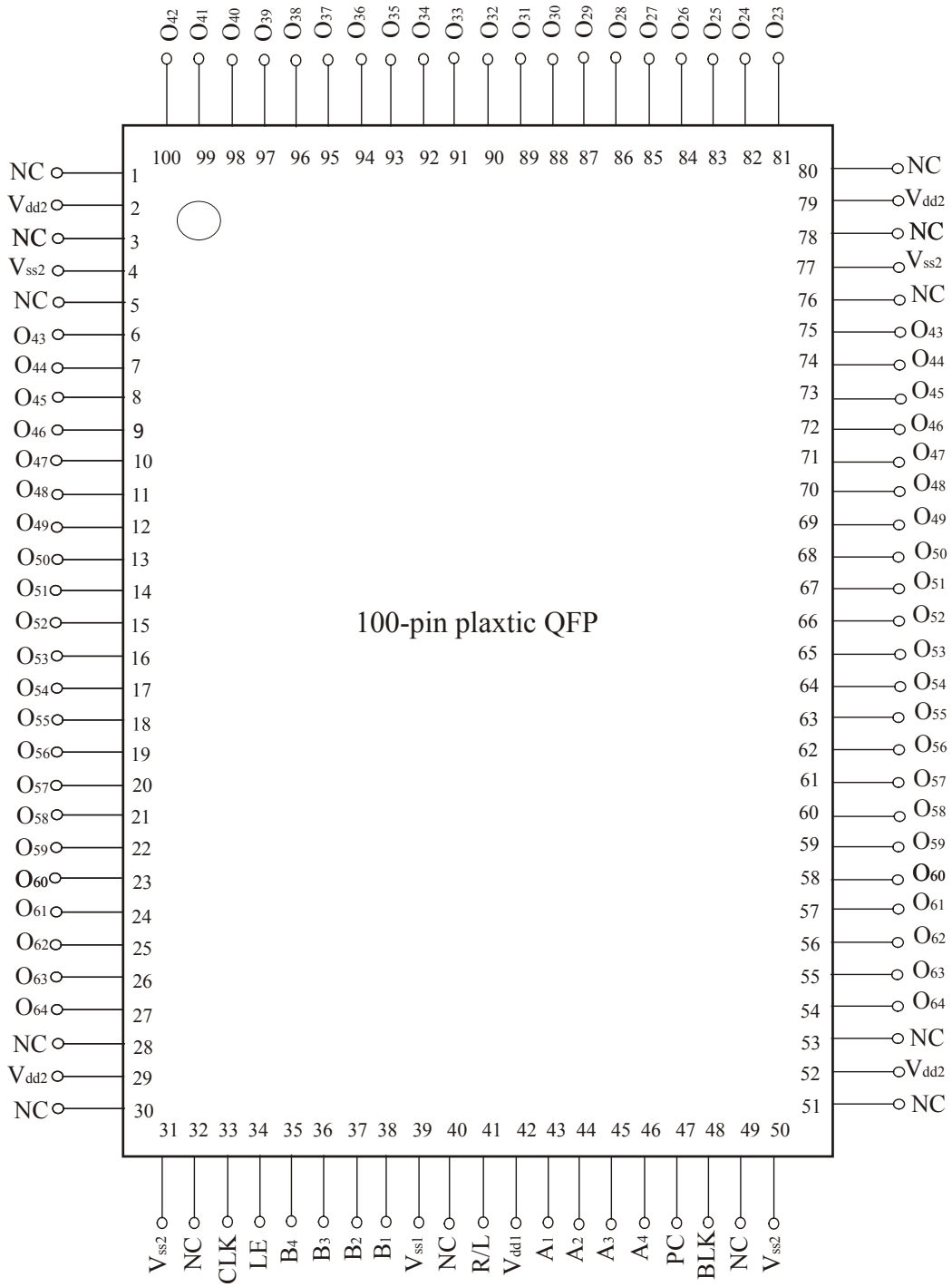


Note High withstand voltage CMOS driver, 150 V, ±40 mA (MAX.)

Korzhenevsky 12, Minsk, 220064, Republic of Belarus
Fax: +375 (17) 278 28 22
Tel: +375 (17) 278 49 09, 212 27 02
Tel/fax: +375 (17) 212 68 53
E-mail: office@bms.by
URL: www.bms.by

BELMICROSYSTEMS

PIN CONFIGURATION (Top View)



Cautions

1. Pin 40 is connected to the lead frame, and therefore must be left open.

2. Ensure that the V_{DD1}, V_{DD2}, V_{SS1} and V_{SS2} pins are all used, and that V_{SS1} and V_{SS2} are used at the same potential.

3. To prevent latch up breakdown, the power should be turned on in the order V_{DD1}, logic signal, V_{DD2}. It should be turned off in the opposite order.

PIN DESCRIPTION

Symbol	Pin Name	Pin Number	Description
PC	Polarity change input	47	PC = L: All driver output invert
BLK	Blank input	48	BLK = H: All output = H or L
LE	Latch enable input	34	Automatically executes latch by setting High at rising edgeof the clock
A1 to A4	RIGHT data input/output	43 to 46	When R/L = H, A1 to A4: Input B1 to B4: Output
B1 to B4	LEFT data input/output	38 to 35	When R/L = L, A1 to A4: Output B1 to B4:Input
CLK	Clock input	33	Shift executed on fall
R/L	Shift control input	41	Right shift mode when R/L = H SR1: A1 → S1 ··· S61 → B1 (Same direction for SR2·SR4) Left shift mode when R/L = L SR1: B1 → S61 ··· S1 → A1 (Same direction for SR2·SR4)
O1 to O64	High withstand voltage output	54 to 75, 81 to 100, 6 to 27	130 V, 40 mA MAX.
V_{DD1}	Power supply for logic block	42	5 V ±10%
V_{DD2}	Power supply for driver block	2, 29, 52, 79	30 to 130 V
V_{SS1}	Logic GND	39	Connect to system GND
V_{SS2}	Driver GND	4, 31, 50, 77	Connect to system GND
NC	Non-connection	1, 3, 5, 28, 30, 32, 40, 49, 51, 53, 76, 78, 80	Non-connection Ensure that pin 40 is left open.

TRUTH TABLE 1 (Shift Register Block)

Input		Output		Shift Register
R/L	CLK	A	B	
H	↓	Input	Output **Note 1**	Right shift execution
H	H or L		Output	Hold
L	↓	Output **Note 2**	Input	Left shift execution
L	H or L	Output		Hold

Notes 1. The data of S57, S58, S59, S60 shifts to S61, S62, S63, S64 and is output from B1, B2, B3, B4 at the falling edge of the clock, respectively.

2. The data of S5, S6, S7, S8 shifts to S1, S2, S3, S4 and is output from A1, A2, A3, A4 at the falling edge of the clock, respectively.

TRUTH TABLE 2 (Latch Block)

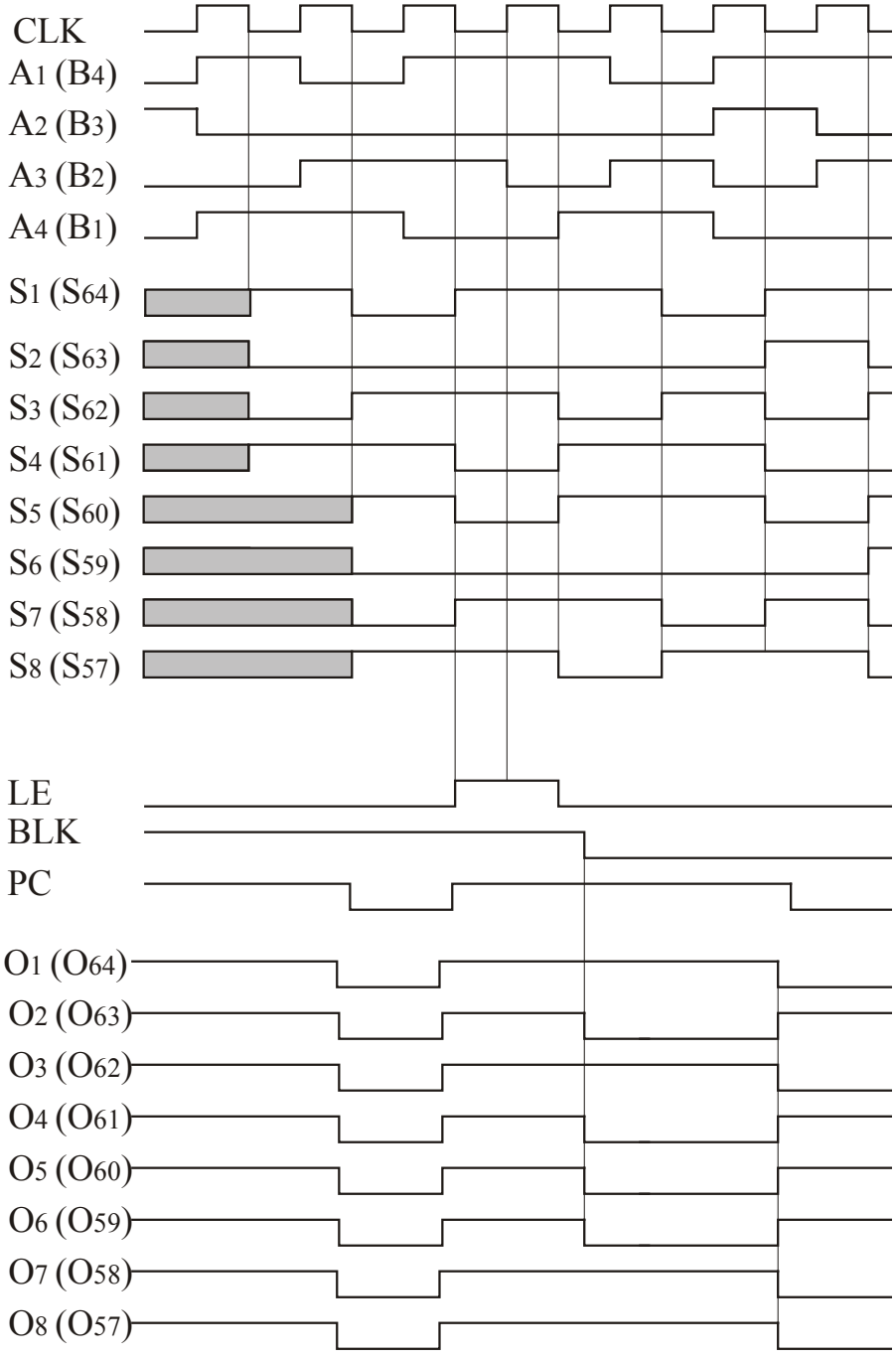
LE	CLK	Output State of Latch Block (Ln)
H	↑	Latch Sn data and hold output data
	↓	Hold latch data
L	X	Hold latch data

TRUTH TABLE 3 (Driver Block)

Ln	BLK	PC	Output State of Driver Block
X	H	H	H (All driver outputs: H)
X	H	L	L (All driver outputs: L)
X	L	H	Output latch data (Ln)
X	L	L	Output reversed latch data (Ln)

X: H or L, H: High level, L: Low level

TIMING CHART (Right shift)



Remark Values in parentheses in the above chart are when R/L = L.

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ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Ratings	Unit
Logic Block Supply Voltage	V_{DD1}	–0.5 to +7.0	V
Driver Block Supply Voltage	V_{DD2}	–0.5 to +150	V
Logic Block Input Voltage	V_I	–0.5 to V_{DD1} + 0.5	V
Driver Block Output Current	I_{O2}	40	mA
Power Dissipation	P_D	1300[Note]	mW
Operating Ambient Temperature	T_A	–40 to +85	°C
Storage Temperature	Tstg	–65 to +150	°C

Note Derate at –13 mW/°C at T_A = 25°C or higher

RECOMMENDED OPERATING CONDITIONS (T_A = –40 to +85°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	MIN.	MAX.	Unit
Logic Block Supply Voltage	V_{DD1}	4.5	5.5	V
Driver Block Supply Voltage	V_{DD2}	30	130	V
High-Level Input Voltage	V_{IH}	0.8 V_{DD1}	V_{DD1}	V
Low-Level Input Voltage	V_{IL}	0	0.2 V_{DD1}	V
Driver Output Current	I_{OH2}		–30	mA
	I_{OL2}		+30	mA

ELECTRICAL SPECIFICATIONS

(T_A = 25°C, V_{DD1} = 5.0 V, V_{DD2} = 130 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
High-Level Output Voltage	V_{OH1}	Logic, I_{OH1} = –1.0 mA	0.9 V_{DD1}	V_{DD1}	V
Low-Level Output Voltage	V_{OL1}	Logic, I_{OL1} = 1.0 mA	0	0.1 V_{DD1}	V
High-Level Output Voltage	V_{OH21}	O_1 to O_{64}, I_{OH2} = –10 mA	123		V
	V_{OH22}	O_1 to O_{64}, I_{OH2} = –30 mA	110		V
Low-Level Output Voltage	V_{OL21}	O_1 to O_{64}, I_{OL2} = 10 mA		5.0	V
	V_{OL22}	O_1 to O_{64}, I_{OL2} = 30 mA		15	V
Input Leakage Current	I_{IL}	V_1 = V_{DD1} or V_{SS1}		±1.0	uA
High-Level Input Voltage	V_{IH}		0.8 V_{DD1}		V
Low-Level Input Voltage	V_{IL}			0.2 V_{DD1}	V
Static Current Dissipation	I_{DD1}	Logic, T_A = –40 to +85°C		100	uA
	I_{DD1}	Logic, T_A = 25°C		10	uA
	I_{DD2}	Driver, T_A = –40 to +85°C		1000	uA
	I_{DD2}	Driver, T_A = 25°C		100	uA

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SWITCHING CHARACTERISTICS

(T_A = 25°C, V_{DD1} = 5.0 V, V_{DD2} = 130 V, V_{SS1} = V_{SS2} = 0 V, logic C_L = 15 pF, driver C_L = 50 pF, t_r = t_f = 6.0 ns)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Transmission Delay Time	t_{PHL1}	CLK↓→A/B		40	ns
	t_{PLH1}			40	ns
	t_{PHL2}	CLK↑ (LE = H) → O_1 to O_{64}		180	ns
	t_{PLH2}			180	ns
	t_{PHL3}	BLK → O_1 to O_{64}		165	ns
	t_{PLH3}			165	ns
	t_{PHL4}	PC→ O_1 to O_{64}		160	ns
	t_{PLH4}			160	ns
Rise Time	t_{TLH}	O_1 to O_{64}		200	ns
Fall Time	t_{THL}	O_1 to O_{64}		200	ns
Maximum Clock Frequency	$f_{max.}$	When data is read, duty 50% T_A = –40 to +85°C V_{DD1} = 4.5 to 5.5 V	25		MHz
		When a cascade connection is made with a duty of 50% T_A = –40 to +85°C V_{DD1} = 4.5 to 5.5 V	20		MHz
Input Capacitance	C_I			15	pF

TIMMING REQUIREMENT

(T_A = –40 to +85°C, V_{DD1} = 4.5 to 5.5 V, V_{SS1} = V_{SS2} = 0 V, t_r = t_f = 6.0 ns)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Clock Pulse Width	PW_{CLK}		20		ns
Latch Enable Pulse Width	PW_{LE}		30		ns
Blank Pulse Width	PW_{BLK}		500		ns
PC Pulse Width	PW_{PC}		500		ns
Data Setup Time	t_{setup}		10		ns
Data Hold Time	t_{hold}		10		ns
Latch Enable Time 1	t_{LE1}		20		ns
Latch Enable Time 2	t_{LE2}		10		ns
Latch Enable Time 3	t_{LE3}		20		ns
Latch Enable Time 4	t_{LE4}		10		ns

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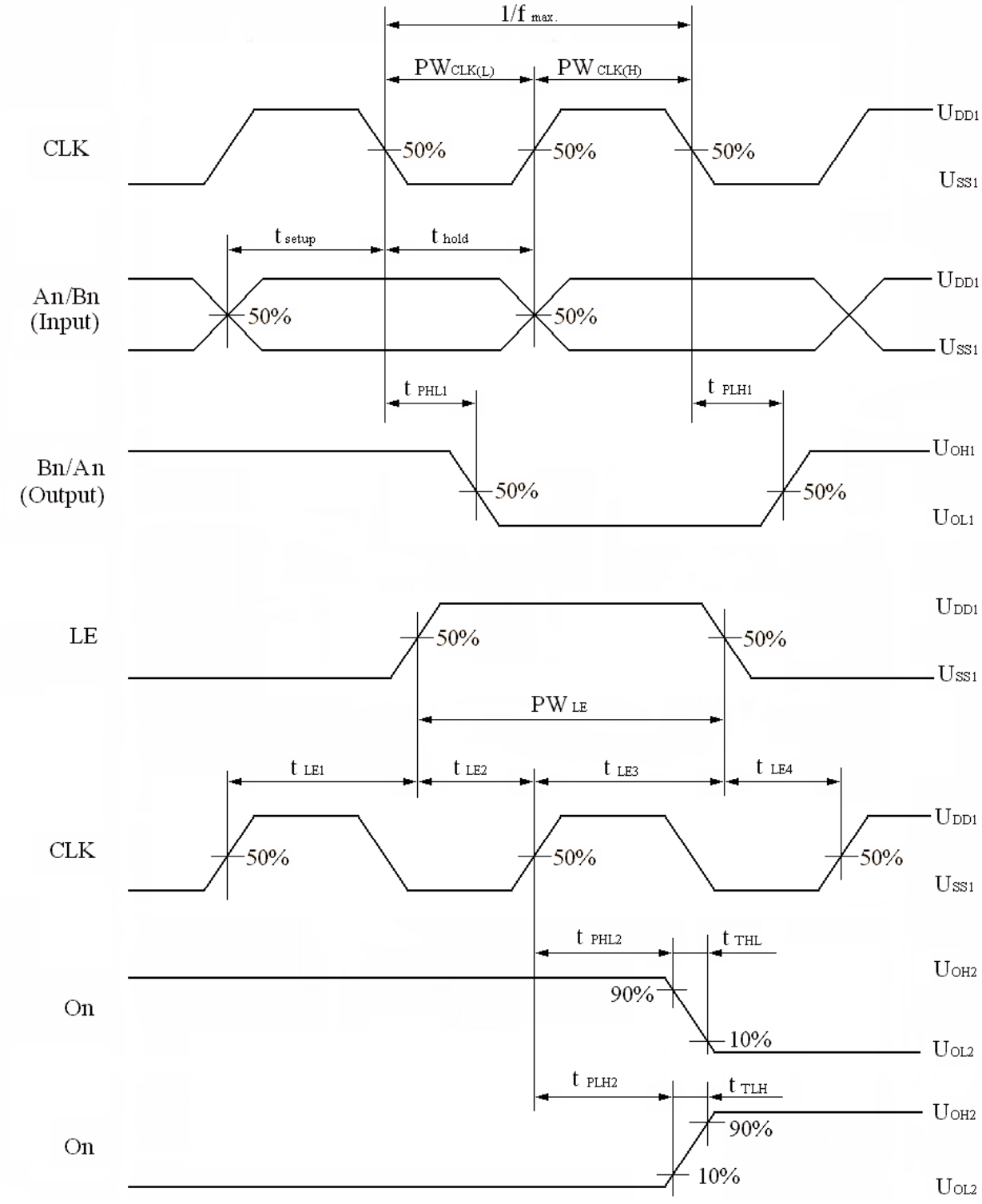
SWITCHING CHARACTERISTICS WAVEFORM



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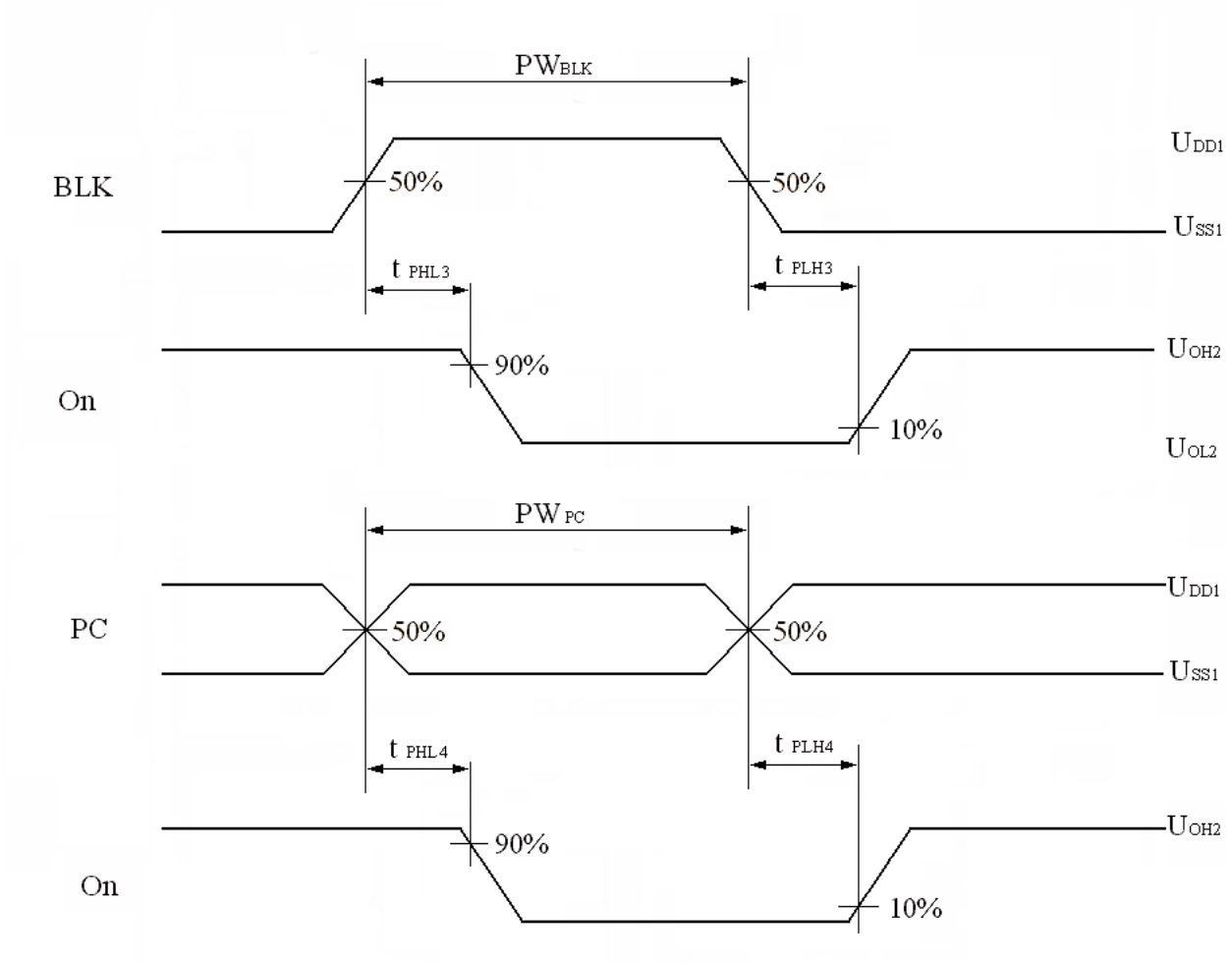

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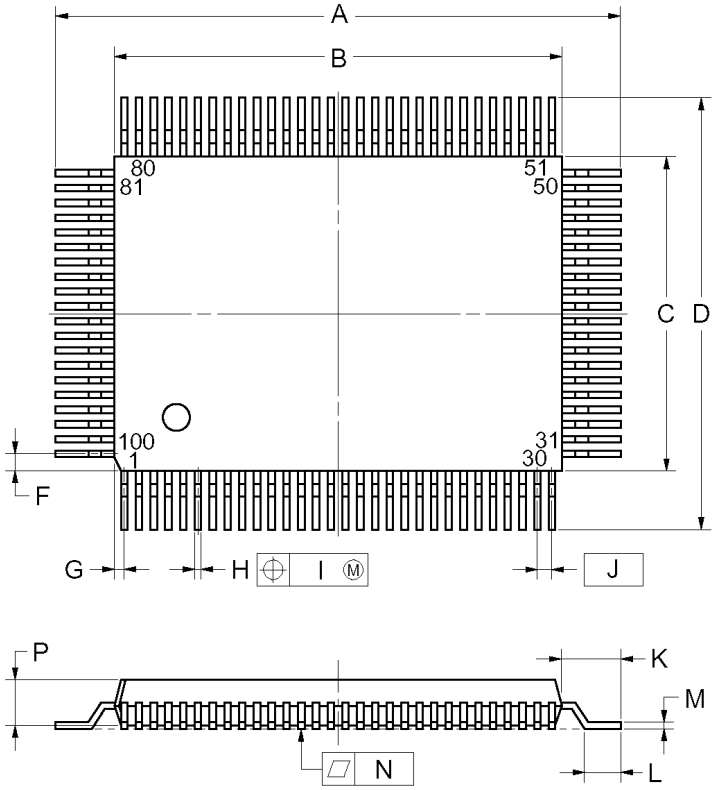
100 PIN PLASTIC QFP (14 20) detail of lead end



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.2±0.2	0.913±0.009
B	20.0±0.2	0.787±0.008
C	14.0±0.2	0.551±0.009
D	17.2±0.2	0.677±0.008
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	0.012±0.005
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	0.031±0.008
M	0.15±0.10	0.006±0.004
N	0.10	0.004
P	2.7	0.106
Q	0.125±0.075	0.005±0.003
R	5° ±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

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