Synchronous Rectified MOSFET Driver

The ISL6596 is a high frequency, MOSFET driver optimized to drive two N-Channel power MOSFETs in a synchronous buck converter topology. This driver combined with Intersil's Multi-Phase Buck PWM controllers forms a complete single-stage core-voltage regulator solution with high efficiency performance at high switching frequency for advanced microprocessors.

The IC is biased by a single low voltage supply (5V), minimizing driver switching losses in high MOSFET gate capacitance and high switching frequency applications. Each driver is capable of driving a 3nF load with less than 10ns rise/fall time. Bootstrapping of the upper gate driver is implemented via an internal low forward drop diode, reducing implementation cost, complexity, and allowing the use of higher performance, cost effective N-Channel MOSFETs. Adaptive shoot-through protection is integrated to prevent both MOSFETs from conducting simultaneously.

The ISL6596 features 4A typical sink current for the lower gate driver, enhancing the lower MOSFET gate hold-down capability during PHASE node rising edge, preventing power loss caused by the self turn-on of the lower MOSFET due to the high dV/dt of the switching node.

The ISL6596 also features an input that recognizes a high-impedance state, working together with Intersil multi-phase 3.3V or 5V PWM controllers to prevent negative transients on the controlled output voltage when operation is suspended. This feature eliminates the need for the schottky diode that may be utilized in a power system to protect the load from negative output voltage damage.

Applications

- Core Voltage Supplies for Intel® and AMD® Microprocessors
- High Frequency Low Profile High Efficiency DC/DC Converters
- High Current Low Voltage DC/DC Converters
- Synchronous Rectification for Isolated Power Supplies

Related Literature

- Technical Brief TB389 "PCB Land Pattern Design and Surface Mount Guidelines for QFN (MLFP) Packages"
- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"

Features

- Drives Two N-Channel MOSFETs
- Adaptive Shoot-Through Protection
- 0.4Ω On-Resistance and 4A Sink Current Capability
- Supports High Switching Frequency
    - Fast Output Rise and Fall Time
    - Low Tri-State Hold-Off Time (20ns)
- Support 3.3V and 5V PWM Input
- Low Quiescent Supply Current
- Power-On Reset
- Expandable Bottom Copper Pad for Heat Spreading
- Dual Flat No-Lead (DFN) Package
    - Compliant to JEDEC PUB95 MO-220 QFN-Quad Flat No Leads-Product Outline
    - Near Chip-Scale Package Footprint; Improves PCB Efficiency and Thinner in Profile
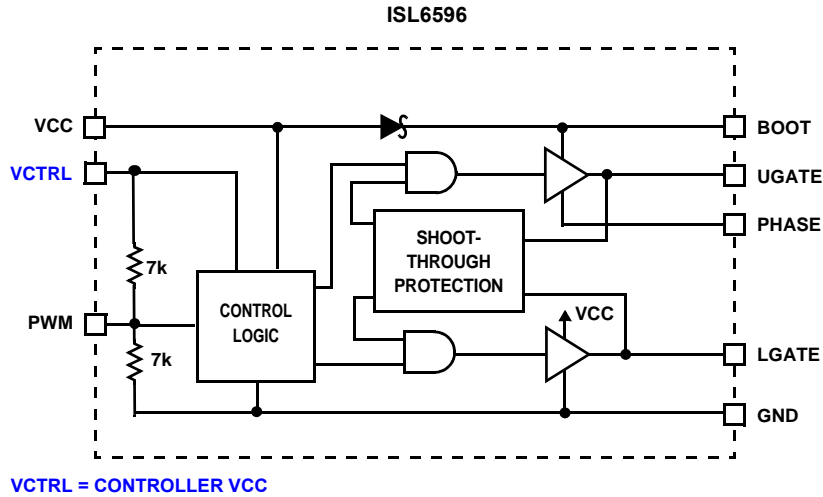- Pb-Free Plus Anneal Available (RoHS Compliant)

Ordering Information

PART NUMBER	PART MARKING	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6596CBZ (Note)	6596CBZ	0 to 70	8 Ld SOIC	M8.15
ISL6596CBZ-T (Note)	6596CBZ		8 Ld SOIC Tape and Reel	
ISL6596CRZ (Note)	596Z	0 to 70	10 Ld 3x3 DFN	L10.3x3
ISL6596CRZ-T (Note)	596Z		10 Ld DFN Tape and Reel	
ISL6596IBZ (Note)		-40 to 85	8 Ld SOIC	M8.15
ISL6596IBZ-T (Note)			8 Ld SOIC Tape and Reel	
ISL6596IRZ (Note)	96IZ	-40 to 85	10 Ld 3x3 DFN	L10.3x3
ISL6596IRZ-T (Note)	96IZ		10 Ld DFN Tape and Reel	

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
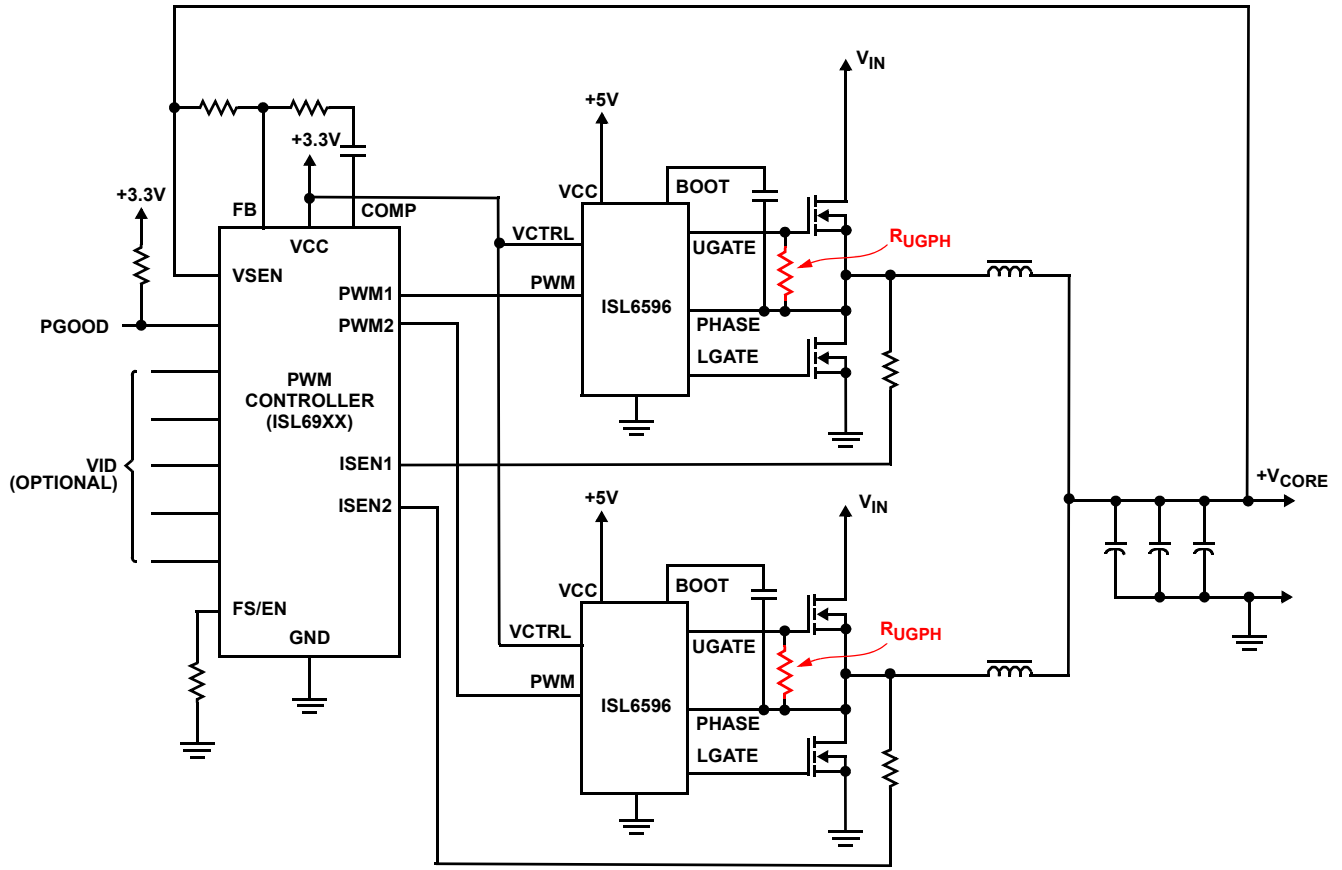
Pinout

ISL6596 (SOIC)
TOP VIEW

```
UGATE   1        8   PHASE
BOOT    2        7   VCTRL
PWM     3        6   VCC
GND     4        5   LGATE
```

ISL6596 (DFN)
TOP VIEW

```
UGATE   1       10   PHASE
BOOT    2        9   VCTRL
N/C     3        8   N/C
PWM     4        7   VCC
GND     5        6   LGATE
```

Block Diagram

ISL6596

VCTRL = CONTROLLER VCC

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FN9240.0
November 2, 2005

Typical Application - Multi-Phase Converter Using ISL6596 Gate Drivers

R$_{UGPH}$ IS REQUIRED FOR SPECIAL POWER SEQUENCING APPLICATIONS (SEE APPLICATION INFORMATION SECTION ON PAGE 8)

Absolute Maximum Ratings

Supply Voltage (VCC, VCTRL) . . . . -0.3V to 7V

Input Voltage (V_{EN}, V_{PWM}) . . . . -0.3V to VCC + 0.3V

BOOT Voltage ($V_{BOOT-GND}$). . . -0.3V to 25V (DC) or 36V (<200ns)

BOOT To PHASE Voltage ($V_{BOOT-PHASE}$) . . . . . . -0.3V to 7V (DC)
. . . . -0.3V to 9V (<10ns)

PHASE Voltage . . . . GND - 0.3V to 15V (DC)
. . . . GND -8V (<20ns Pulse Width, 10μJ) to 30V (<100ns)

UGATE Voltage . . . . V_{PHASE} - 0.3V (DC) to V_{BOOT}
. . . . V_{PHASE} - 5V (<20ns Pulse Width, 10μJ) to V_{BOOT}

LGATE Voltage . . . . GND - 0.3V (DC) to VCC + 0.3V
. . . . GND - 2.5V (<20ns Pulse Width, 5μJ) to VCC + 0.3V

Ambient Temperature Range . . . .-40°C to 125°C

HBM ESD Rating 2kV

Thermal Information

Thermal Resistance (Notes 1, 2, & 3)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SOIC Package (Note 1)	110	N/A
DFN Package (Notes 2 & 3).	48	7

Maximum Junction Temperature . . . . 150°C

Maximum Storage Temperature Range. . . . .-65°C to 150°C

Maximum Lead Temperature (Soldering 10s) . . . . .300°C
(SOIC - Lead Tips Only)

Recommended Operating Conditions

Ambient Temperature Range. . . . .-40°C to 100°C

Maximum Operating Junction Temperature. . . . . 125°C

Supply Voltage, VCC . . . . 5V ±10%

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features.

3. θ_{JC}, "case temperature" location is at the center of the package underside exposed pad. See Tech Brief TB379 for details.

Electrical Specifications   These specifications apply for *Recommended Operating Conditions*, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Bias Supply Current	I_{VCC}	PWM pin floating, V_{VCC} = 5V	-	190	-	μA
POR Rising			-	3.4	4.2	
POR Falling			2.2	3.0	-	
Hysteresis			-	400	-	mV
VCTRL INPUT						
Rising Threshold			-	2.75	2.90	V
Falling Threshold			2.4	2.65	-	V
PWM INPUT						
Sinking Impedance	R_{PWM_SNK}		-	3.5	-	kΩ
Source Impedance	R_{PWM_SRC}		-	3.5	-	kΩ
Tri-State LowerThreshold		V_{VCTRL} = 3.3V (-110mV Hysteresis)	-	1.1	-	V
		V_{VCTRL} = 5V (-250mV Hysteresis)	-	1.5	-	V
Tri-State Upper Threshold		V_{VCTRL} = 3.3V (+110mV Hysteresis)	-	1.9	-	V
		V_{VCTRL} = 5V (+250mV Hysteresis)	-	3.25	-	V
Tri-State Shutdown Holdoff Time	t_{TSSHD}	t_{PDLU} or t_{PDLL} + Gate Falling Time	-	20	-	ns
SWITCHING TIME (See Figure 1 on Page 5)						
UGATE Rise Time (Note 4)	t_{RU}	V_{VCC} = 5V, 3nF Load	-	8.0	-	ns
LGATE Rise Time (Note 4)	t_{RL}	V_{VCC} = 5V, 3nF Load	-	8.0	-	ns
UGATE Fall Time (Note 4)	t_{FU}	V_{VCC} = 5V, 3nF Load	-	8.0	-	ns
LGATE Fall Time (Note 4)	t_{FL}	V_{VCC} = 5V, 3nF Load	-	4.0	-	ns
UGATE Turn-Off Propagation Delay	t_{PDLU}	V_{VCC} = 5V, Outputs Unloaded	-	20	-	ns
LGATE Turn-Off Propagation Delay	t_{PDLL}	V_{VCC} = 5V, Outputs Unloaded	-	15	-	ns
UGATE Turn-On Propagation Delay	t_{PDHU}	V_{VCC} = 5V, Outputs Unloaded	-	19	-	ns
LGATE Turn-On Propagation Delay	t_{PDHL}	V_{VCC} = 5V, Outputs Unloaded	-	18	-	ns
Tri-state to UG/LG Rising Propagation Delay	t_{PTS}	V_{VCC} = 5V, Outputs Unloaded	-	30	-	ns
OUTPUT (Note 4)						
Upper Drive Source Resistance	R_{UG_SRC}	250mA Source Current	-	1.0	2.5	Ω
Upper Drive Sink Resistance	R_{UG_SNK}	250mA Sink Current	-	1.0	2.5	Ω
Lower Drive Source Resistance	R_{LG_SRC}	250mA Source Current	-	1.0	2.5	Ω
Lower Drive Sink Resistance	R_{LG_SNK}	250mA Sink Current	-	0.4	1.0	Ω

NOTE:

4. Guaranteed by Characterization. Not 100% tested in production.

Functional Pin Description

Note: Pin numbers refer to the SOIC package. Check diagram for corresponding DFN pinout.

UGATE (Pin 1)

Upper gate drive output. Connect to gate of high-side N-Channel power MOSFET. A gate resistor is never recommended on this pin, as it interferes with the operation shoot-through protection circuitry.

BOOT (Pin 2)

Floating bootstrap supply pin for the upper gate drive. Connect a bootstrap capacitor between this pin and the PHASE pin. The bootstrap capacitor provides the charge used to turn on the upper MOSFET. See the *Bootstrap Considerations* section for guidance in choosing the appropriate capacitor value.

PWM (Pin 3)

The PWM signal is the control input for the driver. The PWM signal can enter three distinct states during operation, see the *Tri-state PWM Input* section for further details. Connect this pin to the PWM output of the controller.

GND (Pin 4)

Ground pin. All signals are referenced to this node.

LGATE (Pin 5)

Lower gate drive output. Connect to gate of the low side N-Channel power MOSFET. A gate resistor is never recommended on this pin, as it interferes with the operation shoot-through protection circuitry.

VCC (Pin 6)

Connect this pin to a +5V bias supply. Locally bypass with a high quality ceramic capacitor to ground.

VCTRL (Pin 7)

This pin sets the PWM logic threshold. Connect this pin to 3.3V source for 3.3V PWM input and pull it to 5V source for 5V PWM input.

PHASE (Pin 8)

Connect this pin to the source of the upper MOSFET. This pin provides the return path for the upper gate driver current.

Thermal Pad (in DFN only)

The metal pad underneath the center of the IC is a thermal substrate. The PCB "thermal land" design for this exposed die pad should include vias that drop down and connect to one or more buried copper plane(s). This combination of vias for vertical heat escape and buried planes for heat spreading allows the DFN to achieve its full thermal potential. This pad should be either grounded or floating, and it should not be connected to other nodes. Refer to TB389 for design guidelines.
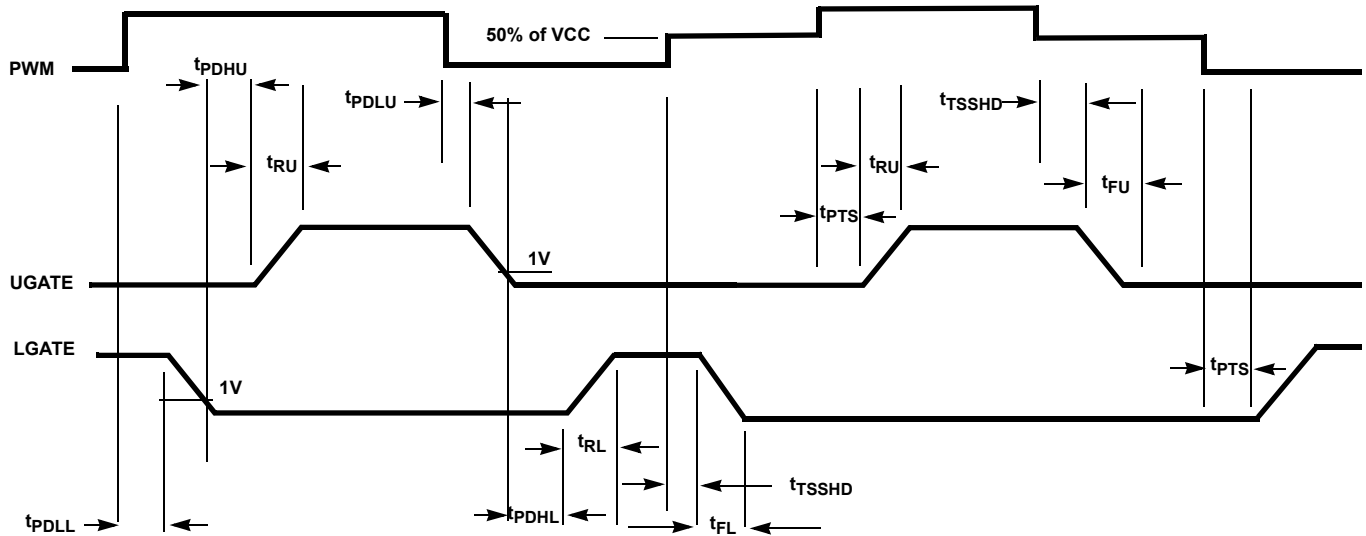
Timing Diagram

FIGURE 1. TIMING DIAGRAM

Operation and Adaptive Shoot-Through Protection

Designed for high speed switching, the ISL6596 MOSFET driver controls both high-side and low-side N-Channel FETs from one externally provided PWM signal.

A rising transition on PWM initiates the turn-off of the lower MOSFET (see Timing Diagram). After a short propagation delay [t_{PDLL}], the lower gate begins to fall. Typical fall times [t_{FL}] are provided in the *Electrical Specifications*. Adaptive shoot-through circuitry monitors the LGATE voltage and turns on the upper gate following a short delay time [t_{PDHU}] after the LGATE voltage drops below ~1V. The upper gate drive then begins to rise [t_{RU}] and the upper MOSFET turns on.

A falling transition on PWM indicates the turn-off of the upper MOSFET and the turn-on of the lower MOSFET. A short propagation delay [t_{PDLU}] is encountered before the upper gate begins to fall [t_{FU}]. The adaptive shoot-through circuitry monitors the UGATE-PHASE voltage and turns on the lower MOSFET a short delay time, t_{PDHL}, after the upper MOSFET's gate voltage drops below 1V. The lower gate then rises [t_{RL}], turning on the lower MOSFET. These methods prevent both the lower and upper MOSFETs from conducting simultaneously (shoot-through), while adapting the dead time to the gate charge characteristics of the MOSFETs being used.

This driver is optimized for voltage regulators with large step down ratio. The lower MOSFET is usually sized larger compared to the upper MOSFET because the lower MOSFET conducts for a longer time during a switching period. The lower gate driver is therefore sized much larger to meet this application requirement. The 0.4Ω on-resistance and 4A sink current capability enable the lower gate driver to absorb the current injected into the lower gate through the drain-to-gate capacitor of the lower MOSFET and help prevent shoot through caused by the self turn-on of the lower MOSFET due to high dV/dt of the switching node.

PWM Input and Threshold Control

A unique feature of the ISL6596 is the programmable PWM logic threshold set by the control pin (VCTRL) voltage. The VCTRL pin should connect to the VCC of the controller, thus the PWM logic threshold follows with the voltage level of the controller. For 5V applications, this pin can tie to the driver VCC and simplify the routing.

The ISL6596 also features the adaptable tri-state PWM input. Once the PWM signal enters the shutdown window, either MOSFET previously conducting is turned off. If the PWM signal remains within the shutdown window for longer than the gate turn-off propagation delay of the previously conducting MOSFET, the output drivers are disabled and both MOSFET gates are pulled and held low. The shutdown state is removed when the PWM signal moves outside the shutdown window. The PWM rising and falling thresholds outlined in the *Electrical Specifications* determine when the lower and upper gates are enabled. During normal operation in a typical application, the PWM rise and fall times through the shutdown window should

not exceed either output's turn-off propagation delay plus the MOSFET gate discharge time to ~1V. Abnormally long PWM signal transition times through the shutdown window will simply introduce additional dead time between turn off and turn on of the synchronous bridge's MOSFETs. For optimal performance, no more than 50pF parasitic capacitive load should be present on the PWM line of ISL6596 (assuming an Intersil PWM controller is used).

Bootstrap Considerations

This driver features an internal bootstrap diode. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit.

The following equation helps select a proper bootstrap capacitor size:

$$C_{BOOT\_CAP} \geq \frac{Q_{GATE}}{\Delta V_{BOOT\_CAP}}$$

(EQ. 1)

$$Q_{GATE} = \frac{Q_{G1} \bullet VCC}{V_{GS1}} \bullet N_{Q1}$$

where Q_{G1} is the amount of gate charge per upper MOSFET at V_{GS1} gate-source voltage and N_{Q1} is the number of control MOSFETs. The ΔV_{BOOT_CAP} term is defined as the allowable droop in the rail of the upper gate drive.

As an example, suppose two IRLR7821 FETs are chosen as the upper MOSFETs. The gate charge, Q_G, from the data sheet is 10nC at 4.5V (V_{GS}) gate-source voltage. Then the Q_{GATE} is calculated to be 22nC at VCC level. We will assume a 200mV droop in drive voltage over the PWM cycle. We find that a bootstrap capacitance of at least 0.110μF is required. The next larger standard value capacitance is 0.22μF. A good quality ceramic capacitor is recommended.
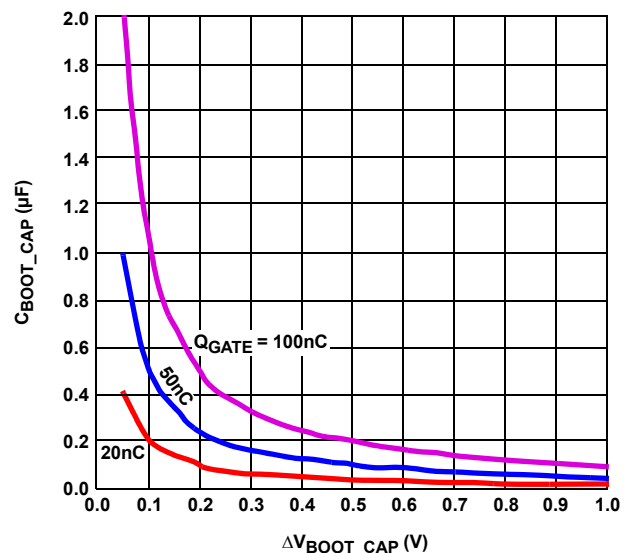

FIGURE 2. BOOTSTRAP CAPACITANCE vs BOOT RIPPLE VOLTAGE

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Power Dissipation

Package power dissipation is mainly a function of the switching frequency (F_{SW}), the output drive impedance, the external gate resistance, and the selected MOSFET's internal gate resistance and total gate charge. Calculating the power dissipation in the driver for a desired application is critical to ensure safe operation. Exceeding the maximum allowable power dissipation level will push the IC beyond the maximum recommended operating junction temperature of 125°C. The maximum allowable IC power dissipation for the SO8 package is approximately 800mW at room temperature, while the power dissipation capacity in the DFN package, with an exposed heat escape pad, is much higher. See Layout Considerations paragraph for thermal transfer improvement suggestions. When designing the driver into an application, it is recommended that the following calculation is used to ensure safe operation at the desired frequency for the selected MOSFETs. The total gate drive power losses due to the gate charge of MOSFETs and the driver's internal circuitry and their corresponding average driver current can be estimated with Equations 2 and 3, respectively:

$$P_{Qg\_TOT} = P_{Qg\_Q1} + P_{Qg\_Q2} + I_Q \bullet VCC \qquad \text{(EQ. 2)}$$

$$P_{Qg\_Q1} = \frac{Q_{G1} \bullet VCC^2}{V_{GS1}} \bullet F_{SW} \bullet N_{Q1}$$

$$P_{Qg\_Q2} = \frac{Q_{G2} \bullet VCC^2}{V_{GS2}} \bullet F_{SW} \bullet N_{Q2}$$

$$I_{VCC} = \left(\frac{Q_{G1} \bullet N_{Q1}}{V_{GS1}} + \frac{Q_{G2} \bullet N_{Q2}}{V_{GS2}} \right) \bullet VCC \bullet F_{SW} + I_Q$$

$$\text{(EQ. 3)}$$

where the gate charge (Q_{G1} and Q_{G2}) is defined at a particular gate to source voltage (V_{GS1} and V_{GS2}) in the corresponding MOSFET datasheet; I_Q is the driver's total quiescent current with no load at both drive outputs; N_{Q1} and N_{Q2} are the number of upper and lower MOSFETs, respectively. The I_Q V_{CC} product is the quiescent power of the driver without capacitive load and is typically negligible.

The total gate drive power losses are dissipated among the resistive components along the transition path. The drive resistance dissipates a portion of the total gate drive power losses, the rest will be dissipated by the external gate resistors (R_{G1} and R_{G2}, should be a short to avoid interfering with the operation shoot-through protection circuitry) and the internal gate resistors (R_{GI1} and R_{GI2}) of MOSFETs. Figures 3 and 4 show the typical upper and lower gate drives turn-on transition path. The power dissipation on the driver can be roughly estimated as:

$$P_{DR} = P_{DR\_UP} + P_{DR\_LOW} + I_Q \bullet VCC \qquad \text{(EQ. 4)}$$

$$P_{DR\_UP} = \left(\frac{R_{HI1}}{R_{HI1} + R_{EXT1}} + \frac{R_{LO1}}{R_{LO1} + R_{EXT1}} \right) \bullet \frac{P_{Qg\_Q1}}{2}$$

$$P_{DR\_LOW} = \left(\frac{R_{HI2}}{R_{HI2} + R_{EXT2}} + \frac{R_{LO2}}{R_{LO2} + R_{EXT2}} \right) \bullet \frac{P_{Qg\_Q2}}{2}$$

$$R_{EXT2} = R_{G1} + \frac{R_{GI1}}{N_{Q1}} \qquad R_{EXT2} = R_{G2} + \frac{R_{GI2}}{N_{Q2}}$$
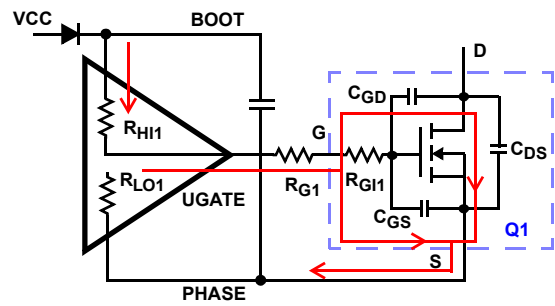

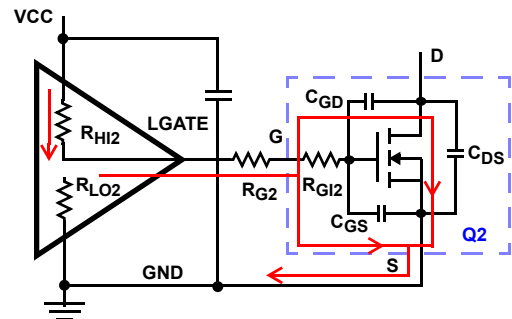**FIGURE 3. TYPICAL UPPER-GATE DRIVE TURN-ON PATH**

FIGURE 4. TYPICAL LOWER-GATE DRIVE TURN-ON PATH

Application Information

MOSFET Selection

The parasitic inductances of the PCB and of the power devices' packaging (both upper and lower MOSFETs) can cause serious ringing, exceeding absolute maximum rating of the devices. The negative ringing at the edges of the PHASE node could increase the bootstrap capacitor voltage through the internal bootstrap diode, and in some cases, it may overstress the upper MOSFET driver. Careful layout, proper selection of MOSFETs and packaging can go a long way toward minimizing such unwanted stress.

The D^2-PAK, or D-PAK packaged MOSFETs, have large parasitic lead inductances and are not recommended unless additional circuits are implemented to prevent the BOOT and PHASE pins from exceeding the device rating. Low-profile MOSFETs, such as Direct FETs and multi-SOURCE leads devices (SO-8, LFPAK, PowerPAK), have low parasitic lead inductances and are preferred.

Layout Considerations

A good layout helps reduce the ringing on the switching node (PHASE) and significantly lowers the stress applied to the output drives. The following advice is meant to lead to an optimized layout:

• Keep decoupling loops (VCC-GND and BOOT-PHASE) as short as possible.

• Minimize trace inductance, especially on low-impedance lines. All power traces (UGATE, PHASE, LGATE, GND, VCC) should be short and wide, as much as possible.

• Minimize the inductance of the PHASE node. Ideally, the source of the upper and the drain of the lower MOSFET should be as close as thermally allowable.

• Minimize the current loop of the output and input power trains. Short the source connection of the lower MOSFET to ground as close to the transistor pin as feasible. Input capacitors (especially ceramic decoupling) should be placed as close to the drain of upper and source of lower MOSFETs as possible.

In addition, for heat spreading, place copper underneath the IC whether it has an exposed pad or not. The copper area can be extended beyond the bottom area of the IC and/or connected to buried power ground plane(s) with thermal vias. This combination of vias for vertical heat escape, extended copper plane, and buried planes improve heat dissipation and allow the part to achieve its full thermal potential.

Upper MOSFET Self Turn-On Effects At Startup

Should the driver have insufficient bias voltage applied, its outputs are floating. If the input bus is energized at a high dV/dt rate while the driver outputs are floating, because of self-coupling via the internal C_{GD} of the MOSFET, the UGATE could momentarily rise up to a level greater than the threshold voltage of the MOSFET. This could potentially turn on the upper switch and result in damaging inrush energy. Therefore, if such a situation (when input bus powered up before the bias of the controller and driver is ready) could conceivably be encountered, it is a common practice to place a resistor (R_{UGPH}) across the gate and source of the upper MOSFET to suppress the Miller coupling effect. The value of the resistor depends mainly on the input voltage's rate of rise, the C_{GD}/C_{GS} ratio, as well as the gate-source threshold of the upper MOSFET. A higher dV/dt, a lower C_{DS}/C_{GS} ratio, and a lower gate-source threshold upper FET will require a smaller resistor to diminish the effect of the internal capacitive coupling. For most applications, a 5kΩ to 10kΩ resistor is typically sufficient, not affecting normal performance and efficiency.

The coupling effect can be roughly estimated with the following equations, which assume a fixed linear input ramp and neglect the clamping effect of the body diode of the upper drive and the bootstrap capacitor. Other parasitic components such as lead inductances and PCB capacitances are also not taken into account. These equations are provided for guidance purpose only. Therefore, the actual coupling effect should be examined using a very high impedance (10MΩ or greater) probe to ensure a safe design margin.

$$V_{GS\_MILLER} = \frac{dV}{dt} \cdot R \cdot C_{rss}\left(1 - e^{\dfrac{-V_{DS}}{\frac{dV}{dt} \cdot R \cdot C_{iss}}}\right) \quad \text{(EQ. 5)}$$

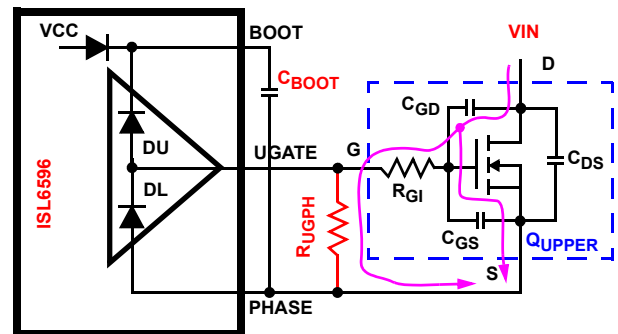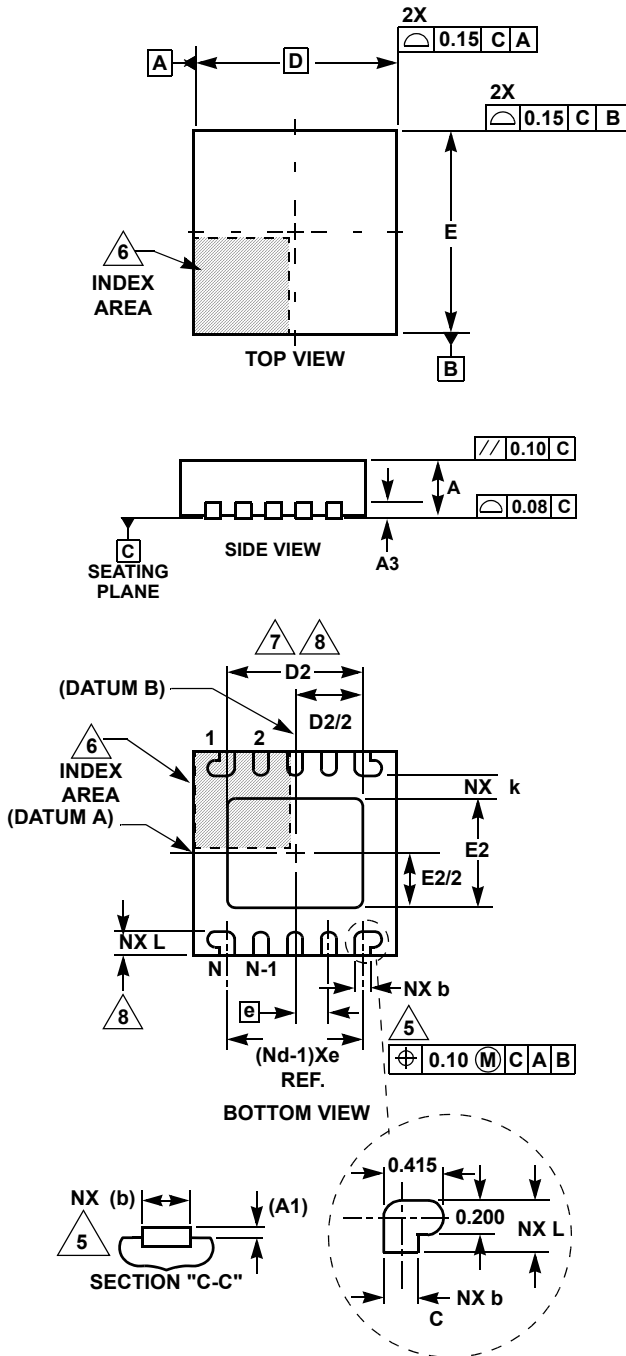$$R = R_{UGPH} + R_{GI} \qquad C_{rss} = C_{GD} \qquad C_{iss} = C_{GD} + C_{GS}$$

FIGURE 5. GATE TO SOURCE RESISTOR TO REDUCE UPPER MOSFET MILLER COUPLING

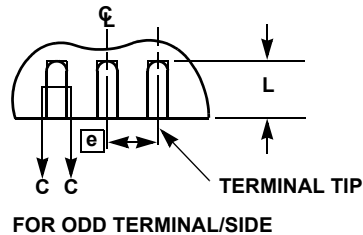## *Dual Flat No-Lead Plastic Package (DFN)*

L10.3x3
10 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A3	0.20 REF			-
b	0.18	0.23	0.28	5,8
D	3.00 BSC			-
D2	1.95	2.00	2.05	7,8
E	3.00 BSC			-
E2	1.55	1.60	1.65	7,8
e	0.50 BSC			-
k	0.25	-	-	-
L	0.30	0.35	0.40	8
N	10			2
Nd	5			3

Rev. 3 6/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.

2. N is the number of terminals.

3. Nd refers to the number of terminals on D.

4. All dimensions are in millimeters. Angles are in degrees.

5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.

6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.

8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.

Small Outline Plastic Packages (SOIC)

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

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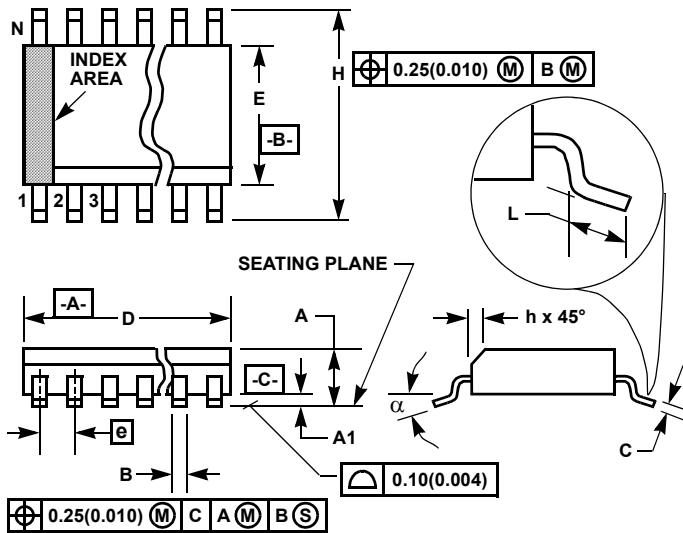
NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.

2. Dimensioning and tolerancing per ANSI Y14.5M-1982.

3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.

4. Dimension "E" does not include interlead flash or protrusions. Inter-lead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.

5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.

6. "L" is the length of terminal for soldering to a substrate.

7. "N" is the number of terminal positions.

8. Terminal numbers are shown for reference only.

9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).

10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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