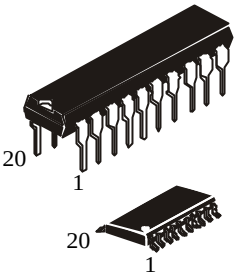
IN74LV241

OCTAL BUFFER/LINE DRIVE; 3-STATE

The IN74LV241 is a low-voltage Si-gate CMOS device and is pin and function compatible with IN74HC/HCT241.

The IN74LV241 is an octal non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $\overline{1OE}$ and 2OE.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 1.2 to 3.6 V
- Low Input Current: 1.0 µA, 0.1 µÀ at Ò = 25 °Ñ
- Output Current: 8 mA at V_{CC} = 3.0 V
- High Noise Immunity Characteristic of CMOS Devices



N SUFFIX
PLASTIC DIP

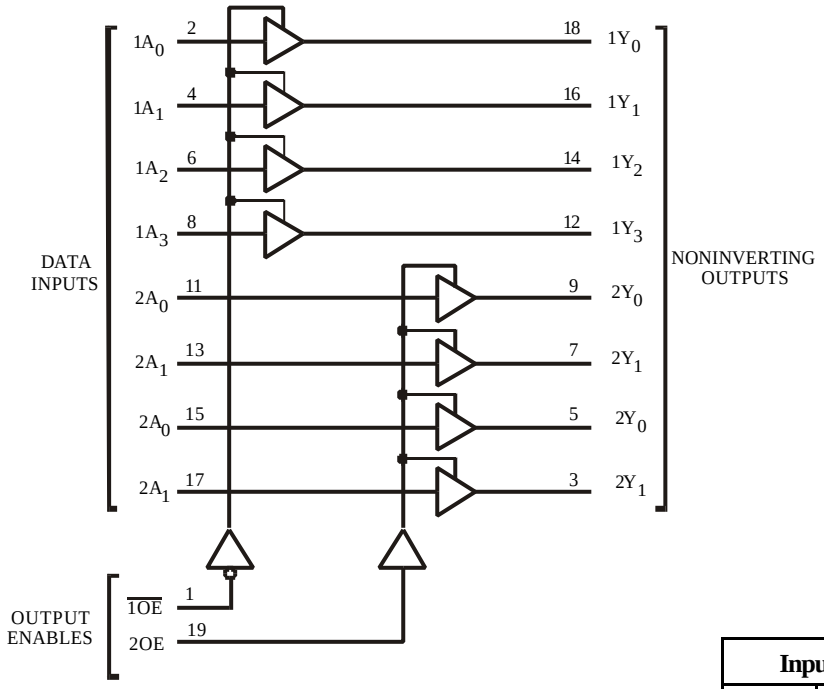
DW SUFFIX
SO

ORDERING INFORMATION

IN74LV241N	Plastic DIP
IN74LV241DW	SOIC
IZ74LV241	chip

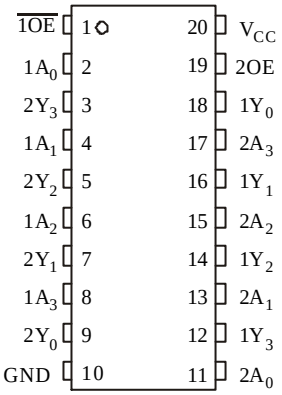
T_A = -40° to 125° C for all packages

LOGIC DIAGRAM



PIN 20=V_{CC}
PIN 10 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Input		Output	Input		Output
$\overline{1OE}$	1An	1Yn	2OE	2An	2Yn
L	L	L	H	L	L
L	H	H	H	H	H
H	X	Z	L	X	Z

H= high level
L = low level
X = don't care
Z = high impedance

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	-0.5 to +5.0	V
I_{IK} *1	DC Input diode current	±20	mA
I_{OK} *2	DC Output diode current	±50	mA
I_O *3	DC Output source or sink current	±35	mA
I_{CC}	DC V_{CC} current	±70	mA
I_{GND}	DC GND current	±70	mA
P_D	Power dissipation per package: *4 Plastic DIP SO	 750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1.5 mm (Plastic DIP Package), 0.3 mm (SO Package) from Case for 4 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
*1 $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V.
*2 $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V.
*3 -0.5 V $< V_O < V_{CC} + 0.5$ V.
*4 Derating - Plastic DIP: - 12 mW/°C from 70° to 125°C
SO Package: : - 8 mW/°C from 70° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		1.2	3.6	V
V_I	Input Voltage		0	V_{CC}	V
V_O	Output Voltage		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-40	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} =1.2 V V_{CC} =2.0 V V_{CC} =3.0 V V_{CC} =3.6 V	0 0 0 0	1000 700 500 400	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test conditions	V_{CC} V	Guaranteed Limit						Unit
				25°C		-40°C to 85°C		125°C		
				min	max	min	max	min	max	
V_{IH}	HIGH level input voltage		1.2 2.0 3.0 3.6	0.9 1.4 2.1 2.5	- - - -	0.9 1.4 2.1 2.5	- - - -	0.9 1.4 2.1 2.5	- - - -	V
V_{IL}	LOW level input voltage		1.2 2.0 3.0 3.6	- - - -	0.3 0.6 0.9 1.1	- - - -	0.3 0.6 0.9 1.1	- - - -	0.3 0.6 0.9 1.1	V
V_{OH}	HIGH level output voltage	$V_I = V_{IH}$ or V_{IL} I_O = -50 µA	1.2 2.0 3.0 3.6	1.1 1.92 2.92 3.52	- - - -	1.0 1.9 2.9 3.5	- - - -	1.0 1.9 2.9 3.5	- - - -	V
		$V_I = V_{IH}$ or V_{IL} I_O = -8 mA	3.0	2.48	-	2.34	-	2.20	-	V
V_{OL}	LOW level output voltage	$V_I = V_{IH}$ or V_{IL} I_O = 50 µA	1.2 2.0 3.0 3.6	- - - -	0.09 0.09 0.09 0.09	- - - -	0.1 0.1 0.1 0.1	- - - -	0.1 0.1 0.1 0.1	V
		$V_I = V_{IH}$ or V_{IL} I_O = 8 mA	3.0	-	0.33	-	0.4	-	0.5	V
I_I	Input current	$V_I = V_{CC}$ or 0 V	*	-	±0.1	-	±1.0	-	±1.0	µA
I_{OZ}	Three state leakage current	3-state outputs V_I (01,19) = V_{IH} V_O = V_{CC} or 0 V	1.2 *	-	±0.5	-	±5	-	±10	µA
I_{CC}	Supply current	V_I = V_{CC} or 0 V I_O = 0 µA	*	-	8.0	-	80	-	160	µA

* V_{CC} = 3.3 ± 0.3 V

AC ELECTRICAL CHARACTERISTICS (C_L=50 pF, t_r=t_f=6.0 ns)

Symbol	Parameter	Test conditions	V_{CC} V	Guaranteed Limit						Unit
				25°C		-40°C to 85°C		125°C		
				min	max	min	max	min	max	
t_{PHL}, t_{PLH}	Propagation delay , 1An to 1Yn, 2An to 2Yn	V_I = 0 V or V_{CC} Figure 1 and 3	1.2	-	100	-	125	-	150	ns
			2.0	-	24	-	30	-	36	
			*	-	15	-	19	-	23	
t_{PHZ} t_{PLZ}	Propagation delay, $\overline{1OE}$ to 1Yn, 2OE to 2Yn	V_I = 0 V or V_{CC} Figure 2 and 4	1.2	-	140	-	175	-	210	ns
			2.0	-	30	-	35	-	41	
			*	-	20	-	24	-	28	
t_{PZH} t_{PZL}	Propagation delay, $\overline{1OE}$ to 1Yn, 2OE to 2Yn	V_I = 0 V or V_{CC} Figure 2 and 4	1.2	-	140	-	175	-	210	ns
			2.0	-	32	-	40	-	48	
			*	-	20	-	25	-	30	
t_{THL}, t_{TLH}	Output Transition Time, Any Output	V_I = 0 V or V_{CC} Figure 1 and 3	1.2	-	60	-	75	-	90	ns
			2.0	-	16	-	20	-	24	
			*	-	10	-	13	-	15	
C_I	Input capacitance		3.0	-	7.0	-	7.0	-	7.0	pF
C_{PD}	Power dissipation capacitance (per one channel)	V_I = 0 V or V_{CC}		-	70	-	-	-	-	pF

* V_{CC} = 3.3 ± 0.3 V

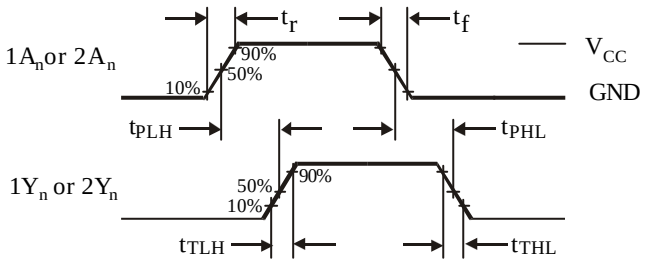


Figure 1. Switching Waveforms

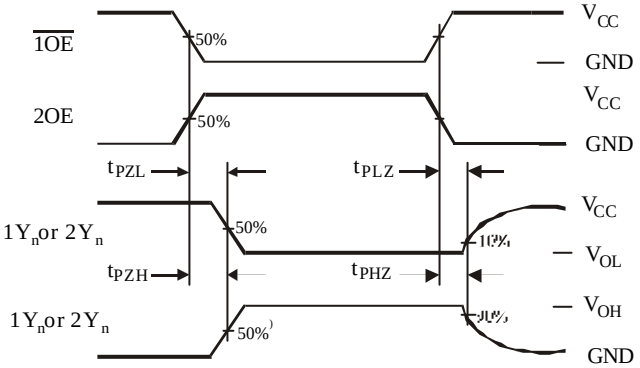
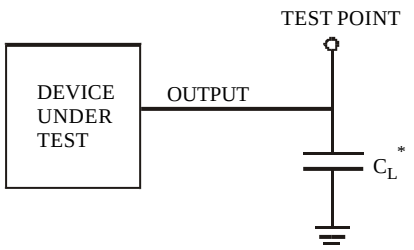
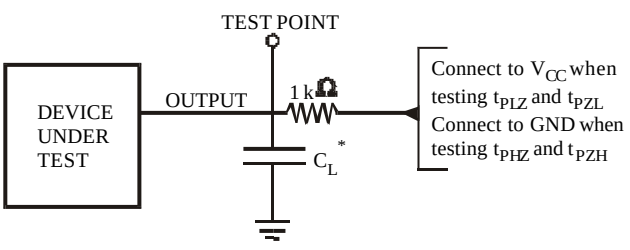


Figure 2. Switching Waveforms



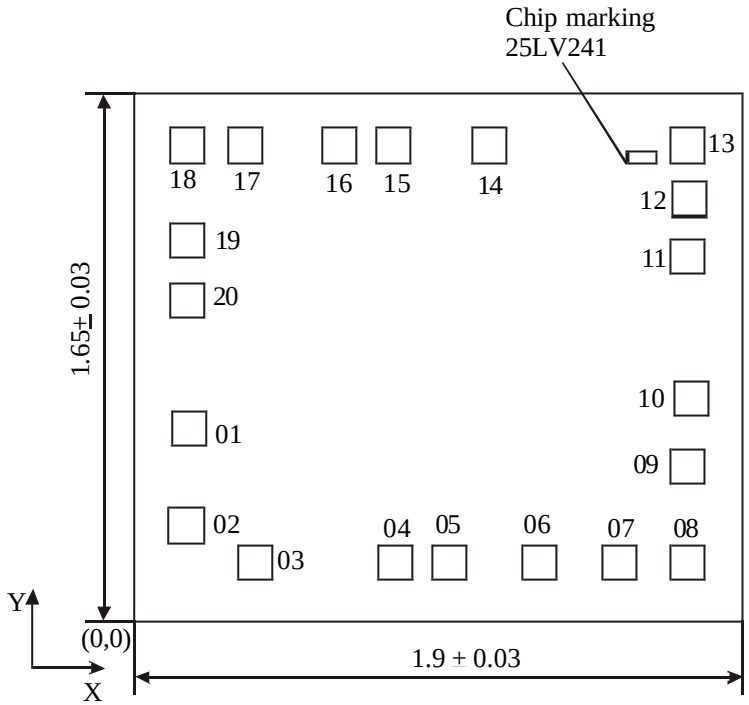
* Includes all probe and jig capacitance



* Includes all probe and jig capacitance

Figure 3. Test Circuit **Figure 4. Test Circuit**

CHIP PAD DIAGRAM



Location of marking (mm): left lower corner x=1.539, y=1.433.

Chip thickness: 0.46 ± 0.02 mm.

PAD LOCATION

Pad No	Symbol	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	$\overline{1OE}$	0.115	0.55	0.108 x 0.108
02	$1A_0$	0.1075	0.246	0.108 x 0.108
03	$2Y_3$	0.3215	0.131	0.108 x 0.108
04	$1A_1$	0.76	0.131	0.108 x 0.108
05	$2Y_2$	0.9285	0.131	0.108 x 0.108
06	$2A_2$	1.2115	0.131	0.108 x 0.108
07	$2Y_1$	1.4615	0.131	0.108 x 0.108
08	$2A_3$	1.674	0.131	0.108 x 0.108
09	$2Y_0$	1.674	0.43	0.108 x 0.108
10	GND	1.685	0.643	0.108 x 0.108
11	$2A_0$	1.674	1.0855	0.108 x 0.108
12	$1Y_3$	1.6795	1.266	0.108 x 0.108
13	$2A_1$	1.674	1.4345	0.108 x 0.108
14	$1Y_2$	1.0525	1.4345	0.108 x 0.108
15	$2A_2$	0.7545	1.4345	0.108 x 0.108
16	$1Y_1$	0.586	1.4345	0.108 x 0.108
17	$2A_3$	0.293	1.4345	0.108 x 0.108
18	$1Y_0$	0.112	1.4345	0.108 x 0.108
19	2OE	0.112	1.1385	0.108 x 0.108
20	V_{CC}	0.112	0.949	0.108 x 0.108

Note: Pad location is given as per metallization layer