

#### -100 Volt, 0.30Ω HEXFET

HEXFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry achieves very low on-state resistance combined with high transconductance.

HEXFET transistors also feature all of the well-established advantages of MOSFETs, such as voltage control, very fast switching, ease of paralleling and electrical parameter temperature stability. They are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits, and virtually any application where high reliability is required.

#### Product Summary

Part Number	BV <sub>DSS</sub>	R <sub>DSON</sub>	I <sub>D</sub>
JANTX2N6804	-100V	0.30Ω	-11A
JANTXV2N6804			

#### Features:

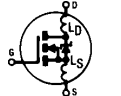
- Avalanche Energy Rating
- Dynamic dv/dt Rating
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed

#### Absolute Maximum Ratings

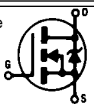
	Parameter	JANTX2N6804, JANTXV2N6804	Units
I <sub>D</sub> @ V <sub>GS</sub> = -10V, T <sub>C</sub> = 25°C	Continuous Drain Current	-11	A
I <sub>D</sub> @ V <sub>GS</sub> = -10V, T <sub>C</sub> = 100°C	Continuous Drain Current	-7	
I <sub>DM</sub>	Pulsed Drain Current ①	-50	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Max. Power Dissipation	75	W
	Linear Derating Factor	0.60	W/K ⑤
V <sub>GS</sub>	Gate-to-Source Voltage	±20	V
EAS	Single Pulse Avalanche Energy ②	81	mJ
I <sub>AR</sub>	Avalanche Current ①	-11	A
EAR	Repetitive Avalanche Energy ①	7.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.5	V/ns
T <sub>J</sub>	Operating Junction	-55 to 150	°C
T <sub>STG</sub>	Storage Temperature Range		
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10.5 seconds)	
	Weight	11.5 (typical)	

# JANTX2N6804, JANTXV2N6804 Device

## Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	-100	—	—	V	$V_{GS} = 0V, I_D = -1.0 \text{ mA}$
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	-0.087	—	V/°C	Reference to 25°C, $I_D = -1.0 \text{ mA}$
RDS(on)	Static Drain-to-Source	—	—	0.30	$\Omega$	$V_{GS} = -10V, I_D = -7A$ ④
	On-State Resistance	—	—	0.35		$V_{GS} = -10V, I_D = -11A$
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
$g_{fs}$	Forward Transconductance	3	—	—	S (r)	$V_{DS} > -15V, I_{DS} = -7A$ ④
IDSS	Zero Gate Voltage Drain Current	—	—	-25	$\mu A$	$V_{DS} = 0.8 \times \text{Max Rating}, V_{GS} = 0V$
		—	—	-250		$V_{DS} = 0.8 \times \text{Max Rating}, V_{GS} = 0V, T_J = 125^\circ C$
IGSS	Gate-to-Source Leakage Forward	—	—	-100	nA	$V_{GS} = -20V$
IGSS	Gate-to-Source Leakage Reverse	—	—	100	nA	$V_{GS} = 20V$
Qg	Total Gate Charge	1.5	—	29	nC	$V_{GS} = -10V, I_D = -11A$
Qgs	Gate-to-Source Charge	1.0	—	7.1		$V_{DS} = \text{Max. Rating} \times 0.5$
Qgd	Gate-to-Drain ("Miller") Charge	2.0	—	21		see figures 6 and 13
td(on)	Turn-On Delay Time	—	—	60	ns	$V_{DD} = -50V, I_D = -11A, R_G = 7.5\Omega, V_{GS} = -10V$
tr	Rise Time	—	—	140		
td(off)	Turn-Off Delay Time	—	—	140		
tf	Fall Time	—	—	140		
LD	Internal Drain Inductance	—	5.0	—	nH	<p>Measured from the drain lead, 6mm (0.25 in.) from package to center of die.</p> <p>Modified MOSFET symbol showing the internal inductances.</p> 
LS	Internal Source Inductance	—	13	—		
Ciss	Input Capacitance	—	860	—	pF	$V_{GS} = 0V, V_{DS} = -25V$ $f = 1.0 \text{ MHz}$ see figure 5
Coss	Output Capacitance	—	350	—		
Crss	Reverse Transfer Capacitance	—	125	—		

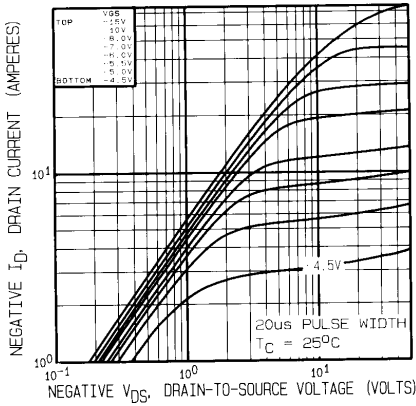
## Source-Drain Diode Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current (Body Diode)	—	—	-11	A	<p>Modified MOSFET symbol showing the integral reverse p-n junction rectifier.</p> 
ISM	Pulse Source Current (Body Diode) ①	—	—	-50		
VSD	Diode Forward Voltage	—	—	-4.7	V	$T_J = 25^\circ C, I_S = -11A, V_{GS} = 0V$ ④
trr	Reverse Recovery Time	—	—	250	ns	$T_J = 25^\circ C, I_F = -11A, di/dt \leq -100A/\mu s$
QRR	Reverse Recovery Charge	—	—	3.0	$\mu C$	$V_{DD} \leq -50V$ ④
ton	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by LS + LD.				

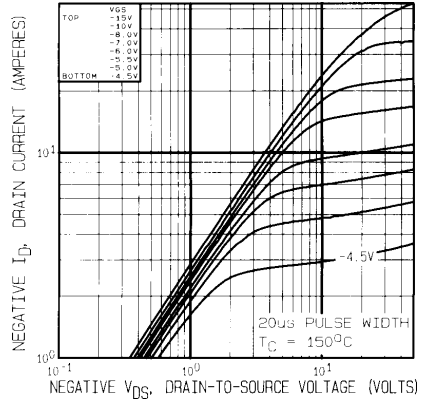
## Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RthJC	Junction-to-Case	—	—	1.67	K/W	Typical socket mount
RthJA	Junction-to-Ambient	—	—	30		

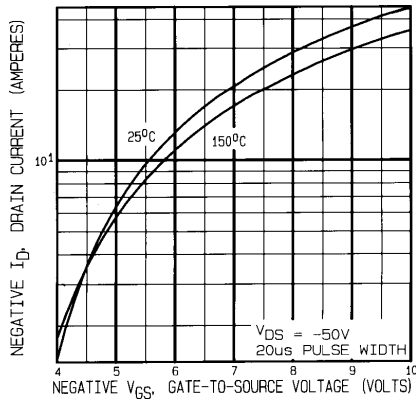
# JANTX2N6804, JANTXV2N6804 Device



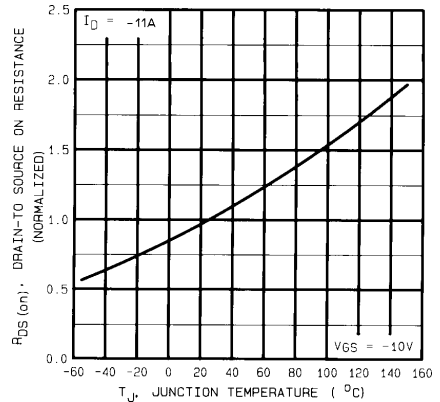
**Fig. 1 — Typical Output Characteristics**  
 $T_C = 25^\circ\text{C}$



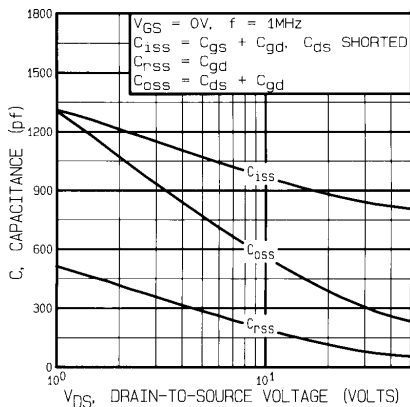
**Fig. 2 — Typical Output Characteristics**  
 $T_C = 150^\circ\text{C}$



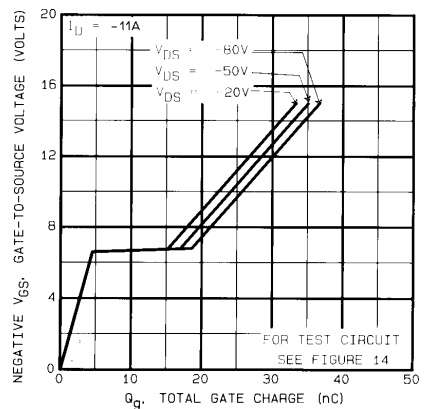
**Fig. 3 — Typical Transfer Characteristics**



**Fig. 4 — Normalized On-Resistance Vs. Temperature**



**Fig. 5 — Typical Capacitance Vs. Drain-to-Source Voltage**



**Fig. 6 — Typical Gate Charge Vs. Gate-to-Source Voltage**

# JANTX2N6804, JANTXV2N6804 Device

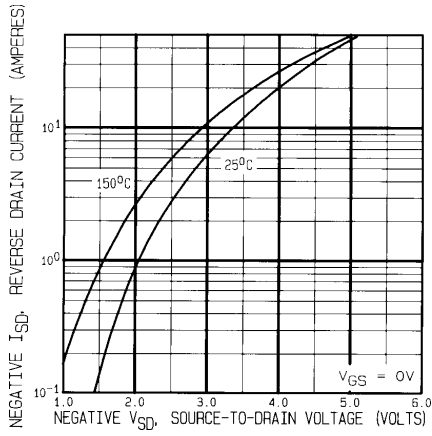


Fig. 7 — Typical Source-to-Drain Diode Forward Voltage

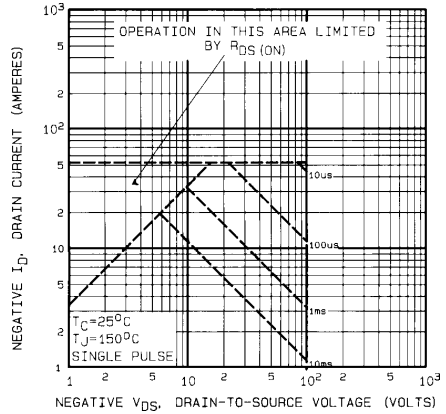


Fig. 8 — Maximum Safe Operating Area

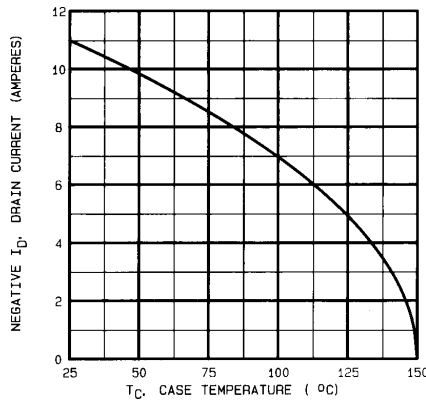


Fig. 9 — Maximum Drain Current vs. Case Temperature

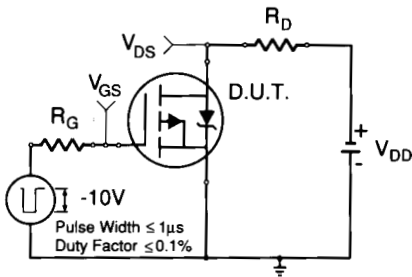


Fig. 10a — Switching Time Test Circuit

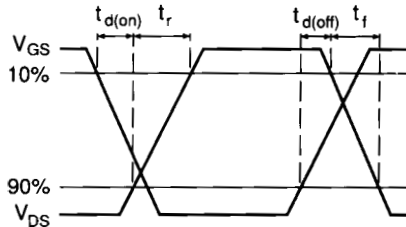


Fig. 10b — Switching Time Waveforms

# JANTX2N6804, JANTXV2N6804 Device

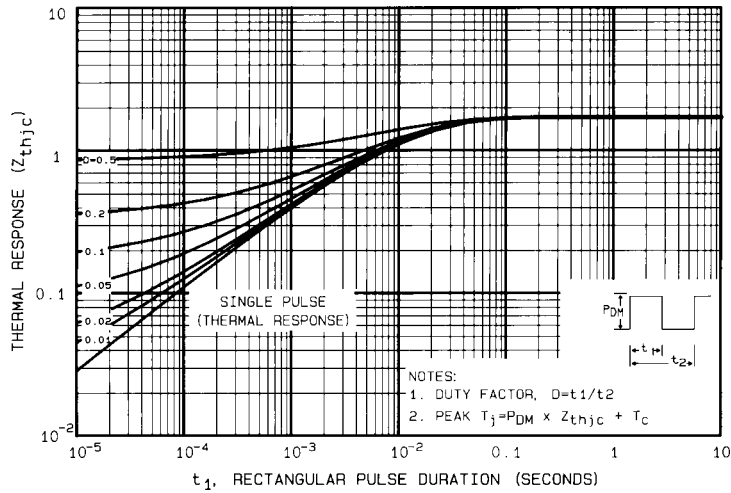


Fig. 11 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

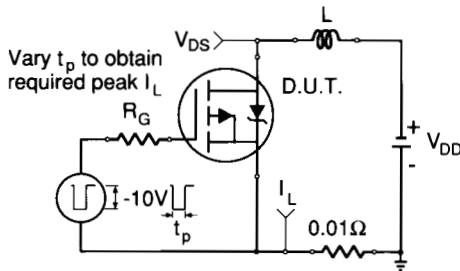


Fig. 12a — Unclamped Inductive Test Circuit

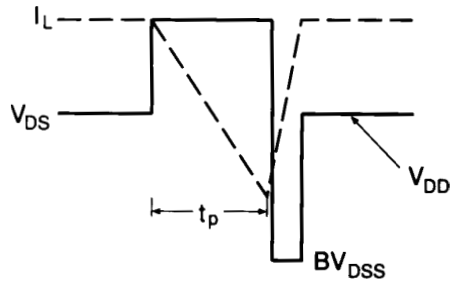


Fig. 12b — Unclamped Inductive Waveforms

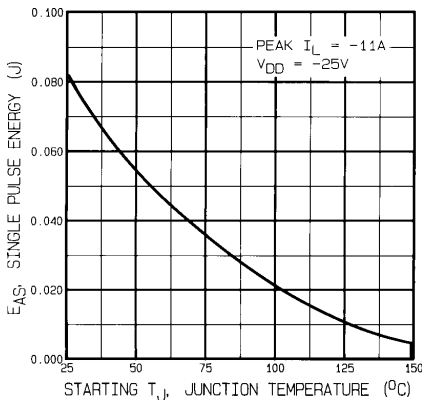


Fig. 12c — Max. Avalanche Energy vs. Current

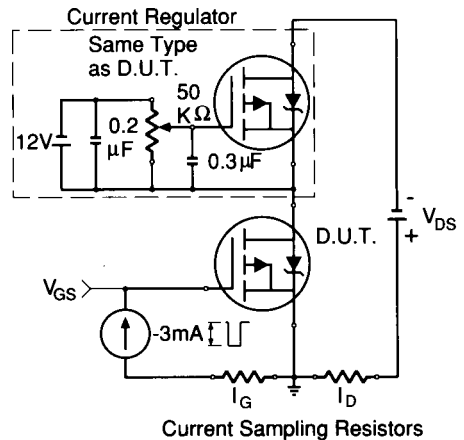


Fig. 13a — Gate Charge Test Circuit

# JANTX2N6804, JANTXV2N6804 Device

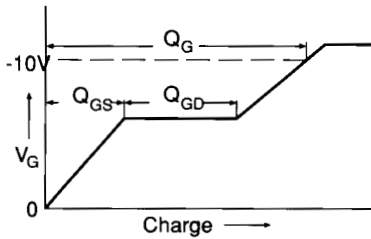
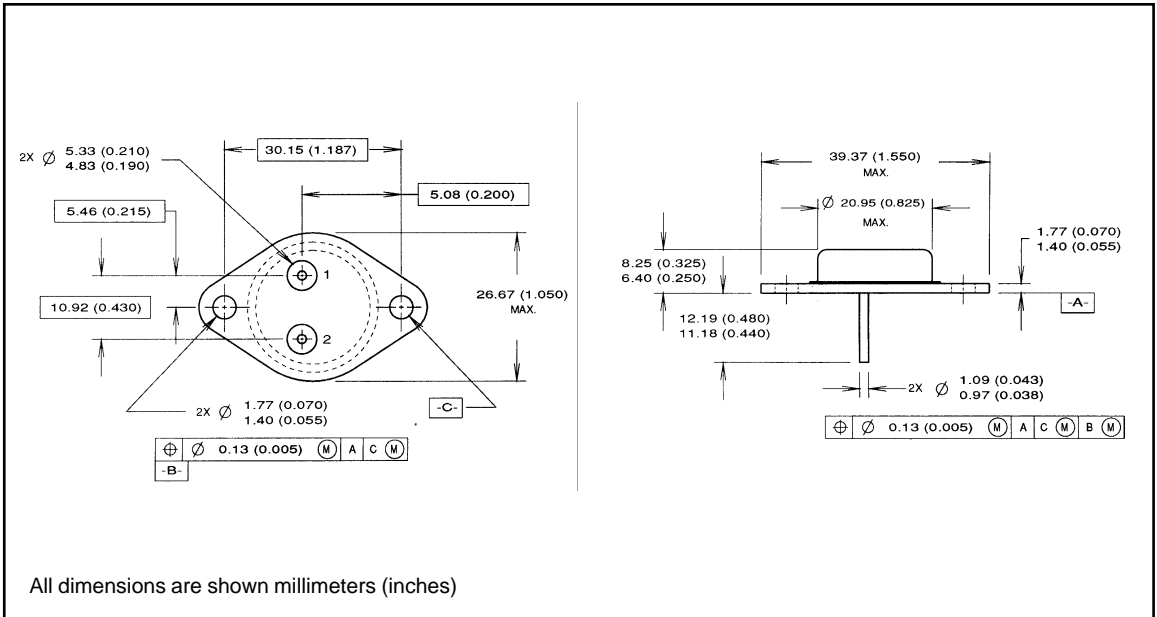


Fig. 13b — Basic Gate Charge Waveform

- ① Repetitive Rating; Pulse width limited by maximum junction temperature. (see figure 11)
- ② @  $V_{DD} = -25V$ , Starting  $T_J = 25^\circ C$ ,  
 $EAS = [0.5 * L * (I_L^2) * [BV_{DSS}/(BV_{DSS}-V_{DD})]$   
 Peak  $I_L = -11A$ ,  $V_{GS} = -10V$ ,  $25 \leq R_G \leq 200\Omega$
- ③  $I_{SD} \leq -11A$ ,  $di/dt \leq -140A/\mu s$ ,  
 $V_{DD} \leq BV_{DSS}$ ,  $T_J \leq 150^\circ C$
- ④ Pulse width  $\leq 300 \mu s$ ; Duty Cycle  $\leq 2\%$
- ⑤  $K/W = ^\circ C/W$   
 $W/K = W/^\circ C$

## Case Outline and Dimensions — TO-204AA (Modified TO-3)



International  
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