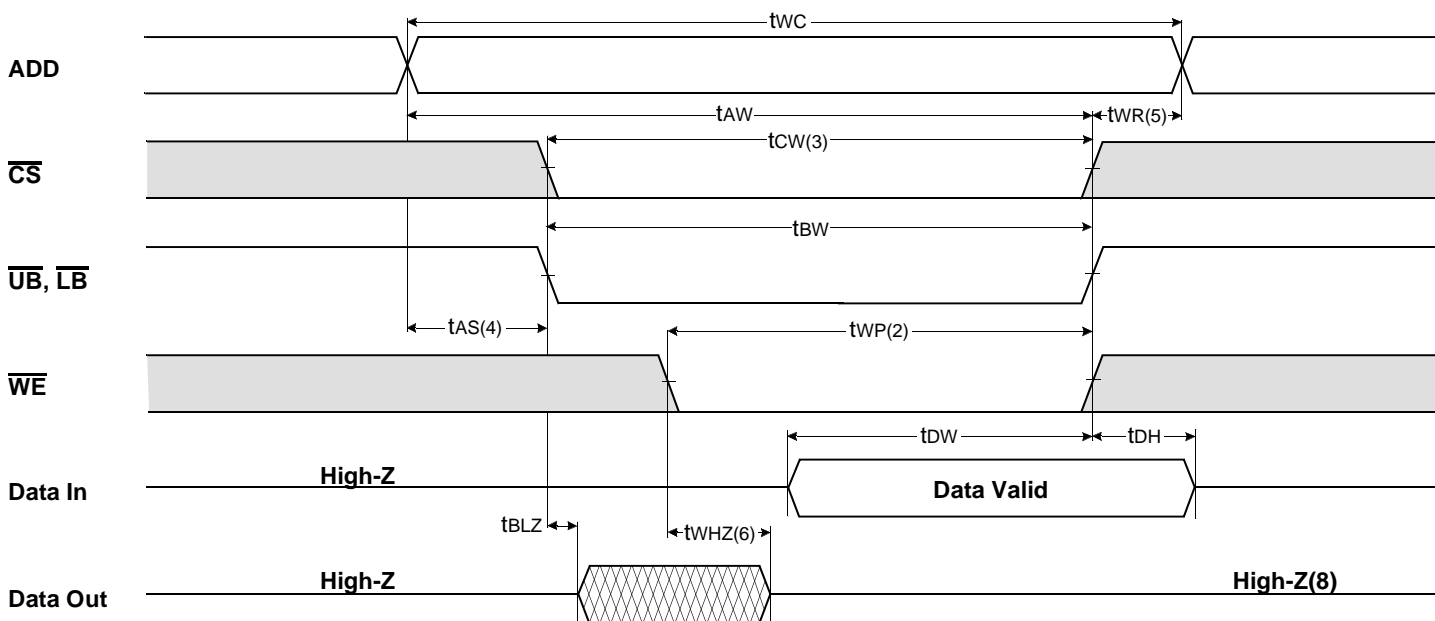




TIMING WAVE FORM OF WRITE CYCLE(4)  $\overline{UB}$ ,  $\overline{LB}$  Controlled)



NOTES(WRITE CYCLE)

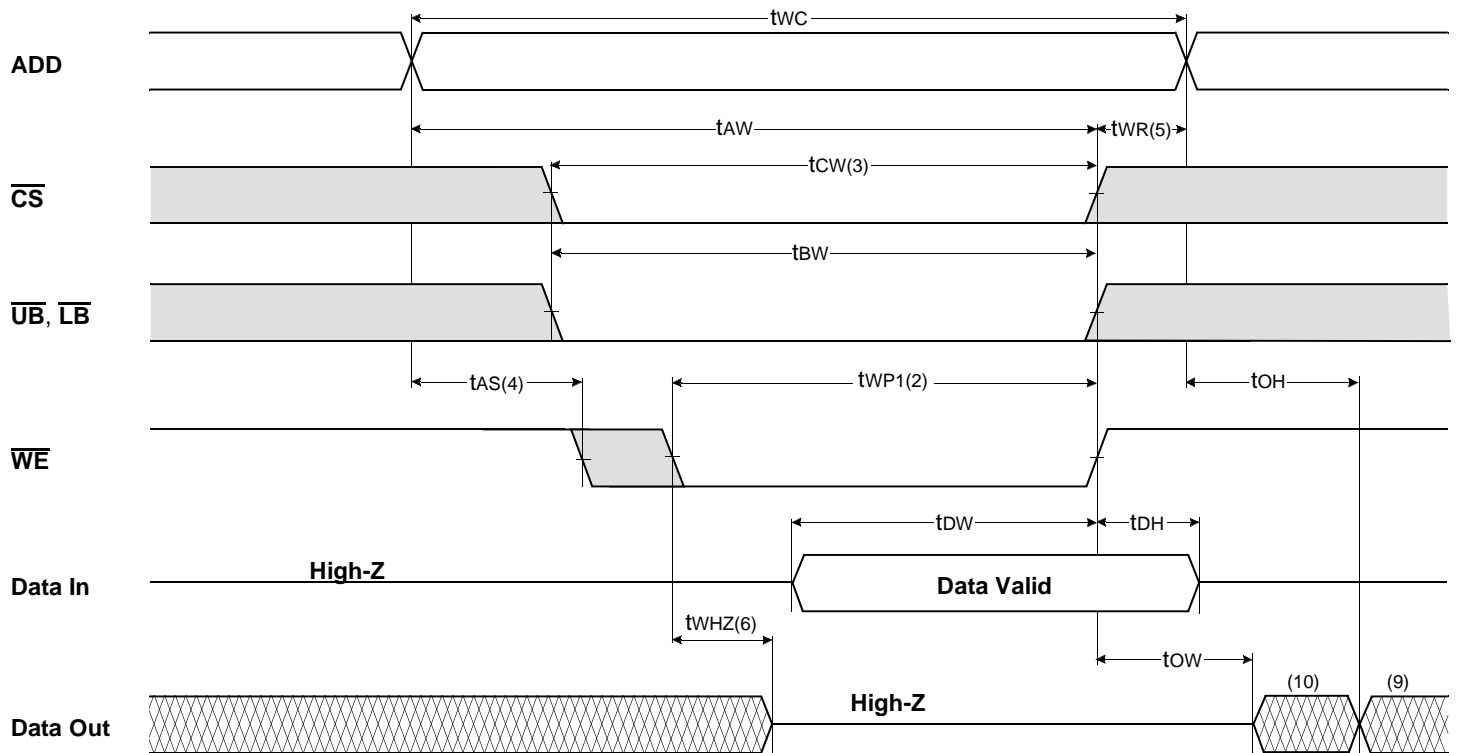
1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low  $\overline{CS}$ ,  $\overline{WE}$ ,  $\overline{LB}$  and  $\overline{UB}$ . A write begins at the latest transition  $\overline{CS}$  going low and  $\overline{WE}$  going low ; A write ends at the earliest transition  $\overline{CS}$  going high or  $\overline{WE}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
3.  $t_{CW}$  is measured from the later of  $\overline{CS}$  going low to end of write.
4.  $t_{AS}$  is measured from the address valid to the beginning of write.
5.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  applied in case a write ends as  $\overline{CS}$ , or  $\overline{WE}$  going high.
6. If  $\overline{OE}$ ,  $\overline{CS}$  and  $\overline{WE}$  are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If  $\overline{CS}$  goes low simultaneously with  $\overline{WE}$  going or after  $\overline{WE}$  going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When  $\overline{CS}$  is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

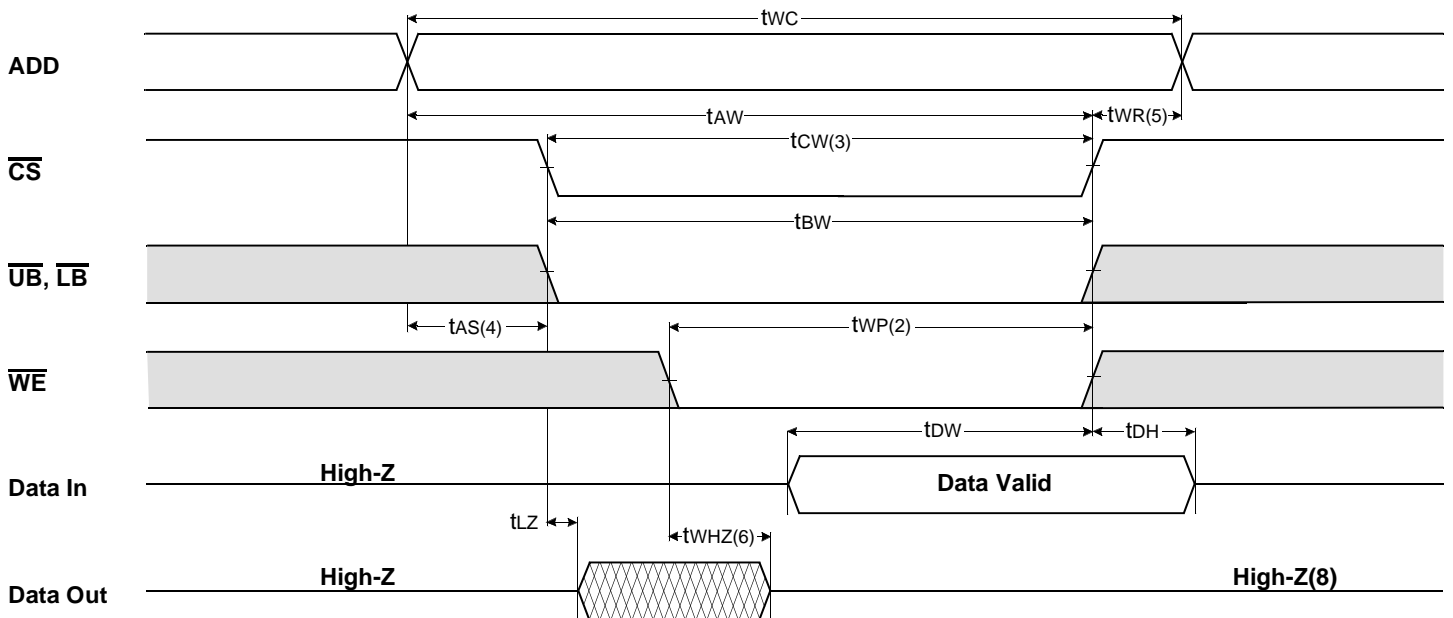
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O1~I/O8	I/O9~I/O16	
H	X	X*	X	X	Not Select	High-Z	High-Z	ISB, ISB1
L	H	H	X	X	Output Disable	High-Z	High-Z	Icc
L	X	X	H	H				
L	H	L	L	H	Read	DOUT	High-Z	Icc
			H	L		High-Z	DOUT	
			L	L		DOUT	DOUT	
L	L	X	L	H	Write	DIN	High-Z	Icc
			H	L		High-Z	DIN	
			L	L		DIN	DIN	

\* NOTE : X means Don't Care.

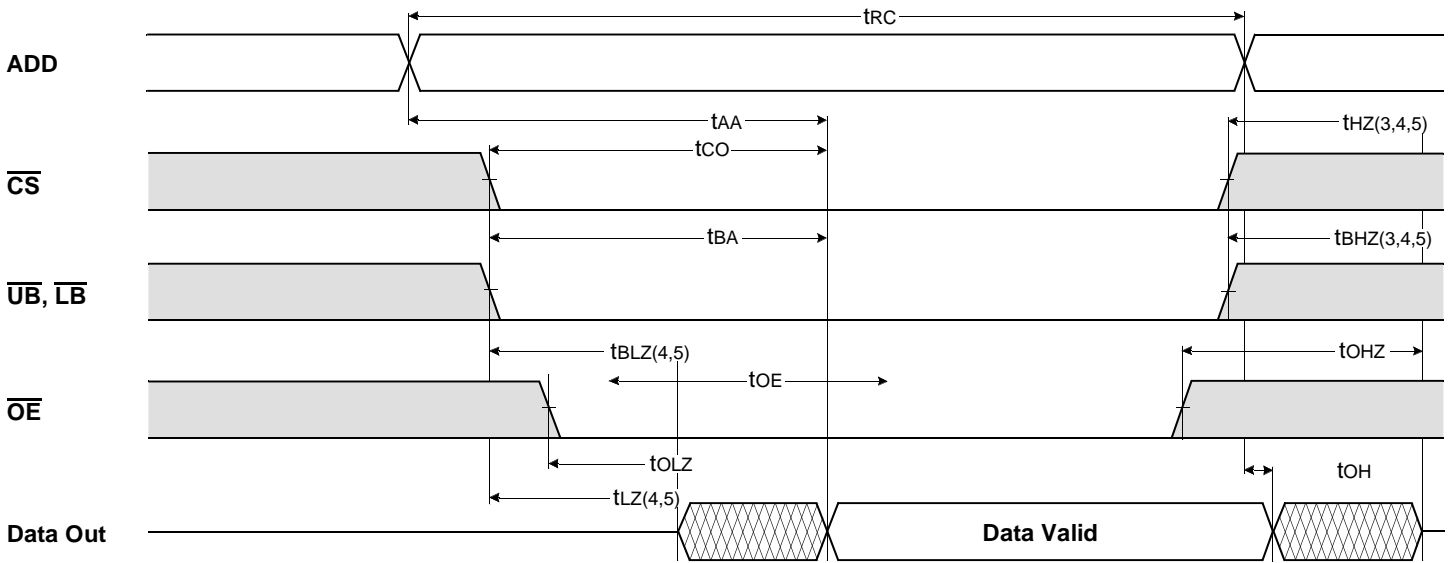
TIMING WAVE FORM OF WRITE CYCLE(2)  $\overline{OE}$ =Low Fixed



TIMING WAVE FORM OF WRITE CYCLE(3)  $\overline{CS}$ =Controlled



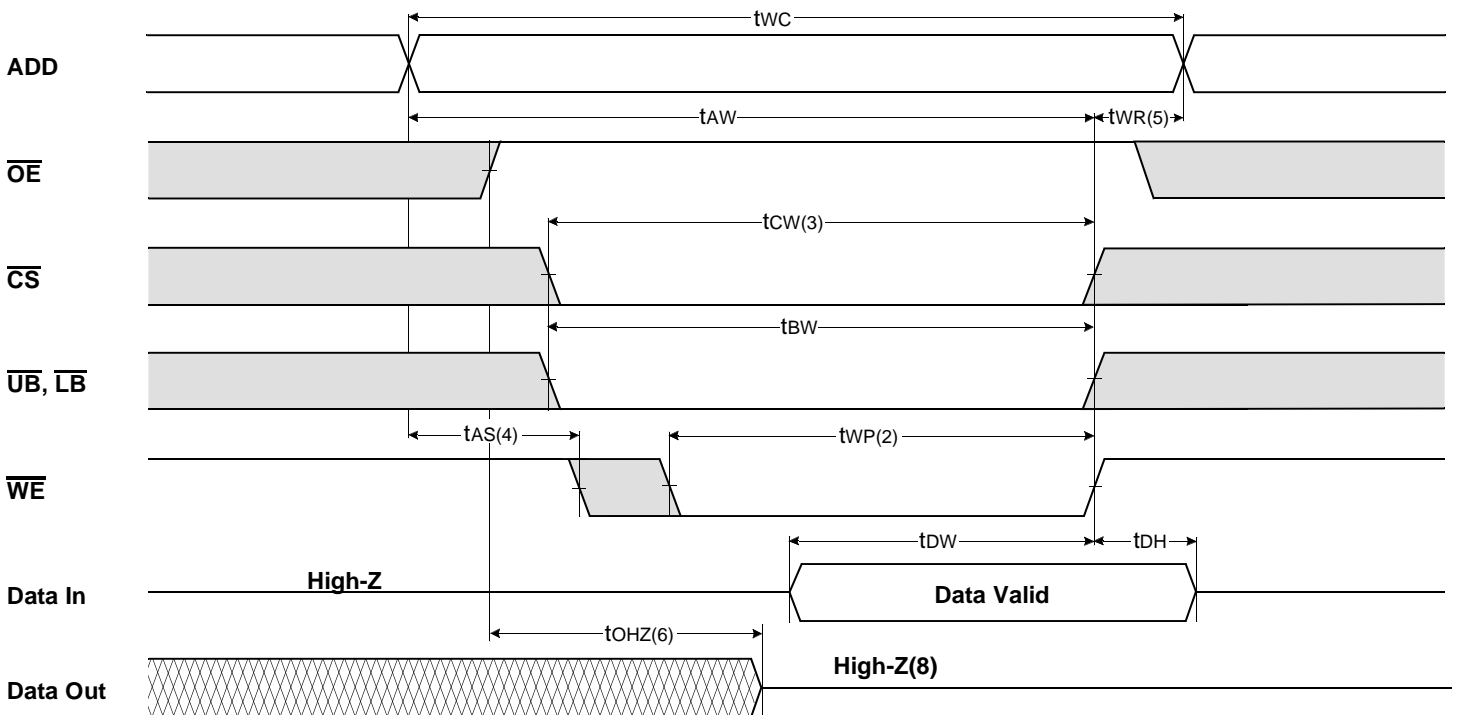
TIMING WAVE FORM OF READ CYCLE(2)  $\overline{WE}=V_{IH}$



NOTES(READ CYCLE)

1.  $\overline{WE}$  is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to  $V_{OH}$  or  $V_{OL}$  Levels.
4. At any given temperature and voltage condition, tHZ(Max.) is less than tLZ(Min.) both for a given device and from device to device.
5. Transition is measured  $\pm 20\%$  from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with  $\overline{CS}=V_{IL}$ .
7. Address valid prior to coincident with  $\overline{CS}$  transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1)  $\overline{OE}=\text{Clock}$



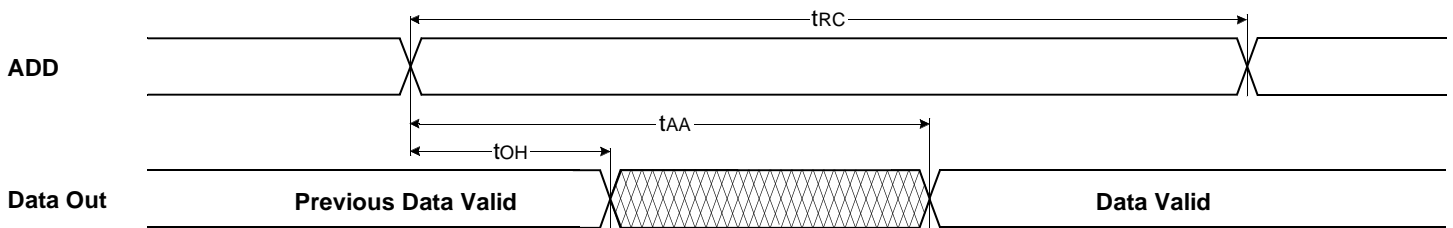
WRITE CYCLE

Parameter	Symbol	KM6164002-20		KM6164002-25		Unit
		Min	Max	Min	Max	
Write Cycle Time	tWC	20	-	25	-	Å
Chip Select to End of Write	tCW	15	-	17	-	Å
Address Set-up Time	tAS	0	-	0	-	Å
Address Valid to End of Write	tAW	15	-	17	-	Å
Write Pulse Width( $\overline{OE}$ High)	tWP	15	-	17	-	Å
Write Pulse Width( $\overline{OE}$ Low)	tWP1	20	-	25	-	Å
$\overline{UB}$ , $\overline{LB}$ Valid to End of Write	tBW	15	-	17	-	ns
Write Recovery Time	tWR	0	-	0	-	Å
Write to Output High-Z	tWHZ	0	8	0	8	Å
Data to Write Time Overlap	tDW	10	-	12	-	Å
Data Hold from Write Time	tDH	0	-	0	-	Å
End Write to Output Low-Z	tOW	3	-	4	-	Å

NOTE: Above parameters are also guaranteed at extended and industrial temperature ranges.

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) Address Controlled,  $\overline{CS}=\overline{OE}=\overline{UB}=\overline{LB}=V_{IL}$ ,  $\overline{WE}=V_{IH}$



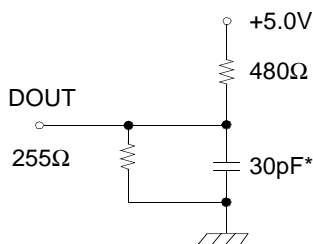
**AC CHARACTERISTICS**( $T_A=0$  to  $70^\circ\text{C}$ ,  $V_{CC}=5.0\text{V}\pm 10\%$ , unless otherwise noted.)

**TEST CONDITIONS**

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3 $\mu\text{s}$
Input and Output timing Reference Levels	1.5V
Output Loads	See below

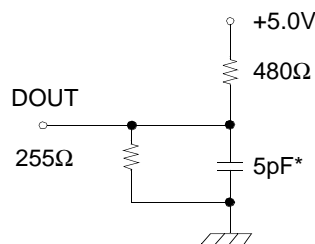
NOTE: Above test conditions are also applied at extended and industrial temperature ranges .

Output Loads(A)



Output Loads(B)

for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



\* Including Scope and Jig Capacitance

**READ CYCLE**

Parameter	Symbol	KM6164002-20		KM6164002-25		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	20	-	25	-	$\mu\text{s}$
Address Access Time	tAA	-	20	-	25	$\mu\text{s}$
Chip Select to Output	tCO	-	20	-	25	$\mu\text{s}$
Output Enable to Valid Output	tOE	-	10	-	12	$\mu\text{s}$
$\overline{\text{UB}}$ , $\overline{\text{LB}}$ Access Time	tBA	-	10	-	12	ns
Chip Enable to Low-Z Output	tLZ	5	-	5	-	$\mu\text{s}$
Output Enable to Low-Z Output	tOLZ	0	-	0	-	$\mu\text{s}$
$\overline{\text{UB}}$ , $\overline{\text{LB}}$ Enable to Low-Z Output	tBLZ	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	7	0	8	$\mu\text{s}$
Output Disable to High-Z Output	tOHZ	0	7	0	8	$\mu\text{s}$
$\overline{\text{UB}}$ , $\overline{\text{LB}}$ Disable to High-Z Output	tBHZ	0	7	0	8	ns
Output Hold from Address Change	tOH	4	-	5	-	$\mu\text{s}$

NOTE: Above parameters are also guaranteed at extended and industrial temperature ranges.

**ABSOLUTE MAXIMUM RATINGS\***

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		VIN, VOUT	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss		Vcc	-0.5 to 7.0	V
Power Dissipation		PD	1.0	W
Storage Temperature		TSTG	-65 to 150	°C
Operating Temperature	Commercial	TA	0 to 70	°C
	Extended	TA	-25 to 85	°C
	Industrial	TA	-40 to 85	°C

\* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS(TA=0 to 70°C)**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	VIH	2.2	-	Vcc+0.5**	V
Input Low Voltage	VIL	-0.5*	-	0.8	V

NOTE: Above parameters are also guaranteed at extended and industrial temperature ranges.

\* VIL(Min) = -2.0V a.c(Pulse Width ≤10ns) for I ≤20 $\bar{I}$

\*\* VIH(Max) = Vcc + 2.0V a.c (Pulse Width ≤10ns) for I ≤20 $\bar{I}$

**DC AND OPERATING CHARACTERISTICS(TA=0 to 70°C, Vcc=5.0V±10%, unless otherwise specified)**

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current	ILI	VIN = Vss to Vcc	-2	2	μA	
Output Leakage Current	ILO	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ VOUT = Vss to Vcc	-2	2	μA	
Operating Current	ICC	Min. Cycle, 100% Duty $\overline{CS}=V_{IL}$ , VIN = VIH or VIL, IOUT=0mA	20ns	-	240	$\bar{I}$
			25ns	-	220	
Standby Current	ISB	Min. Cycle, $\overline{CS}=V_{IH}$	-	60	$\bar{I}$	
	ISB1	f=0MHz, $\overline{CS} \geq V_{CC}-0.2V$ , VIN ≥ VCC-0.2V or VIN ≤ 0.2V	-	10	$\bar{I}$	
Output Low Voltage Level	VOL	IOL=8mA	-	0.4	V	
Output High Voltage Level	VOH	Ioh=-4mA	2.4	-	V	
	VOH1*	Ioh1=-0.1mA	-	3.95	V	

NOTE: Above parameters are also guaranteed at extended and industrial temperature ranges.

\* Vcc=5.0V±5% Temp. = 25°C

**CAPACITANCE\*(TA=25°C, f=1.0MHz)**

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CIO	VIO=0V	-	8	pF
Input Capacitance	CIN	VIN=0V	-	6	pF

\* NOTE : Capacitance is sampled and not 100% tested.

**256K x 16 Bit High-Speed CMOS Static RAM**

**FEATURES**

- Fast Access Time 20,25ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 60µA(Max.)
  - CMOS) : 10µA(Max.)
- Operating KM6164002 - 20 : 240µA(Max.)
- KM6164002 - 25 : 220µA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Data Byte Control :  $\overline{LB}$  : I/O1~ I/O8,  $\overline{UB}$  : I/O9~ I/O16
- Standard Pin Configuration
  - KM6164002J : 44-SOJ-400

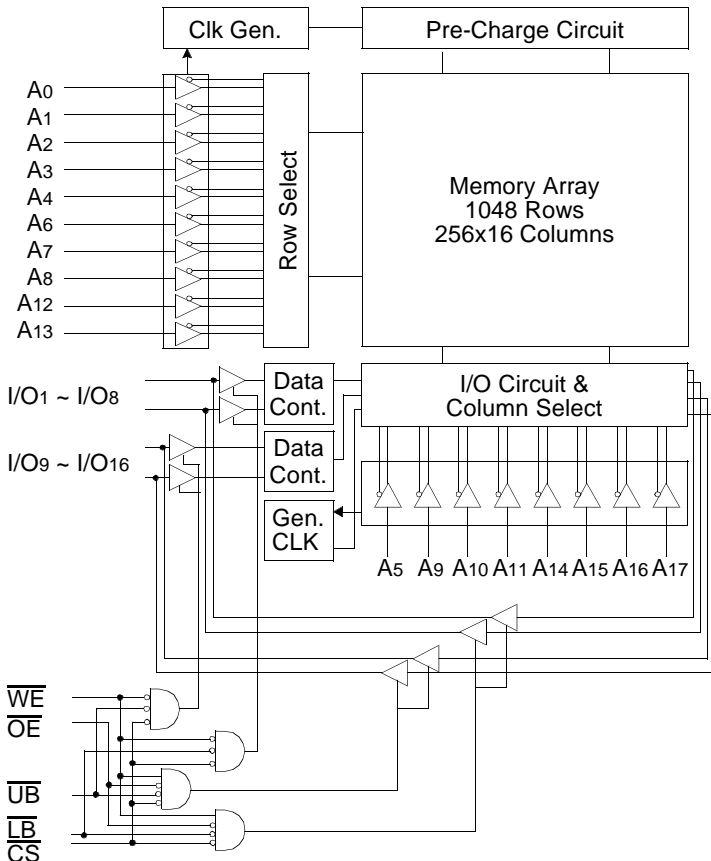
**GENERAL DESCRIPTION**

The KM6164002 is a 4,194,304-bit high-speed Static Random Access Memory organized as 262,144 words by 16 bits. The KM6164002 uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control ( $\overline{UB}$ ,  $\overline{LB}$ ). The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM6164002 is packaged in a 400mil 44-pin plastic SOJ.

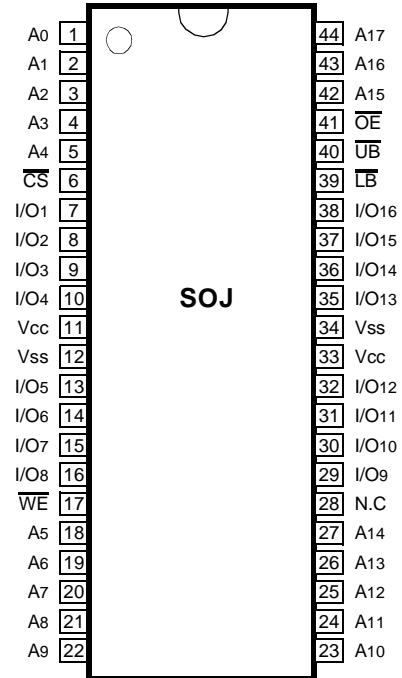
**ORDERING INFORMATION**

KM6164002 -20/25	Commercial Temp.
KM6164002E -20/25	Extended Temp.
KM6164002I -20/25	Industrial Temp.

**FUNCTIONAL BLOCK DIAGRAM**



**PIN CONFIGURATION (Top View)**



**PIN FUNCTION**

Pin Name	Pin Function
A0 - A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O1~I/O8)
$\overline{UB}$	Upper-byte Control(I/O9~I/O16)
I/O1 ~ I/O16	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground



**Document Title**

**64Kx16 Bit High Speed Static RAM(5V Operating), Revolutionary Pin out.  
Operated at Commercial, Extended and Industrial Temperature Range.**

**Revision History**

<u>Rev.No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
Rev. 0.0	Initial release with Preliminary.	Jun. 1th, 1991	Preliminary
Rev. 1.0	Release to final Data Sheet. 1.1. Delete Preliminary	Oct. 4th, 1993	Final
Rev. 2.0	2.1.Delete Low power product with Data Retention Mode. 2.1.1. Delete Data Retention Characteristics 2.2.Add Industrial and Extended Temperature Range parts with the same parameters as Commercial Temperature Range parts. 2.2.1 Add KM6164002I for Industrial Temperature Range. 2.2.2.Add KM6164002E for Extended Temperature Range. 2.2.3.Add ordering information. 2.2.4. Add the condition for operating at Industrial and Extended Temperature Range. 2.3.Add timing diagram to define tWP1 as "(Timing Wave Form of Write Cycle( $\overline{OE}$ =Low fixed))" 2.4.Delete 35ns part.	Jun. 17th, 1997	Final

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.