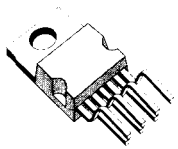
MONOLITHIC LAMP DIMMER

- HIGH EFFICIENCY DUE TO PWM CONTROL AND POWER DMOS DRIVER
- LOAD CONNECTED TO GROUND
- CURRENT LIMITATION
- OVER AND UNDERVOLTAGE PROTECTION
- ON CHIP THERMAL PROTECTION
- LIMITED AND PROGRAMMABLE OUTPUT VOLTAGE SLEW RATE
- OPEN GROUND PROTECTION
- VERY LOW STANDBY POWER CONSUMPTION
- LOAD DUMP PROTECTION
- MINIMIZED ELECTROMAGNETIC INTERFERENCE
- WIDE CHOICE IN PWM FREQUENCY RANGE
- LOAD POWER LIMITATION

MULTIPOWER BCD TECHNOLOGY

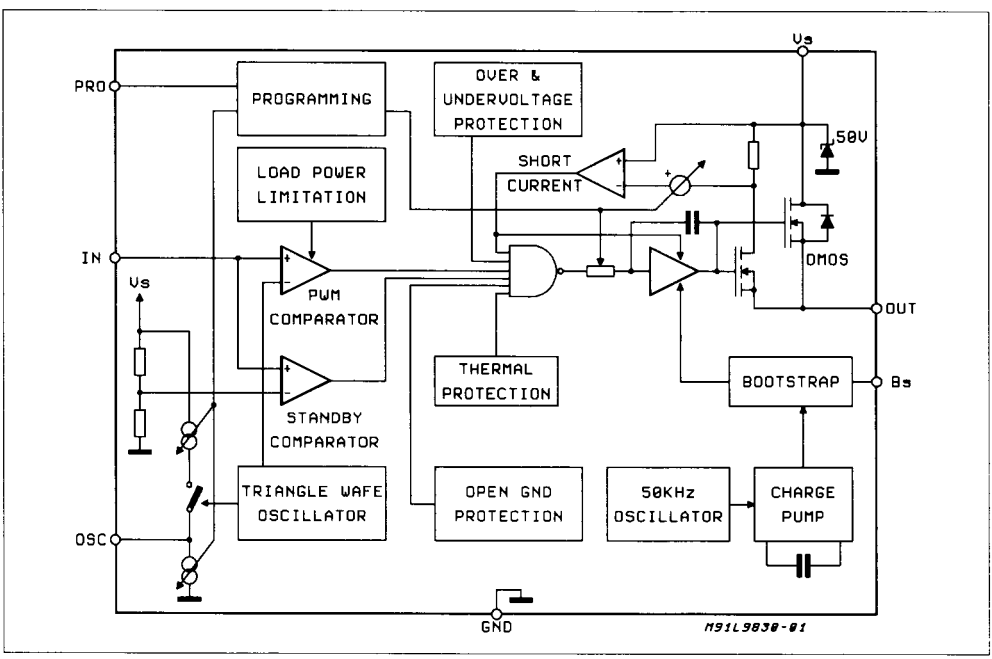


Heptawatt
ORDERING NUMBER: L9830

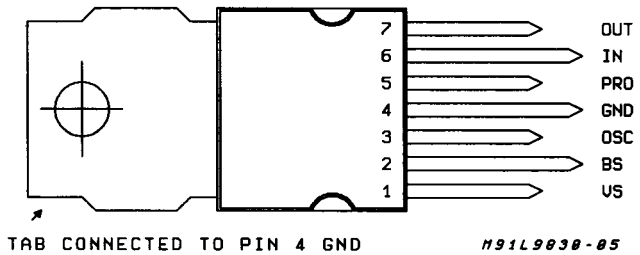
DESCRIPTION

The L9830 high side driver is a monolithic integrated circuit realized with Multipower BCD mixed technology to drive resistive loads in PWM mode with one side connected to ground.

BLOCK DIAGRAM



PIN CONNECTION (Top view)



PIN FUNCTION

PIN	NAME	DESCRIPTION
1	V_S	Common suppy connection also Drain of the power DMOS.
2	BS	A capacitor connected between this pin and the Source of the power DMOS pin Out gives the possibility to bootstrap the gate driving voltage of the power DMOS.
3	OSC	A capacitance CT connected between GND and this terminal determines the PWM switching frequency.
4	GND	Common ground connection.
5	PRO	A resistor connected between this pin and GND provide the possibility to programming the output voltage slew rate, the PWM oscillator frequency and the short current value.
6	IN	Analog input for controlling the PWM ratio, related to V_S.
7	OUT	Source connection of the internal power DMOS.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	60	V
V_{DS}	Drain Source Voltage	60	V
V_{iN}	Input Voltage	-0.3V up to V_S +0.3V	
I_S	Supply Current	±0.2	A
I_{OR}	Output Reverse Current	-2	A
P_{tot}	Power Dissipation at $T_{case} \leq 75°C$	37.5	W
T_{amb}	Operating Ambient Temperature Range	-40 to +85	°C
T_j	Operating Junction Temperature Range	-40 to 150	°C
T_{stg}	Storage Temperature	-65 to 150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	2	°C/W

ELECTRICAL CHARACTERISTICS ($6V \le V_S \le 16V$; $-40°C \le T_{amb} \le 85°C$, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{qo}	Operating Quiescent Current $I_{qo} = 11.3 \frac{V_S - 0.7V}{R_P} + 0.67mA$	$V_{IN} = V_S$ $R_P \to \infty$ $R_P = 30K\Omega$		2.4 8.5	6 18	mA mA
I_{qs}	Standby Current	$V_{IN} = 0$ $T_j \le 100°C$	0	200	600	µA
V_{INSB}	Input Standby High Threshold V_{IN}/V_S		0.1	0.15	0.2	
$V_{INSBhys}$	Input Standby Hysteresis		-350	-190	-50	mV
V_{INH}	Input High Threshold	$f_o \times t_{on} = 1$ $V_S \le VS_{LPL}$	0.95VS		V_S+0.3V	
I_{IN}	Input Current	$-0.3 \le V_{IN} \le V_S$+0.3V		1	5	µA
VS_L	Low Supply Voltage Disable High Threshold		5	5.5	6	V
VS_{Lhys}	Low Supply Voltage Disable Hysteresis		-300	-100	-50	mV
VS_{LPL}	Load Power Limitation Start Supply Voltage	$V_{IN} \ge V_{INH}$, $f_{on} \cdot t_{on} = 0.96$	12	13.0	14.5	V
VS_H	High Supply Voltage Disable High Threshold		16	17.8	20	V
VS_{Hhys}	High Supply Voltage Disable Hysteresis		-350	-190	-50	mV
VS_{LD}	Load Dump Supply Voltage Threshold	$I_q = 50mA$	45	52	55	V
I_{CLD}	Load Dump Clamping Current	$VS = 60V$	100	150	300	mA
T_{ST}	Thermal Shutdown Temperature		150	175	200	°C
T_{SThys}	Thermal Shutdown Temperature Hysteresis		-50	-40	-30	°C
K_{Ti}	Internal PWM Frequency Constant (without RP)	$f_o = K_{T/CT}$	1000	2000	3000	Hznf
K_{Te}	External PWM Frequency Constant	$f_o = \frac{1}{C_T R_P} K_{Te}$ $30K\Omega \le R_P \le 500K\Omega$	0.220	0.250	0.350	
I_{osi}	Internal Short Current Limitation (without R_P) (4)	$V_S = 12V$	3	6	9	A
I_{ose}	External Programmable Short Current Limit ($30K\Omega \le R_P \le 500K\Omega$) (3)	$V_S = 12V$, $R_P = 125K\Omega$	5	6	10	A
R_{DS}	Static Drain Source on Resistance	$V_S \ge 9V$, $I_O = 1A$		190	380	mΩ
S_i	Internal Fixed Output Voltage Slew Rate (without R_P) (1)	$V_S = 12V$; $5\Omega \le R_L \le 7\Omega$	50	120	230	V/ms
		$T_{amb} \le 25°C$	50	120	250	V/ms
S_e	External Programmable Output Voltage Slew Rate ($30K\Omega \le R_P \le 500K\Omega$) (2)	$V_S = 12V$, $R_P = 125K\Omega$ $R_L = 6\Omega$	50	120	200	V/ms
		$T_{amb} \le 25°C$	50	120	250	V/ms

Notes:

(1) $S_i = VS \cdot 11.16 \frac{1}{ms} - 7.26 \frac{V}{ms}$

(2) $S_e = \frac{R_L}{R_P} \cdot \frac{VS - 0.65V}{R_L + 0.32\Omega} 1.47 \cdot 10^6 \frac{V}{msA}$

(3) $I_{OSP} = (VS - 0.6V) \cdot \frac{64260}{R_P}$

(4) $I_{OS} = (VS - 0.6V) \cdot 0.514 \frac{A}{V}$

If R_P is not present in application an internal equivalent resistor can be inserted in the calculation with a typical value of $R_P = 125K\Omega$

FUNCTIONAL DESCRIPTION

To control the power of the load with a POWERMOS transistor in the switched mode, its gate must be driven with a PWM signal. The amplitude of the gate driving pulse must guarantee that the Power DMOS transistor will be completely saturated during the ON phase. To generate the necessary gate driving voltage a charge pump circuit is required. With this circuit a gate voltage of $2 \cdot (V_S - 1.5V) \leq VS + 16V$ typically will be obtained.

The slope of the leading and trailing edge of the gate driving pulse is defined with an internal capacitor. The important criteria for the dimensioning of the output voltage slope are the electromagnetic radiation and the power dissipation of the Power DMOS. The typical value of the output pulse slope is in the range of 120V/ms to fullfill automotive radiation requirements.

The output pulse slope is directly related to the value of the supply voltage VS and in a wide range programmable through the programming resistance R_P.

$$S = \frac{dV_{out}}{dt} = R_L \cdot \frac{dI_{load}}{dt} = \frac{R_L}{R_P} \cdot \frac{VS - 0.65V}{R_L + 0.32\Omega} \cdot 1.47 \frac{10^6\ V}{Ams}$$

The value of the gate voltage slope due to the POWERMOS parasitic capacitors must be in a relation to the charge pump performance. For fast gate voltage variation the bootstrap option can be used. The bootstrap capacitance should have a relation greater than 50 to the DMOS parasitic capacitors and should be in the range of

$$C_{BS} \geq 100nF$$

The switching frequency "f_O" is defined with a triangle oscillator and it's programmed with the capacitor C_T, or C_T and R_P if a greater precision is required.

$$f_O = K_T/C_T \text{ (without } R_P)$$

$$f_O = \frac{1}{4C_TR_P} \text{ (with } R_P)$$

The modulation factor of the PWM driving signal of the external Power DMOS transistor is defined with the voltage level at the analog input. Fig. 1 shows the typical transfer curve giving the PWM factor as a function of the input/supply voltage ratio.

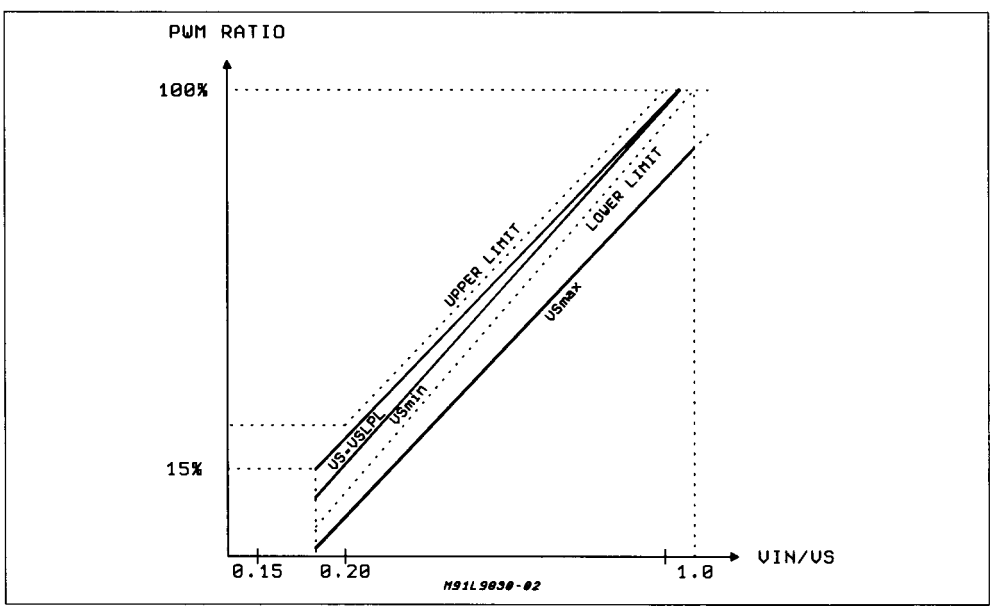
For higher supply voltage values, the power limitation circuitry will linearly reduce the PWM ratio to achive a constant load power to extend the lamps life time.

The input voltage is referred to the supply voltage. The regulation of the PWM factor can be realized with a potentiometer connected to the supply voltage and the analog input, see the typical application circuit diagram.

The maximum load current in the short circuit condition is limited internally with a sense DMOS cell.

The value of the short current is a multiple of the programming current flowing through R_P or the in-

Figure 1: Transfer Characteristc



ternal fixed resistance. Threfore this short current value is supply voltage dependent to achieve in any condition the lamp required warm up current which will be normally two or three times higher.

$$I_{OSe} = \frac{VS - 0.6V}{R_P} \cdot 64260$$

If the short current condition is detected the gate will be driven with a DC voltage which value is regulated to maintain the specified current. With this function the switch ON phase for each load will be speeded up.

The circuit features also a protection which allows to withstand high overvoltage for a limited time (load dump in automotive application). Above the VS_H threshold the gate driving of the POWERMOS transistor is switched OFF and the gate is held at the GND potential. When the V_{BAT} rises above the internal supply clamp voltage VS_{LD} the clamping diode becomes active with a serial resistance of R_{LD} and the gate voltage is floating with the GND potential. At this time the current flowing through the load is not limited. In this condition the load voltage can be calculated to

$$V_L = VS = VS_{LD} - VS_{GS} \qquad V_{GS} << VS_{LD}$$

This device is protected against temperature destruction through an internal power dissipation protection. The total power dissipation of the device can be calculated with:

for $VS_L \le VS \le VS_{LPL}$:

$$P_{tot} = VS^2 \cdot \left(\frac{R_{DS}}{(R_{DS} + R_L)^2} + \frac{f_O}{S} \cdot \left(1 - \frac{R_{DS}}{R_{DS} + R_L}\right) \cdot \left(1 - \frac{R_{DS}}{R_{DS} + R_L}\right) \cdot \left(1 + \frac{2VS}{R_{DS} + R_L}\right) \right)$$

and for $VS_{LPL} \le VS \le VS_H$:

$$P_{tot} = V^2_{SLPL} \cdot \frac{R_{DS}}{(R_{DS} + R_L)} + \frac{VS^2 \, f_O}{S} \cdot \left(1 - \frac{R_{ON}{}^2}{R_{ON} + R_L}\right)$$

Figure 2: Total Power Dissipation Characteristic

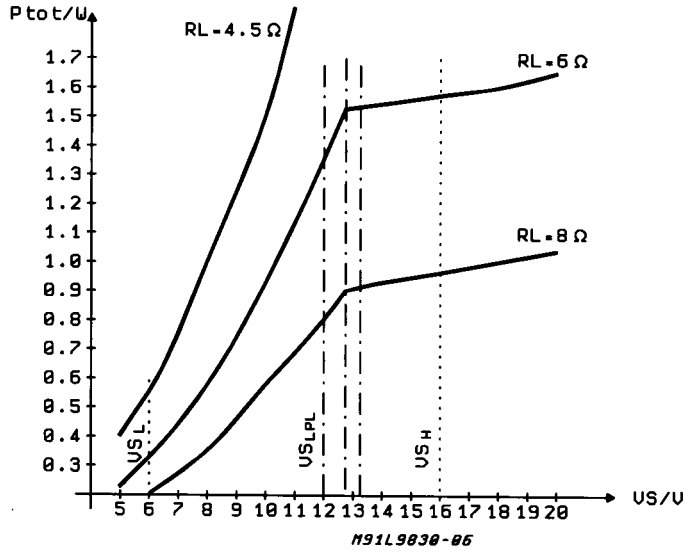
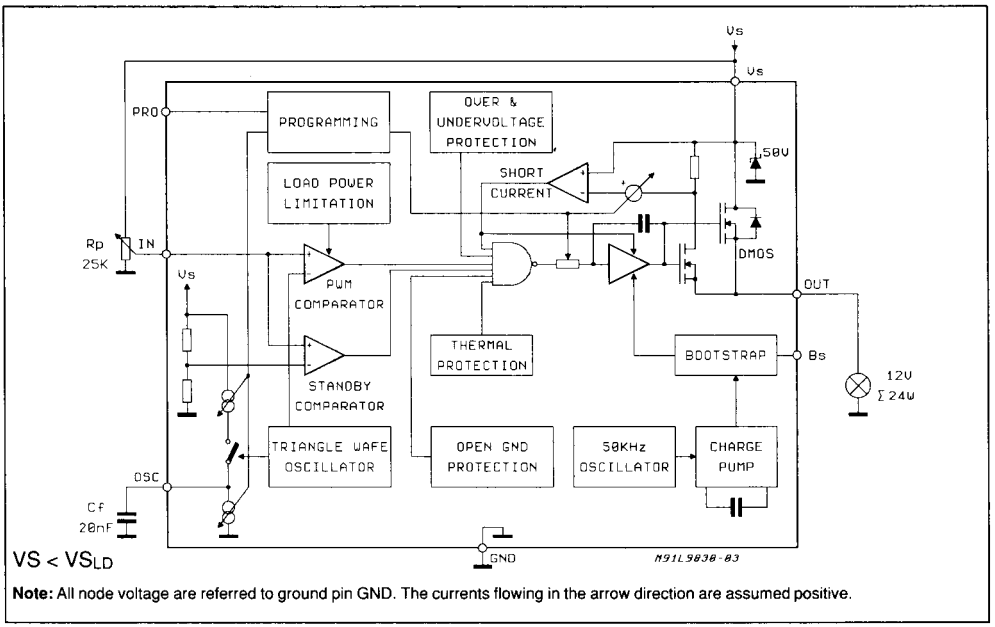
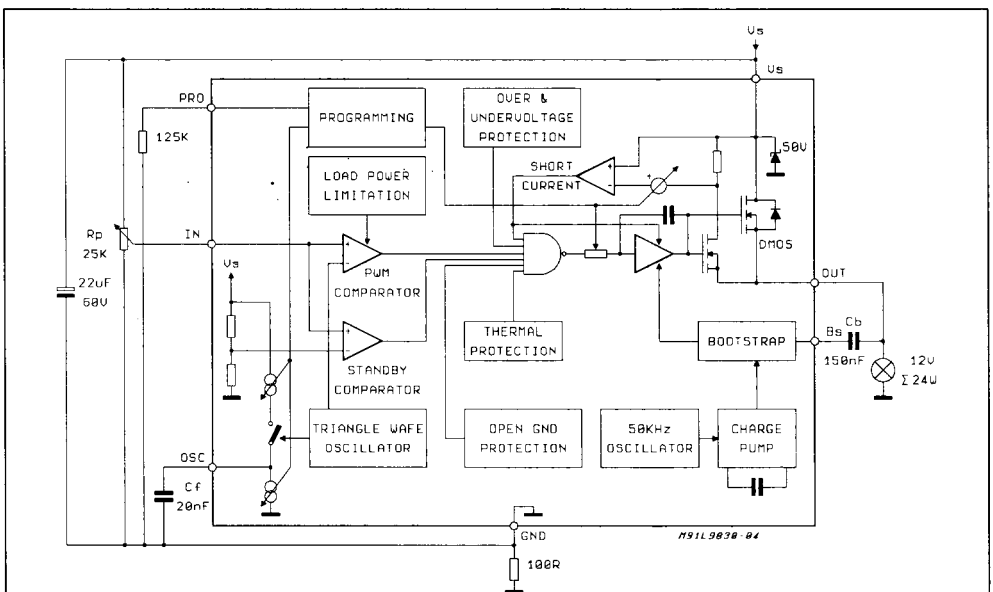


Figure 3: Application Circuit Diagram for Dashboard Dimming



Note: All node voltage are referred to ground pin GND. The currents flowing in the arrow direction are assumed positive.

Figure 4: Application Circuit Diagram for Dashboard Dimming with Optimized Device Power Dissipation



Note: All node voltage are referred to ground pin GND. The currents flowing in the arrow direction are assumed positive.