LX1684

Voltage-Mode PWM Controller

PRODUCTION

DESCRIPTION

The LX1684 is a monolithic, voltage-mode pulse-width modulator controller. It is designed to implement a flexible, low cost buck (step-down) regulator supply with a minimal of external components.

The LX1684 has a synchronous driver for higher efficiency and is optimized to provide 12V to 3.3V or 12V to 2.5V regulation. It also can be used to convert 5V or 3.3V to voltages as low as 1.25V.

Switching frequency is fixed at 175kHz for optimal cost and space. Short-circuit current limiting can be implemented without expensive current sense resistors.

Similar to the LX1682 in function but with the positive side of the current sense comparator brought out (CSP) to allow it to be referenced to the topside FET.

Current is sensed using the voltage drop across the $R_{DS(ON)}$ of the MOSFET this sensing is delayed for 1µs to eliminate MOSFET ringing errors. Hiccup-mode fault protection reduces average power to the power elements during short-circuit conditions.

Under-voltage lockout and soft-start are provided for optimal start-up performance. Pulling the soft-start pin to ground can disable the LX1684.

The small 14-pin SOIC packaging, combined with low profile, low ESR capacitors, and TO-252 packaged FETs results in a high efficiency converter in a small board area. In most cases PCB copper can accomplish necessary heat sinking and no bulky additional heat sinks are required.

If a low profile design is not required small electrolytic capacitors can be used reducing the overall converter cost.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: **http://www.microsemi.com**

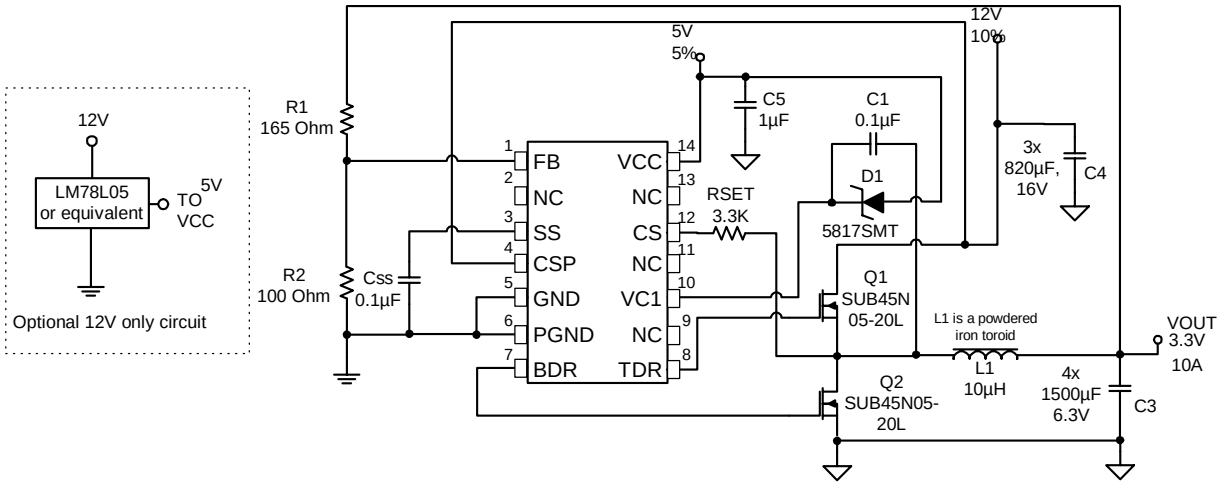
KEY FEATURES

- Fixed 175kHz Switching Frequency
- Constant Frequency Voltage-Mode Control Requires No External Compensation
- Hiccup-Mode Over-Current Protection
- High Efficiency
- Output Voltage Set By Resistor Divider
- Under-Voltage Lockout
- Soft-Start And Enable
- Synchronous Rectification
- Small, 14-pin Surface Mount Package

APPLICATIONS

- 12V to 3.3V Or Less Buck Regulators
- 3.3/5V to 2.5V Or Less Buck Regulators
- Hard Disk Drives
- Computer Add-on Cards

PRODUCT HIGHLIGHT - TYPICAL 12V TO 3.3V APPLICATION



PACKAGE ORDER INFO

T_A (°C)	OUTPUT	D Plastic SOIC 14-PIN
0 to 70	Synchronous	LX1684CD

Note: Available in Tape & Reel.
Append the letter "T" to the part number. (i.e. LX1684CDT)

Rev. 1.0, 2001-09-19

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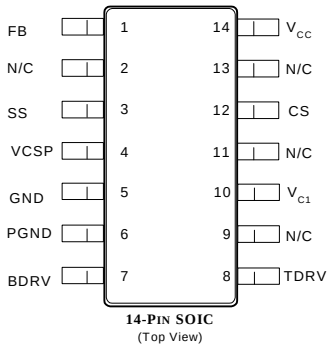
ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Supply Voltage (V_{C1}) 18V
Supply Voltage (V_{CC}) 7V
Input Voltage (CSP Pin) 14V
Output Drive Peak Current Source (500ns) 1.0A
Output Drive Peak Current Sink (500ns) 1.0A
Input Voltage (SS/ENABLE Pin) ..... -0.3 to 6V
Operating Junction Temperature ..... 150°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10 Seconds) ..... 300°C

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

PACKAGE PIN OUT



14-PIN SOIC
(Top View)

THERMAL DATA

D PACKAGE

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	165°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

FUNCTIONAL PIN DESCRIPTION

PIN NAME	DESCRIPTION
V_{FB}	Voltage Feedback. A 1.25V reference is connected to a resistor divider to set desired output voltage.
SS	Soft-Start And Hiccup Capacitor Pin. During start up the voltage of this pin controls the output voltage. An internal 22kΩ resistor and the external capacitor set the time constant for soft-startup. Soft-start does not begin until the supply voltage exceeds the UVLO threshold. When over-current occurs, this capacitor is used for timing hiccup. The PWM can be disabled by pulling the SS pin below 0.3V
VCSP	Positive Over-Current Threshold Input
GND	Analog ground for SS, FB, CS and VCC.
PGND	MOSFET driver power ground
TDRV	Gate Drive For Upper MOSFET.
BDRV	Gate Drive For Lower MOSFET.
V_{C1}	Separate Supply For MOSFET Gate Drives. Connect to gate drive voltage.
CS	Over-Current Set. Connect resistor between CS pin and the source of the upper MOSFET to set current-limit point.
V_{CC}	IC Supply Voltage (nominal 5V).

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ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature $0°C \leq T_A \leq 70°C$ except where otherwise noted. Test conditions: V_{CC}=5V, V_{C1}=16V

Parameter	Symbol	Test Conditions	LX1684			Units
			Min	Typ	Max	
REFERENCE						
Reference Voltage	V_{FB}	$V_{OUT}=V_{FB}$, T_A=25°C	1.237	1.25	1.262	V
		$V_{OUT}=V_{FB}$, $0°C \leq T_A \leq 70°C$	1.231		1.269	V
OSCILLATOR						
Frequency	F_{OSC}		135	175	200	kHz
Ramp Amplitude	V_{RAMP}			1.25		VPP
ERROR AMPLIFIER						
Input Resistance	R_{IN}	$V_{OUT} = V_{FB}$		20		kΩ
CURRENT SENSE						
Current Set	I_{SET}	$V_{CS} = V_{CC} - 0.4V$	40	45		µA
V_{TRIP}			300	380	420	mV
Current Sense Delayed	T_{CSD}			1.0		µsec
OUTPUT DRIVERS						
Drive Rise Time, Fall Time	T_{RF}	C_L = 3000pF		50		nS
Drive High	V_{DH}	I_{SOURCE} = 20mA, V_{C1}=16V	13	14		V
Drive Low	V_{DL}	I_{SINK} = 20mA, V_{C1} =16V		0.1	0.2	V
UVLO AND SOFT-START (SS)						
V_{CC5} Start-Up Threshold	V_{ST}	V_{C1} > 4.0V	4.0	4.25	4.5	V
Hysteresis				0.10		V
SS Resistor	R_{SS}			22		kΩ
SS Output Enable	V_{EN}		0.25	0.3	0.35	V
Hiccup Duty Cycle	DC_{HIC}	C_{SS} = 0.1µF, F_{REQ} =100Hz		12	14	%
SUPPLY CURRENT						
V_{C1} Dynamic Supply Current	I_{CD}	Out Freq = 175kHz, C_L=3000pF, Synch., V_{SS} > 0.3V		30	40	mA
Static Supply Current V_{C1}	I_{VC1}	V_{SS} < 0.3V ; outputs low (disable), V_{C1} = 16V		7	9	mA
5V	I_{VCC}	V_{SS} > 0.3V ; outputs low (disable)		9	12	mA

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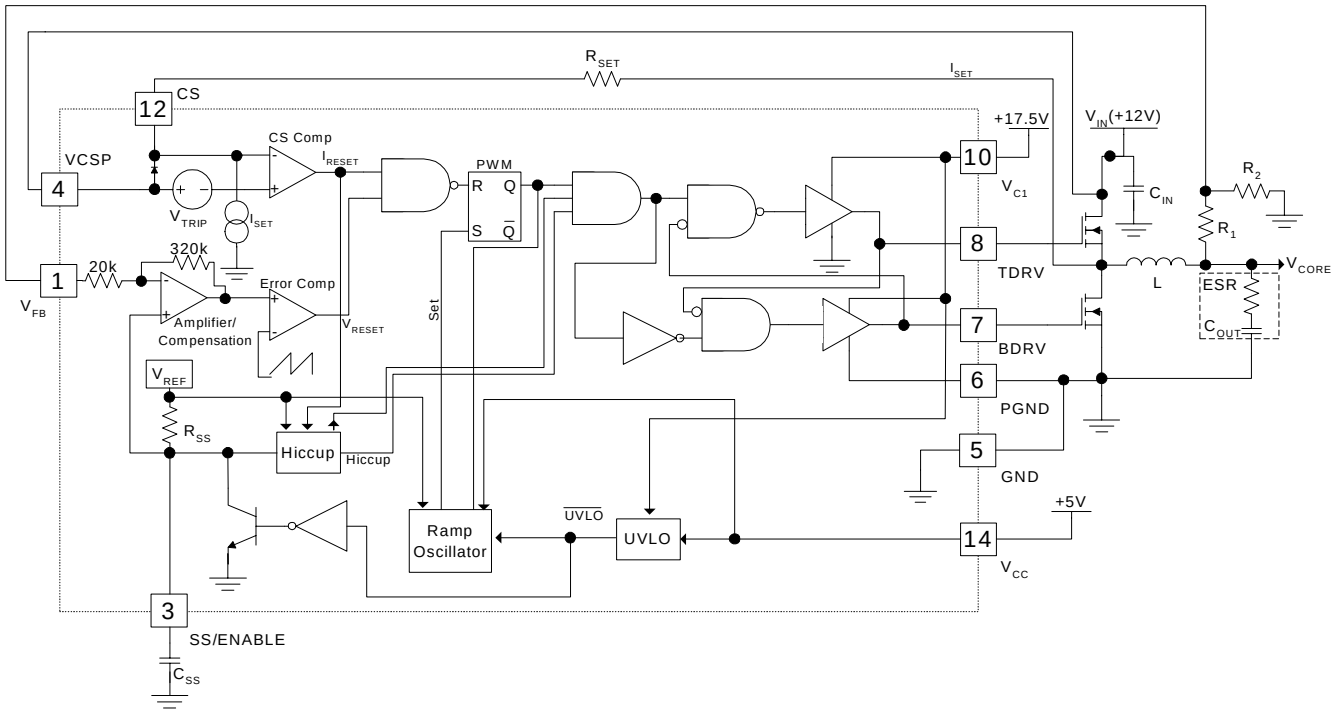
BLOCK DIAGRAM



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THEORY OF OPERATION

GENERAL DESCRIPTION

The LX1684 is a voltage-mode pulse-width modulation controller integrated circuit. The internal oscillator and ramp generator frequency is fixed at 175kHz. The devices have internal compensation, so that no external compensation is required.

POWER UP AND INITIALIZATION

At power up, the LX1684 monitors the supply voltage to both the +5V and the V_{C1} pins (there is no special requirement for the sequence of the two supplies). Before both supplies reach their under-voltage lock-out (UVLO) thresholds, the soft-start (SS) pin is held low to prevent soft-start from beginning; the oscillator control is disabled and the top MOSFET is kept OFF.

SOFT-START

Once the supplies are above the UVLO threshold, the soft-start capacitor begins to be charged up by the reference through a 20k internal resistor. The capacitor voltage at the SS pin rises as a simple RC circuit. The SS pin is connected to the amplifier's non-inverting input that controls the output voltage. The output voltage will follow the SS pin voltage if sufficient charging current is provided to the output capacitor. The simple RC soft-start allows the output to rise faster at the beginning and slower at the end of the soft-start interval. Thus, the required charging current into the output capacitor is less at the end of the soft-start interval so decreasing the possibility of an over-current. A comparator monitors the SS pin voltage and indicates the end of soft-start when SS pin voltage reaches 95% of V_{REF} .

OVER-CURRENT PROTECTION (OCP) AND HICCUP

The LX1684 uses the RDS(ON) of the upper MOSFET, together with a resistor (RSET) to set the actual current limit point. Unlike the LX1681/2 controllers the LX1684 includes the positive current sense comparator input providing true Kelvin sensing which is more accurate and offers more noise immunity. This Kelvin sensing also simplifies the PCB layout for current sense. The CSP pin has a useful common mode input range to about 14V. The comparator senses the current 1µs after the top MOSFET is switched on.

Experiments have shown that the MOSFET drain voltage will ring for 200-500ns after the gate is turned on. In order to reduce inaccuracies due to ringing, a 1µs blanking delay after gate turn-on is built into the current sense comparator. This 1us delay reduces the effectiveness of the current sense comparator when the output pulse width is below 1us. This can be problem when the set application output voltage is less than 3.0V with a 12V input. Under this condition the output current limit protection will not function properly. This is usually not true with a short circuit current condition, which causes the on time to be greater than the blanking delay. In this circumstance the current limit comparator would turn off the top FET driver.

The comparator draws a current (ISET), whose magnitude is 45µA. The set resistor is selected to set the current limit for the application. When the sensed voltage across the RDS(ON) plus the set resistor exceeds the 400mV VTRIP threshold, the OCP comparator outputs a signal to reset the PWM latch and to start hiccup mode. The soft-start capacitor (CSS) is discharged slowly (10 times slower than when being charged up by RSS). When the voltage on the SS/ENABLE pin reaches a 0.3V threshold, hiccup finishes and the circuit soft-starts again. During hiccup, the top MOSFET is OFF and the bottom MOSFET remains ON. Hiccup is disabled during the soft-start interval, allowing the circuit to start up with the maximum current. If the rise speed of the output voltage is too fast, the required charging current to the output capacitor may be higher than the limit-current. In this case, the peak MOSFET current is regulated to the limit-current by the current-sense comparator. If the MOSFET current still reaches its limit after the soft-start finishes, the hiccup is triggered again. The hiccup ensures the average heat generation on both MOSFET's and the average current to be much less than that in normal operation, if the output has a short circuit. Over-current protection can also be implemented using a sense resistor, instead of using the RDS(ON) of the upper MOSFET, for greater set-point accuracy. See Application Information section.

OSCILLATOR FREQUENCY

An internal oscillator sets the switching frequency at about 175 kHz.

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APPLICATION INFORMATION

OUTPUT INDUCTOR

The output inductor should be selected to meet the requirements of the output voltage ripple in steady-state operation and the inductor current slew-rate during transient. The peak-to-peak output voltage ripple is:

$$V_{RIPPLE} = ESR \times I_{RIPPLE}$$

where

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT})}{f_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

I_{RIPPLE} is the inductor ripple current, L is the output inductor value and ESR is the Effective Series Resistance of the output capacitor.

I_{RIPPLE} should typically be in the range of 20% to 40% of the maximum output current. Higher inductance results in lower output voltage ripple, allowing slightly higher ESR to satisfy the transient specification. Higher inductance also slows the inductor current slew rate in response to the load-current step change, ΔI, resulting in more output-capacitor voltage droop. The inductor-current rise and fall times are:

$$T_{RISE} = \frac{L \times \Delta I}{(V_{IN} - V_{OUT})}$$

and

$$T_{FALL} = \frac{L \times \Delta I}{V_{OUT}}$$

When using electrolytic capacitors, the capacitor voltage droop is usually negligible, due to the large capacitance.

OUTPUT CAPACITOR

The output capacitor is sized to meet ripple and transient performance specifications. Effective Series Resistance (ESR) is a critical parameter. When a step load current occurs, the output voltage will have a step that equals the product of the ESR and the current step, ΔI. In an advanced microprocessor power supply, the output capacitor is usually selected for ESR instead of capacitance or RMS current capability. A capacitor that satisfies the ESR requirement usually has a larger capacitance and current capability than strictly needed. The allowed ESR can be found by:

$$ESR \times (I_{RIPPLE} + \Delta I) < V_{EX}$$

where I_{RIPPLE} is the inductor ripple current, ΔI is the maximum load current step change, and V_{EX} is the allowed output voltage excursion in the transient.

OUTPUT CAPACITOR (continued)

Electrolytic capacitors can be used for the output capacitor, but are less stable with age than tantalum capacitors. As they age, their ESR degrades, reducing the system performance and increasing the risk of failure. It is recommended that multiple parallel capacitors be used, so that, as ESR increases with age, overall performance will still meet the processor's requirements.

There is frequently strong pressure to use the least expensive components possible, however, this could lead to degraded long-term reliability, especially in the case of filter capacitors. Linfinity's demonstration boards use Sanyo MV-GX filter capacitors, which are aluminum electrolytic, and have demonstrated reliability. The Oscon series from Sanyo generally provides the very best performance in terms of long term ESR stability and general reliability, but at a substantial cost penalty. The MV-GX series provides excellent ESR performance at a reasonable cost. Beware of off-brand, very low-cost filter capacitors, which have been shown to degrade in both ESR and general electrolytic characteristics over time.

INPUT CAPACITOR

The input capacitor and the input inductor are to filter the pulsating current generated by the buck converter to reduce interference to other circuits connected to the same 12V rail. In addition, the input capacitor provides local de-coupling the buck converter. The capacitor should be rated to handle the RMS current requirement. The RMS current is:

$$I_{RMS} = I_L \sqrt{d(1-d)}$$

where I_L is the inductor current and the d is the duty cycle. The maximum value, when d = 50%, $I_{RMS} = 0.5 I_L$. For 12V input and output in the range of 3V, the required RMS current is very close to $0.43 I_L$.

SOFT-START CAPACITOR

The value of the soft-start capacitor determines how fast the output voltage rises and how large the inductor current is required to charge the output capacitor. The output voltage will follow the voltage at SS pin if the required inductor current does not exceed the maximum current in the inductor. The SS pin voltage can be expressed as:

$$V_{SS} = V_{SET}(1 - e^{-t / R_{SS}C_{SS}})$$

where V_{SET} is the reference voltage. R_{SS} and C_{SS} are soft start resistor and capacitor. The required inductor current for the output capacitor to follow the SS-pin voltage equals the required capacitor current plus the load current. The soft-start capacitor should be selected so that the overall inductor current does not exceed its maximum.

APPLICATION INFORMATION

SOFT-START CAPACITOR (continued)

The capacitor current to follow the SS-pin voltage is:

$$I_{COUT} = C_{OUT}\frac{dV}{dt} = \frac{C_{OUT}}{C_{SS}} \times e^{-(t/R_{SS}C_{SS})}$$

where C_{OUT} is the output capacitance. The typical value of C_{SS} should be in the range of 0.1 to 0.2µF.

During the soft-start interval the load current from a microprocessor is negligible; therefore, the capacitor current is approximately the required inductor current.

OVER-CURRENT PROTECTION

Current limiting occurs at current level I_{CL}, when the voltage detected by the current sense comparator is greater than the current sense comparator threshold, V_{TRIP} (400mV).

$$I_{CL} \times R_{DS(ON)} + I_{SET} \times R_{SET} = V_{TRIP}$$

So,

$$R_{SET} = \frac{V_{TRIP} - I_{CL} \times R_{DS(ON)}}{I_{SET}}$$

$$R_{SET} = \frac{400mV - I_{CL} \times R_{DS(ON)}}{45\mu A}$$

Example:

For 10A current limit, using SUB45N05-20L MOSFET (20mΩ $R_{DS(ON)}$):

$$R_{SET} = \frac{0.4 - 10 \times 0.020}{45 \times 10^{-6}} = 4.42k\Omega$$

Current Sensing Using Sense Resistor

The method of current sensing using the $R_{DS(ON)}$ of the upper MOSFET is economical, but can have a large tolerance, since the $R_{DS(ON)}$ can vary with temperature, etc. A more accurate alternative is to use an external sense resistor (R_{SENSE}). The sense resistor could be a PCB trace (for construction details, see Application Note AN-10 or LX1668 data sheet). The over-current trip point is calculated as in the equations above, replacing $R_{DS(ON)}$ with R_{SENSE}.

Example:

For 10A current limit, using a 5mΩ sense resistor:

$$R_{SET} = \frac{V_{TRIP} - (I_{CL} \times R_{SENSE})}{I_{SET}}$$

$$R_{SET} = \frac{0.4 - 10 \times 0.005}{45 \times 10^{-6}} = 7.8k\Omega$$

OUTPUT ENABLE

The LX1684 FET driver outputs are driven to ground by pulling the soft-start pin below 0.3V.

PROGRAMMING THE OUTPUT VOLTAGE

The output voltage is sensed by the feedback pin (V_{FB}) which has a 1.25V reference. The output voltage can be set to any voltage above 1.25V (and lower than the input voltage) by means of a resistor divider (see Product Highlight).

$$V_{OUT} = V_{REF}(1 + \frac{R_1}{R_2})$$

Note: Keep R_1 and R_2 close to 100Ω (order of magnitude).

FET SELECTION

To insure reliable operation, the operating junction temperature of the FET switches must be kept below certain limits. The Intel specification states that 115°C maximum junction temperature should be maintained with an ambient of 50°C. This is achieved by properly derating the part, and by adequate heat sinking. One of the most critical parameters for FET selection is the $R_{DS(ON)}$ resistance. This parameter directly contributes to the power dissipation of the FET devices, and thus impacts heat sink design, mechanical layout, and reliability. In general, the larger the current handling capability of the FET, the lower the $R_{DS(ON)}$ will be, since more die area is available.

TABLE 1 - FET Selection Guide

This table gives selection of suitable FETs from VISHAY

Device	V_{DS} (V)	$R_{DS(ON)}$ @4.5V (mΩ)	$R_{DS(ON)}$ @10V (mΩ)	Gate Charge typ(nC)
D^2PAK and TO-220				
SUB70N03-09BP	30	13	9	15.5
SUB45N03-13L	30	20	13	45
SUB45N05-20L	40	20	18	43
SUB70N04-10	40	14	10	50
SO-8				
Si4810DY	30	20	13.5	20
Si4812DY	30	28	18	16

Heat Dissipated In Upper MOSFET

The heat dissipated in the top MOSFET will be:

$$P_D = (I^2 \times R_{DS(ON)} \times Duty\ Cycle) + (0.5 \times I \times V_{IN} \times t_{SW} \times f_S)$$

Where t_{SW} is switching transition line for body diode (~100ns) and f_S is the switching frequency.

For the SUB70N03-09BP (13mΩ $R_{DS(ON)}$), converting 12V to 3.3V at 15A will result in typical heat dissipation of 2.6W.

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APPLICATION INFORMATION

FET SELECTION (continued)

Synchronous Rectification – Lower MOSFET

The lower pass element can be either a MOSFET or a Schottky diode. The use of a MOSFET (synchronous rectification) will result in higher efficiency, but at higher cost than using a Schottky diode (non-synchronous). Power dissipated in the bottom MOSFET will be:

$$P_D = I^2 \times R_{DS(ON)} \times [1 - Duty\ Cycle] = 3.26W$$

[SUB45N03-13L or 2.12W for the SUB70N03-09BP]

Non-Synchronous Operation - Schottky Diode

A typical Schottky diode, with a forward drop of 0.6V will dissipate 0.6 * 15 * [1 – 3.3/12] = 6.5W (compared to the 2.1 to 4.2W dissipated by a MOSFET under the same conditions). This power loss becomes much more significant at lower duty cycles. The use of a dual Schottky diode in a single TO-220 package (e.g. the MBR2535) helps improve thermal dissipation.

Boost Operation

The LX1684 needs a secondary supply voltage (V_{C1}) to provide sufficient drive to the upper MOSFET. The top FET must be a logic level power MOSFET such as SUB45N03-13L. It must be able to turn on to a low $R_{DS(ON)}$ with V_{GS} of 4.5V or higher. V_{C1} can be generated using a bootstrap (charge pump) circuit, as shown in the Product Highlight on page 1. The capacitor, (C_1) is alternatively charged up from 5V via the Schottky diode, (D_1), and then boosted up when the FET is turned on. Under any circumstance the voltage at V_{C1} should not be more than 18V for more than 300nS and must not be greater than 19V for more than 50nS. Lab evaluation and module production test should be the final arbiter to verify the proper operation. For application with a large MOSFET, the maximum voltage at V_{C1} should be kept lower due to thermal dissipation in the FET driver section. It is inherent in a higher current power supply that the parasitic inductance and capacitance on PCB board and Power MOSFET device induces ringing at the gate drive. The extra thermal dissipation and the higher peak voltage generated by gate ringing should be taken in account during final design. The temperature rise due to gate drive thermal dissipation can be reduced by extra heat sinking. A resistor in series with the gate in order of 10ohm or snubber circuitry can reduce the gate ringing. The voltage must provide sufficient gate drive to the external MOSFET in order to get a low $R_{DS(ON)}$ and MUST be lower than maximum voltage rating of 18V.

Note that using the bootstrap circuit in synchronous rectification mode is likely to result in faster turn-on than in non-synchronous mode.

LAYOUT GUIDELINES - THERMAL DESIGN

A great deal of time and effort were spent optimizing the thermal design of the demonstration boards. Any user who intends to implement an embedded motherboard would be well advised to carefully read and follow these guidelines.

If the FET switches have been carefully selected, external heatsinking is generally not required. However, this means that copper trace on the PC board must now be used. This is a potential trouble spot; as much copper area as possible must be dedicated to heatsinking the FET switches, and the diode as well if a non-synchronous solution is used..

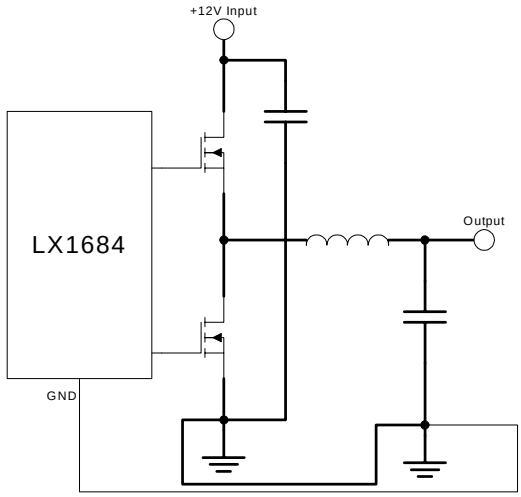

FIGURE 2 — Key Power PCB Traces

General Notes

As always, be sure to provide local capacitive decoupling close to the chip. Be sure use ground plane construction for all high-frequency work. Use low ESR capacitors where justified, but be alert for damping and ringing problems. High-frequency designs demand careful routing and layout, and may require several iterations to achieve desired performance levels.

Power Traces

To reduce power losses due to ohmic resistance, careful consideration should be given to the layout of traces that carry high currents. The main paths to consider are:

- Input power from 12V supply to drain of top MOSFET.
- Trace between top MOSFET and lower MOSFET or Schottky diode.
- Trace between lower MOSFET or Schottky diode and ground.
- Trace between source of top MOSFET and inductor and load.

All of these traces should be made as wide and thick as possible, in order to minimize resistance and hence power losses. It is also recommended that, whenever possible, the ground, input and output power signals should be on separate planes (PCB layers). See Figure 2 – bold traces are power traces.

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TYPICAL APPLICATION

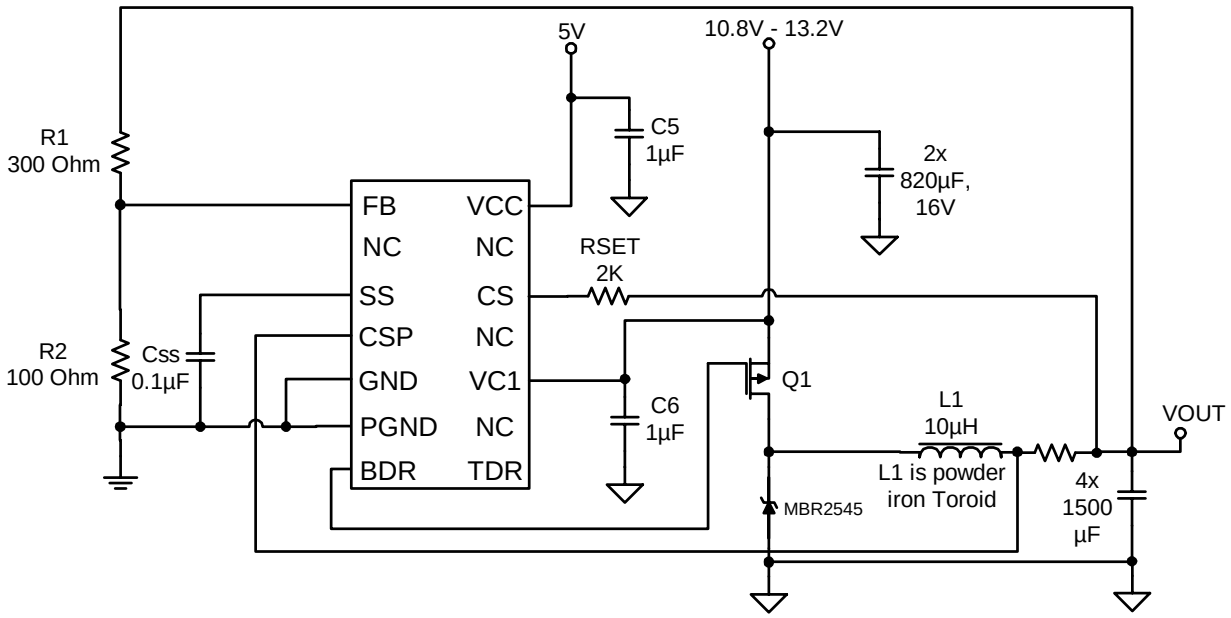

Figure 3 – 12V to 5V with P-MOSFET. No Charge Pump is Needed.

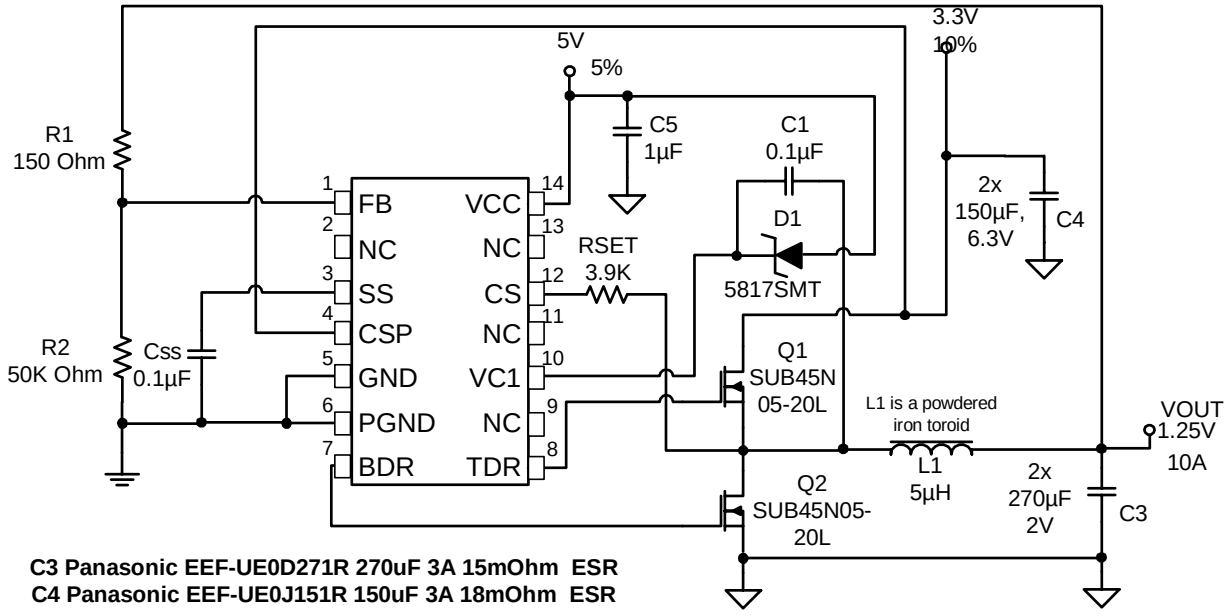

Figure 4 – 3.3V to 1.25V with Charge Pump.

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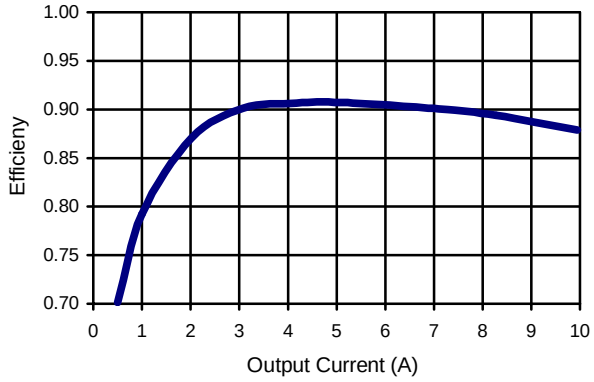
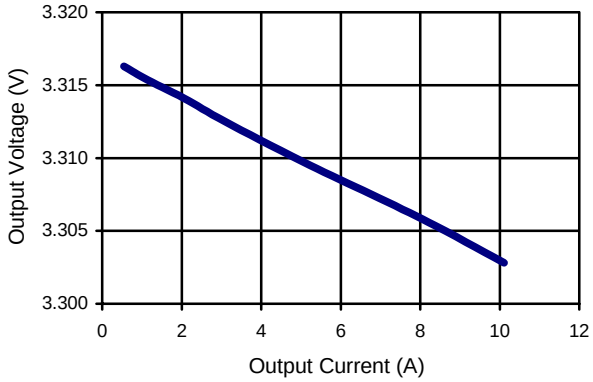
CHARACTERIZATION CHARTS

SEE PRODUCT HIGHLIGHT SCHEMATIC
Typical 12V to 3.3V application

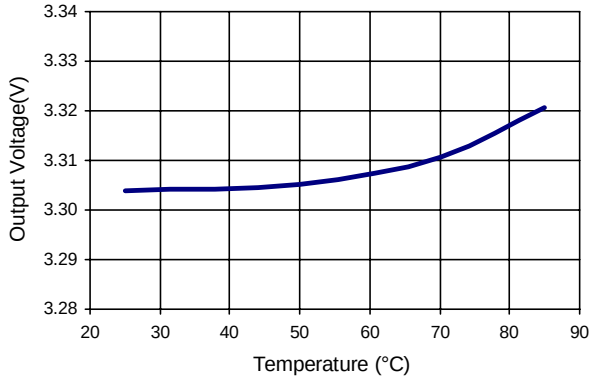
EFFICENCY VS. OUTPUT CURRENT



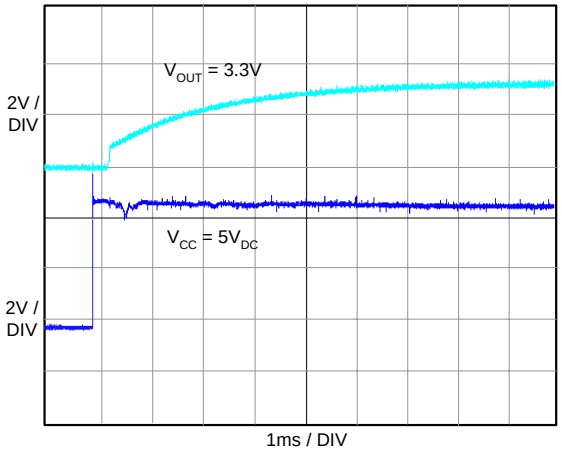
OUTPUT VOLTAGE VS. LOAD



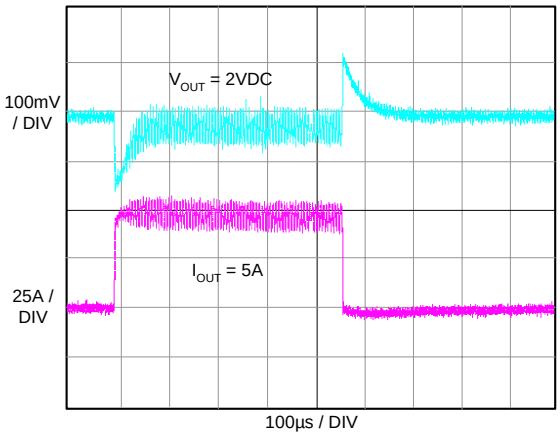
OUTPUT VOLTAGE VS. TEMPERATURE



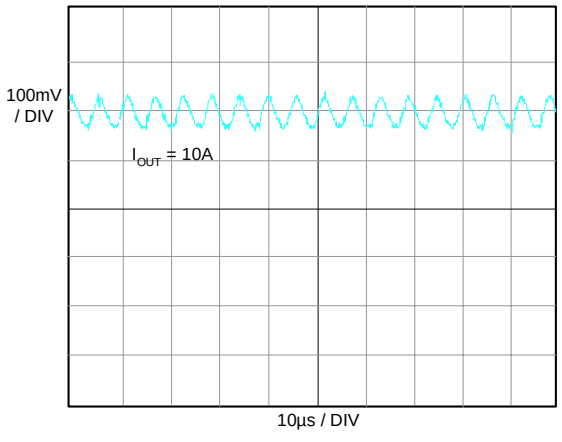
OUTPUT STARTUP



OUTPUT VOLTAGE VS. TEMPERATURE



OUTPUT VOLTAGE VS. TEMPERATURE



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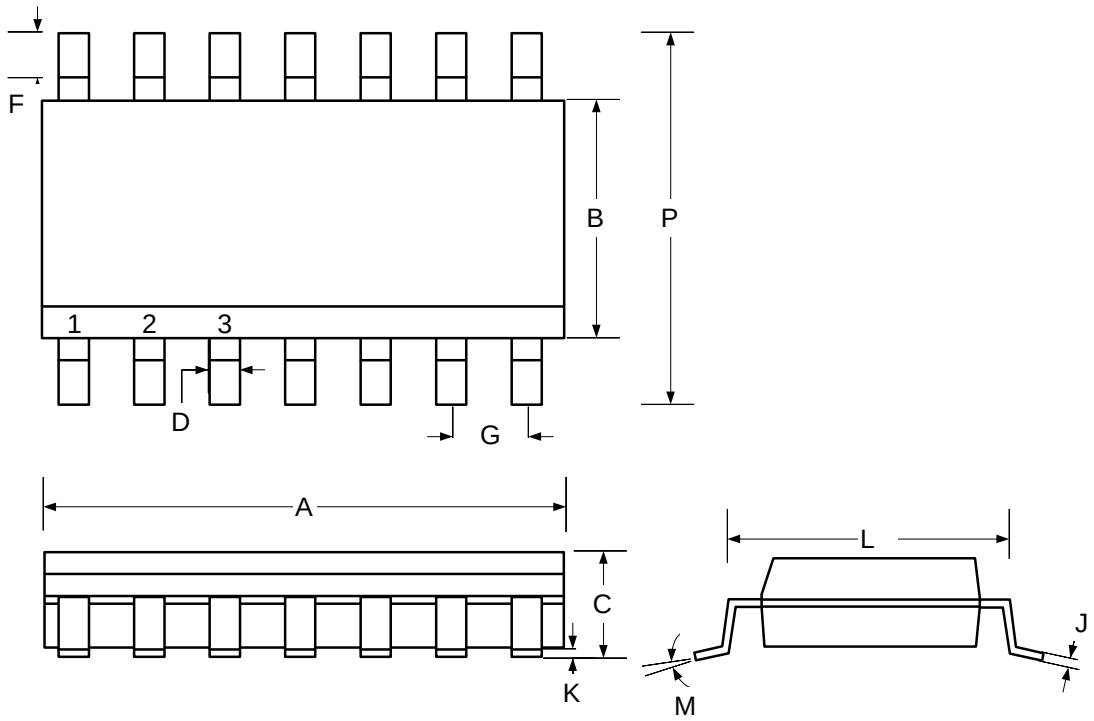
PACKAGE DIMENSIONS

D — 14-Pin Plastic SOIC



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.54	8.74	0.336	0.344
B	3.81	3.94	0.150	0.155
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
F		0.77		0.030
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.007	0.010
K	0.10	0.25	0.004	0.010
L	4.82	5.21	0.189	0.205
M	0	8	0	8
P	5.79	6.20	0.228	0.244
*LC		0.10		0.004

*Lead Coplanarity

Note:
1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.

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NOTES