Microsemi

LX5506

InGaP HBT 4.5 – 6GHz Power Amplifier

PRODUCTION DATA SHEET

DESCRIPTION

The LX5506 is a power amplifier designed for the FCC Unlicensed National Information Infrastructure (U-NII) band, HyperLAN2 and Japan WLAN applications in the 4.9-5.95 GHz frequency range. The PA is implemented as a three-stage monolithic microwave integrated circuit (MMIC) with active bias and complete on-chip input matching. The device is manufactured with an InGaP/GaAs Heterojunction Bipolar Transistor (HBT) IC process (MOCVD). It operates at a single positive voltage supply of 3.3V (nominal), with +26dBm of P1dB and up to 23dB power gain in the 5.15 - 5.85GHz frequency range with a simple output matching capacitor pair.

For OFDM operation (64QAM, 54Mbps), the PA provides +18dBm linear output power with a very low EVM (Error-Vector Magnitude) of 3%, and consumes about 190mA total DC current. At higher supply voltage of 5V, the same device provides +24dBm linear OFDM output power with 5% EVM.

The LX5506 is available in a 16-pin 3mmx3mm micro-lead package (MLP). The compact footprint, low profile, and excellent thermal capability of the MLP package makes the LX5506 an ideal solution for broadband, high-gain power amplifier requirements for IEEE 802.11a, and HiperLAN2 portable WLAN applications.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: http://www.microsemi.com

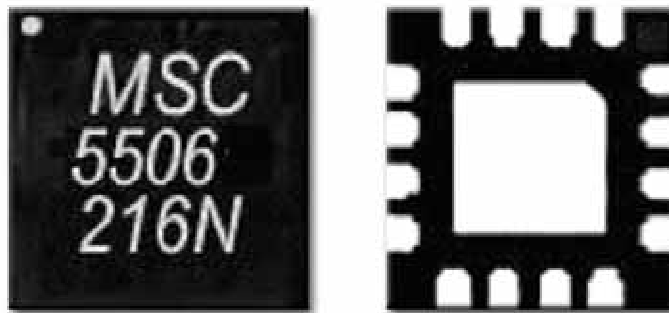
KEY FEATURES

- Advanced InGaP HBT
- Single-Polarity 3.3V Supply
- EVM ~ 3% at Pout=18dBm for 64QAM/ 54Mbps OFDM
- P1dB ~ +26dBm
- Power Gain ~ 23dB at 5.25GHz for Icq ~100mA
- Power Gain ~ 21dB at 5.85GHz for Icq ~100mA
- Total Current ~190mA at Pout=18dBm at 5.25GHz
- ACPR ~ -50dBc at 30MHz Offset at Pout=18dBm
- Complete On-Chip Input Match
- Simple Output Capacitor Match
- Small Footprint: 3x3mm2
- Low Profile: 0.9mm

APPLICATIONS

- FCC U-NII Wireless
- IEEE 802.11a
- HiperLAN2
- 5GHz Cordless Phone

PRODUCT HIGHLIGHT



PACKAGE ORDER INFO

LQ	Plastic MLPQ 16-Pin
	LX5506LQ
	RoHS Compliant / Pb-free Transition DC: 0418

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX5506LQ-TR)

This device is classified as ESD Level 0 in accordance with JESD22-A114-B, (HBM) testing. Appropriate ESD procedures should be observed when handling this device.

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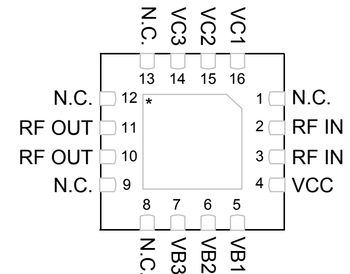
ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage, RF off 6V
Collector Current 600mA
Total Power Dissipation 3W
RF Input Power .... +15dBm
Maximum Junction Temperature (T_J max) .... 150°C
Operation Ambient Temperature .... -40 to +85°C
Storage Temperature .... -65 to +150°C
Peak Package Solder Reflow Temperature (40 second max. exposure) .... 260°C (+0, -5)

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

PACKAGE PIN OUT



LQ PACKAGE
(Bottom View)

RoHS / Pb-free 100% Matte Tin Lead Finish

FUNCTIONAL PIN DESCRIPTION

Name	Description
RF IN	RF input for the power amplifier. This pin is DC-shorted to GND but AC-coupled to the transistor base of the first stage.
VCC	Supply voltage for the bias reference and control circuits.
VB1	Bias current control voltage for the first stage.
VB2	Bias current control voltage for the second stage.
VB3	Bias current control voltage for the third stage.
RF OUT	RF output for the power amplifier. This pin is AC-coupled and does not require a DC-blocking capacitor.
VC1	Power supply for the first stage amplifier.
VC2	Power supply for the second stage amplifier.
VC3	Power supply for the third stage amplifier.
GND	The center metal base of the MLP package provides both DC and RF ground as well as heat sink for the power amplifier.
N.C.	These are unused pins and not connected to the device. They can be treated either as open pins or connected to ground for better heat dissipation.

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ELECTRICAL CHARACTERISTICS

Test conditions: Vcc = 3.3V, Vref = 2.9V, Icq = 100mA, T_A = 25°C, unless otherwise specified.

Parameter	Condition	Symbol	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
Frequency Range		f	5.15		5.35	5.7		5.85	GHz
Output Power at 1dB Compression		Pout	25	26		25	26		dBm
Power Gain at Pout=18dBm		Gp	21	23		19	21		dB
EVM at Pout=18dBm	64QAM/54Mbps			3			3		%
Total Current at Pout=18dBm		Ictotal		190			200		mA
Quiescent Current		Icq		100			100		mA
Bias Control Reference Current	For Icq=100mA	Iref		2.2			2.2		mA
Small-Signal Gain		S21		22			20		dB
Gain Flatness	Over 200MHz	ΔS21		+/-0.5			+/-0.5		dB
Gain Variation Over Temperature	-40 to +85°C	ΔS21		3 [a)], 1 [b)]			2 [a)], 1 [b)]		dB
Input Return Loss		S11		-15	-10		-15	-10	dB
Output Return Loss		S22		-7			-15		dB
Reverse Isolation		S12		-40			-40		dB
Second Harmonic	Pout = 18dBm			-40			-60		dBc
Third Harmonic	Pout = 18dBm			-40			-40		dBc
Ramp-On Time	10 - 90%	t_{ON}		100			100		ns

Note a) Vref = 2.9V b)Vref = 3.0V

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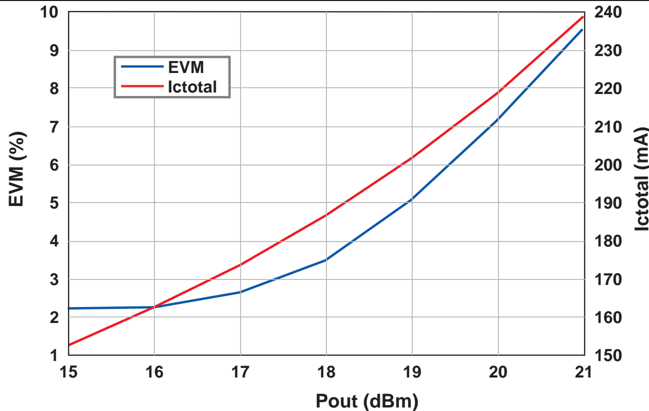
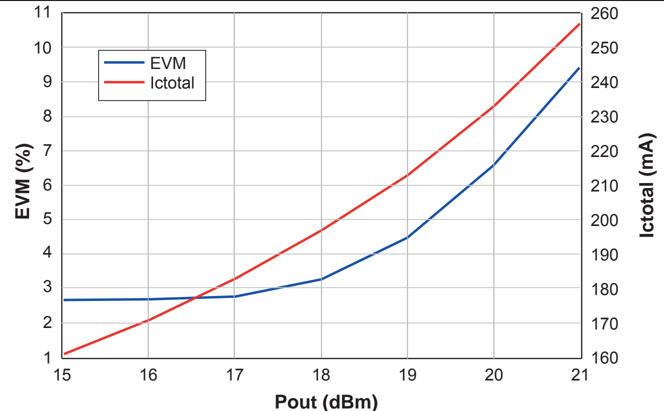
EVM VS POUT FREQ=5.15GHZ



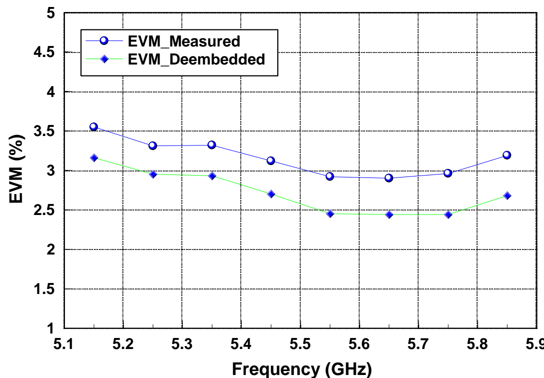
Typical EVM and Total Current vs. Pout at Vc = 3.3V
(Vc = 3.3V, Icq = 100mA, 64QAM / 54Mbps)

EVM VS POUT FREQ=5.85GHZ



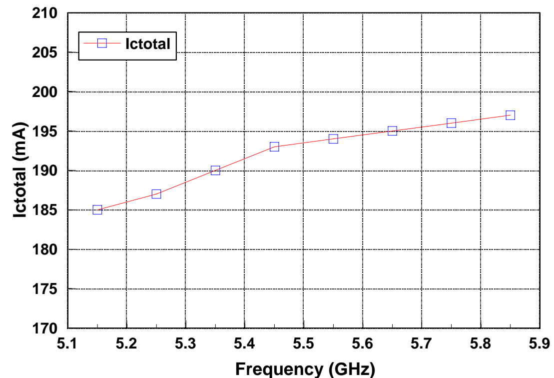
Typical EVM and Total Current vs. Pout at Vc = 3.3V
(Vc = 3.3V, Icq = 100mA, 64QAM / 54Mbps)

EVM VS FREQUENCY



Typical EVM vs. Frequency
(Vc =3.3V, Icq = 100mA, Pout = 18dBm, 64QAM / 54Mpbs)

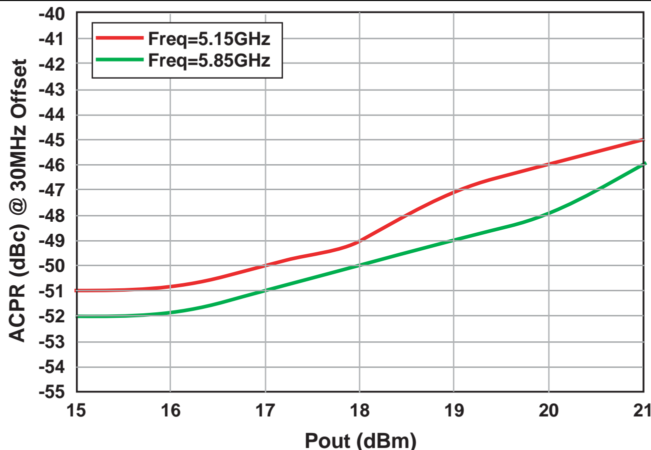
CURRENT VS FREQUENCY



Typical Total Current vs. Frequency
(Vc=3.3V, Icq=100mA, Pout=18dBm, 64QAM/54Mbps)

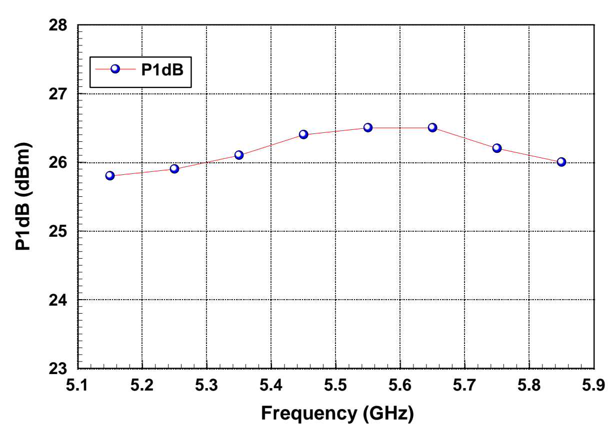
Notes: All EVM data are for OFDM signal of 64QAM/54Mbps and are actual measured data without any de-embedding. Source EVM is around 1.4 - 1.8% for the input power levels for test.

ACPR VS OUTPUT POWER



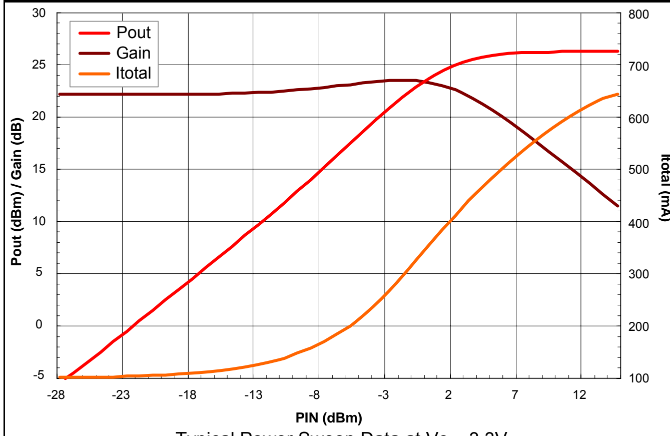
Typical ACPR vs. Output Power
(Vc = 3.3V, Icq = 100mA, 64QAM / 54Mpbs)

P1DB VS FREQUENCY



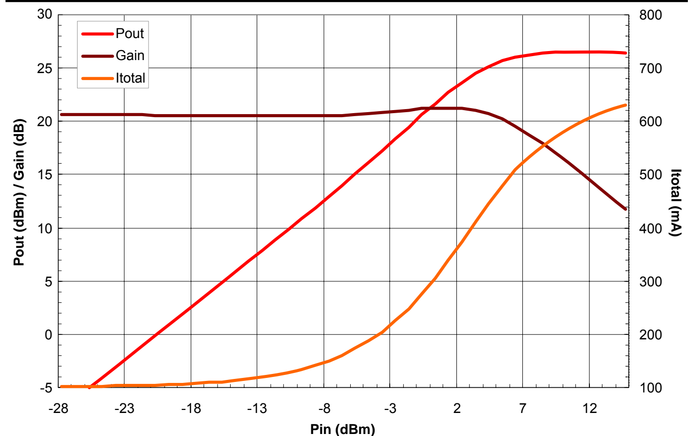
Typical P1dB vs. Frequency
(Icq = 100mA for Vc = 3.3V, Icq = 110mA for Vc=4.5V)

POWER SWEEP DATA 5.15GHZ



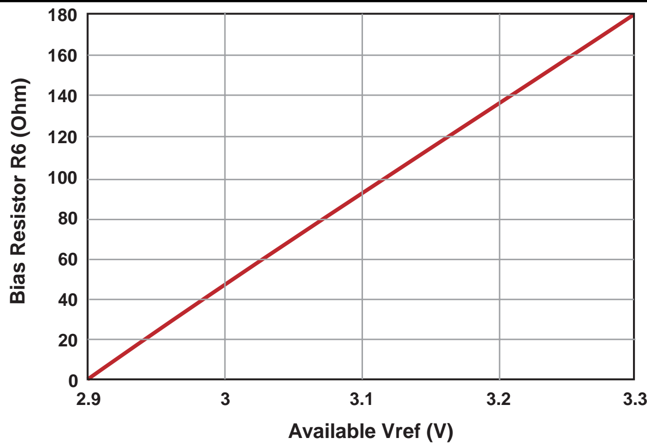
Typical Power Sweep Data at Vc = 3.3V
(VC = 3.3V, Icq = 100mA, No Heat Sink) Frequency = 5.15GHz

POWER SWEEP DATA 5.85GHZ



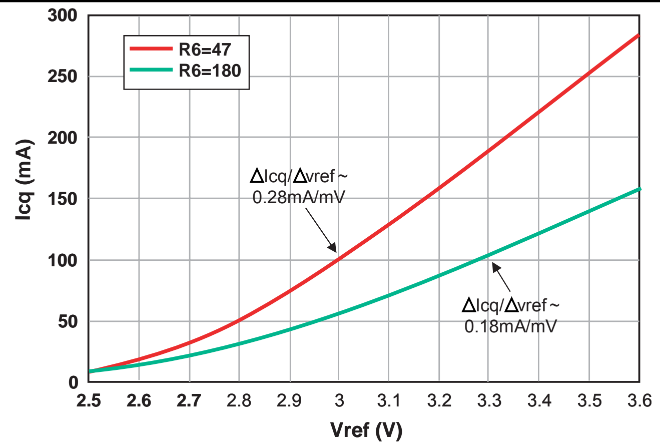
Typical Power Sweep Data at Vc = 3.3V
(VC = 3.3V, Icq = 100mA, No Heat Sink) Frequency = 5.85GHz

RECOMMENDED BIAS RESISTOR



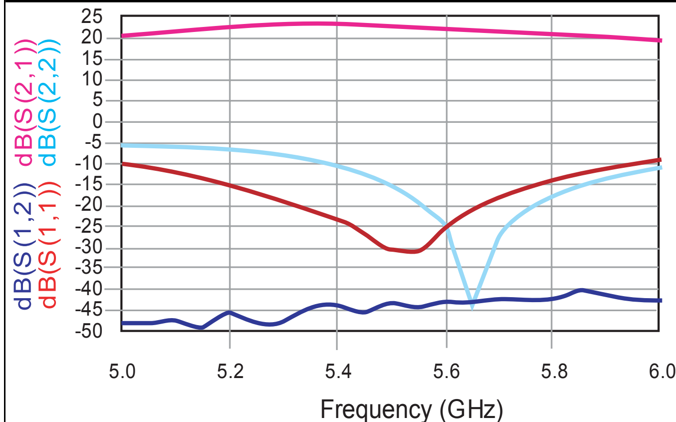
Recommended Bias Resistor for Available Vref
(Adjusted R6 value for Obtaining Nominal Icq = 10mA at Vc = 3.3V)

QUIESCENT CURRENT VS VREF



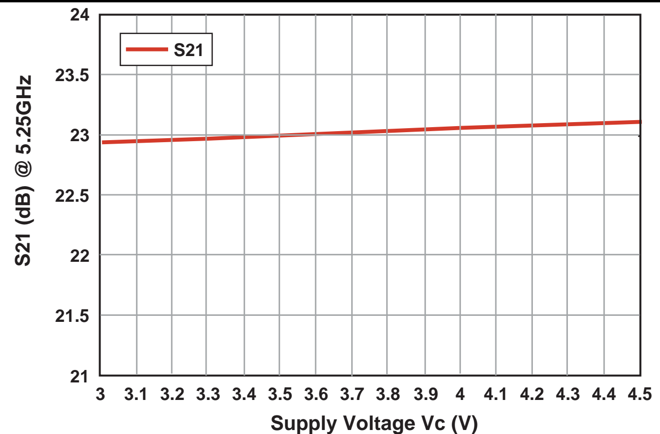
Quiescent Current vs. Vref
(Vc = 3.3V, Bias Resistor R6 = 47Ω & 180Ω)

S-PARAMETER DATA



Typical S-Parameter Data at Room Temperature
(Vc = 3.3V, R6 = 0Ω, Vref = 2.9V. Icq = 100mA)

SMALL SIGNAL VS SUPPLY VOLTAGE



Typical Small Signal Gain vs. Supply Voltage
(R6 = 0Ω, Vref = 2.9V, Icq = 100mA for Vc = 3.3V, Freq = 5.25GHz)

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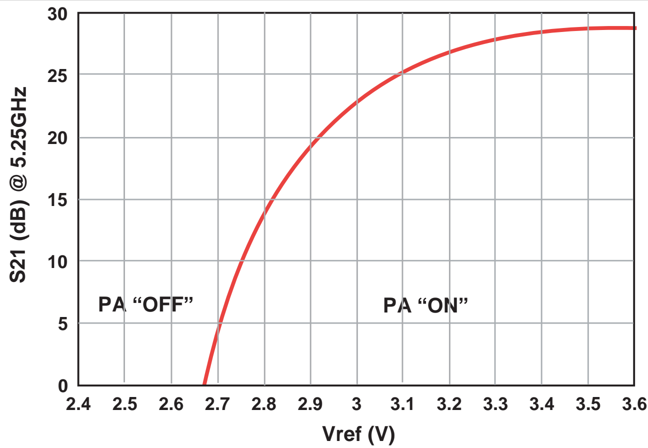
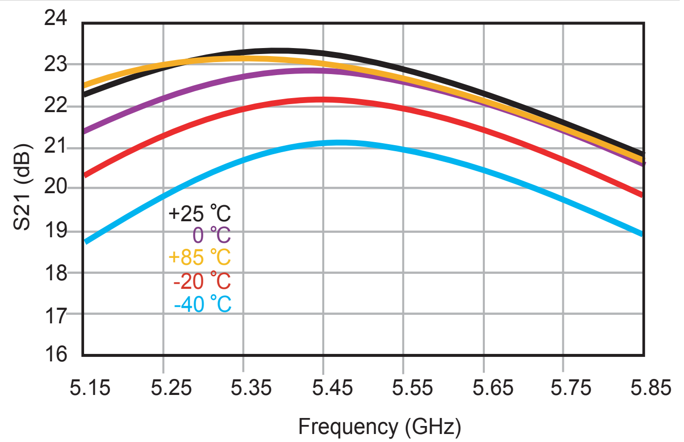
SMALL SIGNAL VS BIAS REF.



Typical Small Signal Gain vs. Bias Reference Voltage
(Vc = 3.3V, R6 = 47Ω, Vref = 3.0V, Icq = 100mA, Freq = 5.25GHz)

SMALL SIGNAL GAIN OVER TEMP



Typical Small Signal Gain Variation Over Temperature
(Vc = 3.3V, R6 = 0Ω, Vref = 2.9V, Icq = 100mA at Room Temperature)

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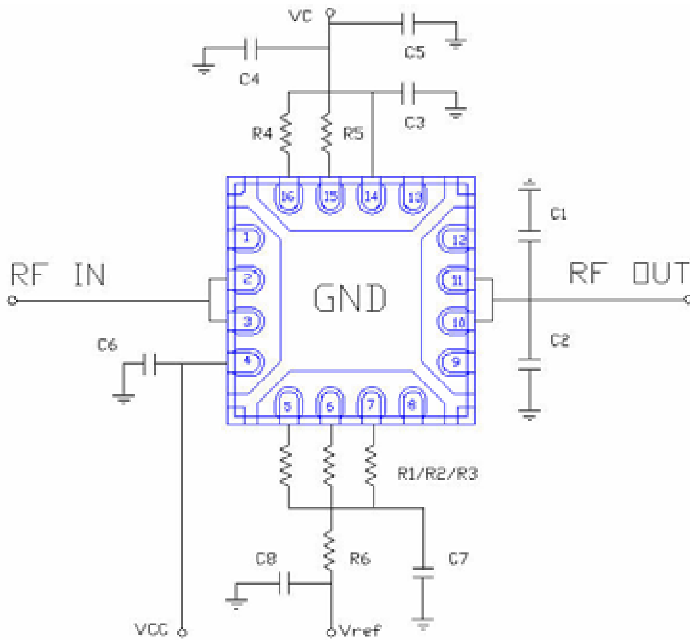
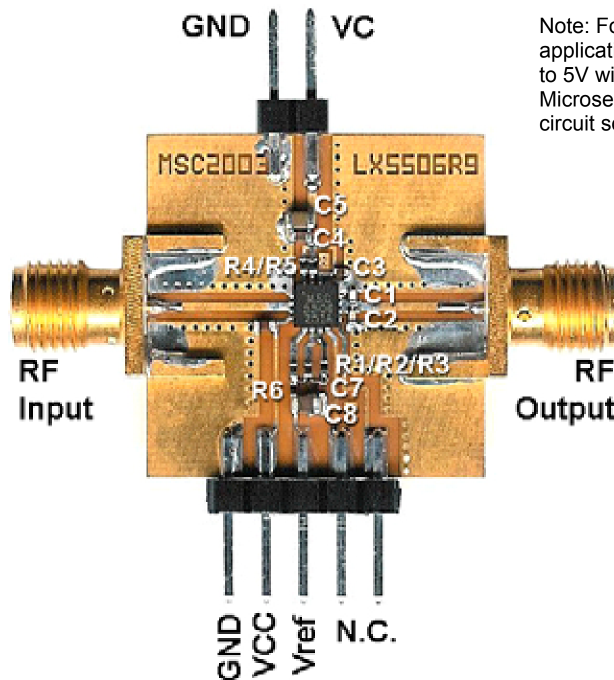
APPLICATION NOTE



Recommended BOM

Location	Value
C1/C2	0.5/0.5pF (0402)
C3	220pF (0402)
C4=C6	1µF (0603)
C5=C8	10µF (0805)
C7	1nF (0402)
R1/R2/R3	100/604/909Ω (0402)
R4/R5	10/10Ω (0402)
R6	0 Ω (For Vref=2.9V, Adjustable for Different Vref)
Substrate	10mil GETEK $\varepsilon_r = 3.9, \tan\delta = 0.02$

Notes:
1) C1/C2 position should be ~30mil from MLP package edge connected with 50 Ohm microstrip.
2) All other component positions are not critical.
3) R6 should be adjusted to maintain nominal Icq for different available Vref values (see R6-Vref plot).
4) For Vref<2.9V operation please contact technical support for BOM modification.
5) C6 can be eliminated when VC/VCC pins are tied together in multiplayer board layout.
6) C7 ensures ~100ns switching time for PA on/off.
7) For PA switching speed test C8 should be moved to input side of the switch.



Note: For higher output power applications VC can be increased up to 5V with +/-10% tolerance. Contact Microsemi for details on application circuit schematic and BOM.

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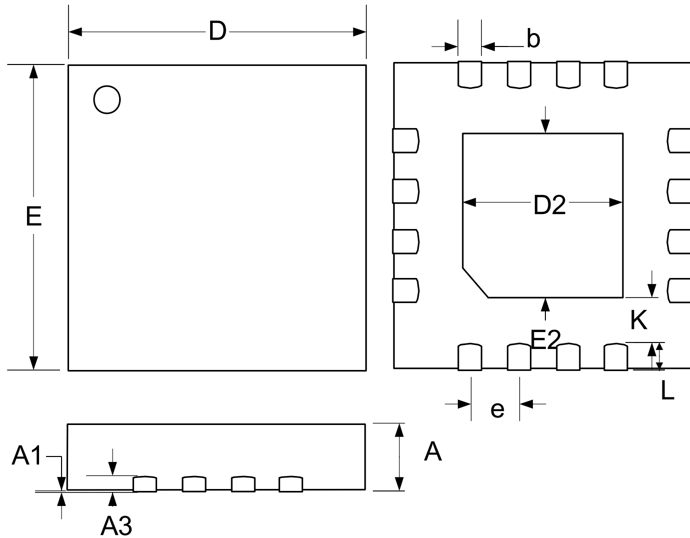
PACKAGE DIMENSIONS

LQ **16-Pin MLPQ 3x3 (75 x 75 mil DAP)**



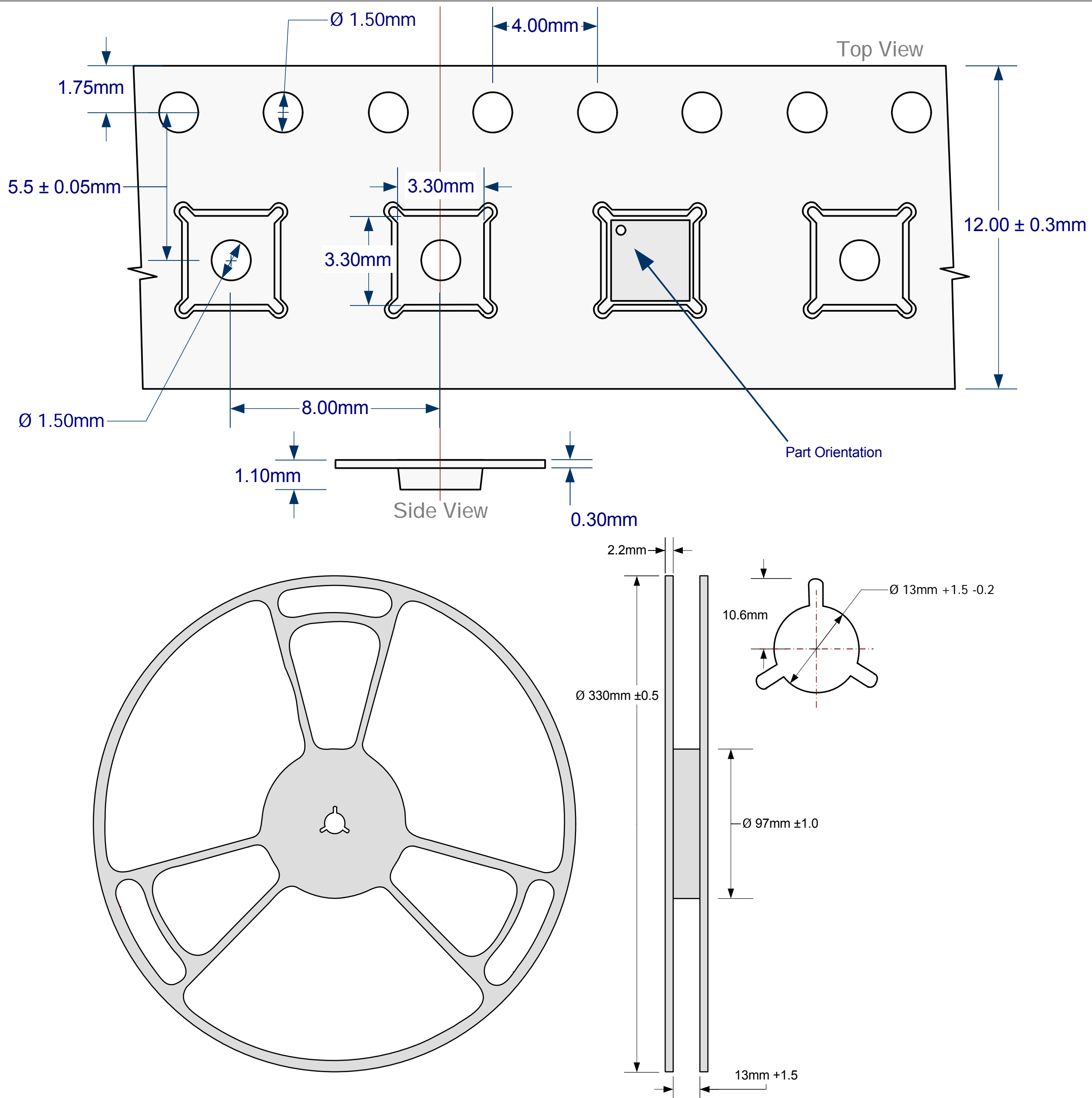
Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0	0.05	0	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	3.00 BSC		0.118 BSC	
E	3.00 BSC		0.118 BSC	
e	0.50 BSC		0.020 BSC	
D2	1.55	1.80	0.061	0.071
E2	1.55	1.80	0.061	0.071
K	0.2	-	0.008	-
L	0.35	0.50	0.012	0.020

Note:

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006”) on any side. Lead dimension shall not include solder coverage.

TAPE AND REEL

Tape And Reel Specification



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