

# DDR SDRAM Unbuffered Module (DDR400 Module)

184pin Unbuffered Module based on 256Mb D-die  
64/72-bit Non ECC/ECC

Revision 1.2

May. 2003

## Revision History

### Revision 0.0 (June. 2002)

1. First release

### Revision 0.1 (Aug. 2002)

- Changed IDD3P value from 40mA to 55mA
- Changed IDD3N value from 60mA to 75mA

### Revision 1.0 (February, 2003)

- Modified AC Timing Parameters and Idd value.

### Revision 1.1 (February, 2003)

- Modified tAC value +/-0.7ns => +/-0.65ns

### Revision 1.2 (May, 2003)

- Corrected typo

**184Pin Unbuffered DIMM based on 256Mb D-die (x8, x16)****Ordering Information**

Part Number	Density	Organization	Component Composition	Height
M368L1624DTM-C(L)CC/C4	128MB	16M x 64	16Mx16( K4H561638D) * 4EA	1,250(mil)
M368L3223DTM-C(L)CC/C4	256MB	32M x 64	32Mx8( K4H560838D) * 8EA	1,250(mil)
M368L6423DTM-C(L)CC/C4	512MB	64M x 64	32Mx8( K4H560838D) * 16EA	1,250(mil)
M381L3223DTM-C(L)CC/C4	256MB	32M x 72	32Mx8( K4H560838D) * 9EA	1,250(mil)
M381L6423DTM-C(L)CC/C4	512MB	64M x 72	32Mx8( K4H560838D) * 18EA	1,250(mil)

**Operating Frequencies**

	CC(DDR400@CL=3)	C4(DDR400@CL=3)
Speed @CL3	200MHz	200MHz
CL-tRCD-tRP	3-3-3	3-4-4

**Feature**

- Power supply : Vdd: 2.6V ± 0.1V, Vddq: 2.6V ± 0.1V
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe(DQS)
- Differential clock inputs(CK and  $\overline{CK}$ )
- DLL aligns DQ and DQS transition with CK transition
- Programmable Read latency 3 (clock) for DDR400 , 2.5 (clock) for DDR333
- Programmable Burst length (2, 4, 8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto & Self refresh, 7.8us refresh interval(8K/64ms refresh)
- Serial presence detect with EEPROM
- PCB : Height 1,250 (mil), single (128MB, 256MB) and double(512MB) sided
- SSTL\_2 Interface

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# 128MB, 256MB, 512MB Unbuffered DIMM

# DDR SDRAM

## Pin Configuration (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VREF	32	A5	62	VDDQ	93	VSS	124	VSS	154	/RAS
2	DQ0	33	DQ24	63	/WE	94	DQ4	125	A6	155	DQ45
3	VSS	34	VSS	64	DQ41	95	DQ5	126	DQ28	156	VDDQ
4	DQ1	35	DQ25	65	/CAS	96	VDDQ	127	DQ29	157	/CS0
5	DQS0	36	DQS3	66	VSS	97	DM0	128	VDDQ	158	/CS1
6	DQ2	37	A4	67	DQS5	98	DQ6	129	DM3	159	DM5
7	VDD	38	VDD	68	DQ42	99	DQ7	130	A3	160	VSS
8	DQ3	39	DQ26	69	DQ43	100	VSS	131	DQ30	161	DQ46
9	NC	40	DQ27	70	VDD	101	NC	132	VSS	162	DQ47
10	NC	41	A2	71	*/CS2	102	NC	133	DQ31	163	*/CS3
11	VSS	42	VSS	72	DQ48	103	*A13	134	CB4	164	VDDQ
12	DQ8	43	A1	73	DQ49	104	VDDQ	135	CB5	165	DQ52
13	DQ9	44	CB0	74	VSS	105	DQ12	136	VDDQ	166	DQ53
14	DQS1	45	CB1	75	/CK2	106	DQ13	137	CK0	167	NC
15	VDDQ	46	VDD	76	CK2	107	DM1	138	/CK0	168	VDD
16	CK1	47	DQS8	77	VDDQ	108	VDD	139	VSS	169	DM6
17	/CK1	48	A0	78	DQS6	109	DQ14	140	DM8	170	DQ54
18	VSS	49	CB2	79	DQ50	110	DQ15	141	A10	171	DQ55
19	DQ10	50	VSS	80	DQ51	111	CKE1	142	CB6	172	VDDQ
20	DQ11	51	CB3	81	VSS	112	VDDQ	143	VDDQ	173	NC
21	CKE0	52	BA1	82	VDDID	113	*BA2	144	CB7	174	DQ60
22	VDDQ	KEY		83	DQ56	114	DQ20	KEY		175	DQ61
23	DQ16	53	DQ32	84	DQ57	115	A12	145	VSS	176	VSS
24	DQ17	54	VDDQ	85	VDD	116	VSS	146	DQ36	177	DM7
25	DQS2	55	DQ33	86	DQS7	117	DQ21	147	DQ37	178	DQ62
26	VSS	56	DQS4	87	DQ58	118	A11	148	VDD	179	DQ63
27	A9	57	DQ34	88	DQ59	119	DM2	149	DM4	180	VDDQ
28	DQ18	58	VSS	89	VSS	120	VDD	150	DQ38	181	SA0
29	A7	59	BA0	90	NC	121	DQ22	151	DQ39	182	SA1
30	VDDQ	60	DQ35	91	SDA	122	A8	152	VSS	183	SA2
31	DQ19	61	DQ40	92	SCL	123	DQ23	153	DQ44	184	VDDSPD

### Note :

- \* : These pins are not used in this module.
- Pins 44, 45, 47, 49, 51, 134, 135, 140, 142, 144 are used on x72 module, and are not used on x64 module.
- Pins 111, 158 are NC for 1 Row Module[M368L1624DTM, M368(81)L3223DTM] & used for 2 Row Module[M368(81)L6423DTM]

## Pin Description

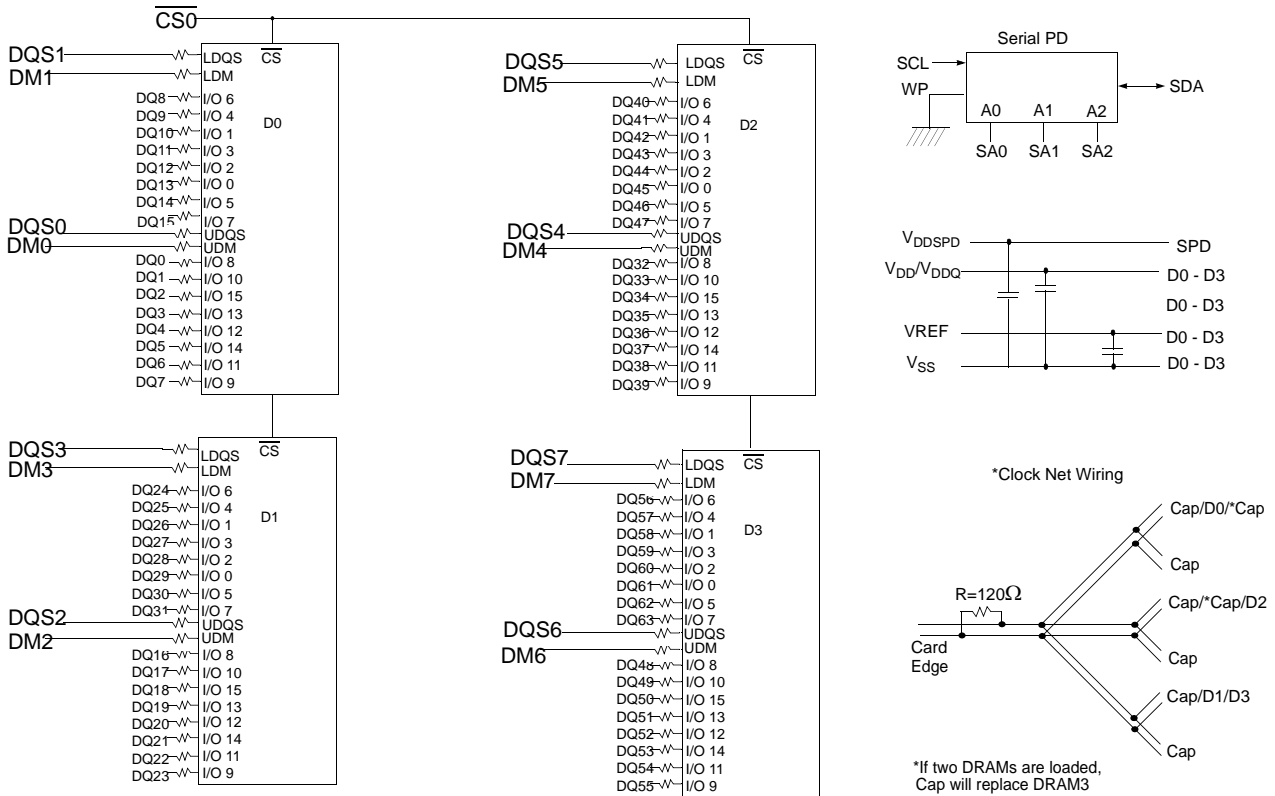
Pin Name	Function	Pin Name	Function
A0 ~ A12	Address input (Multiplexed)	DM0 ~ 7	Data - in mask
BA0 ~ BA1	Bank Select Address	VDD	Power supply (2.6V)
DQ0 ~ DQ63	Data input/output	VDDQ	Power Supply for DQS(2.6V)
DQS0 ~ DQS7	Data Strobe input/output	VSS	Ground
CK0,CK0 ~ CK2, CK2,CK2	Clock input	VREF	Power supply for reference
CKE0, CKE1(for double banks)	Clock enable input	VDDSPD	Serial EEPROM Power/Supply ( 2.3V to 3.6V )
/CS0, /CS1(for double banks)	Chip select input	SDA	Serial data I/O
RAS	Row address strobe	SCL	Serial clock
CAS	Column address strobe	SA0 ~ 2	Address in EEPROM
WE	Write enable	NC	No connection
CB0 ~ CB7(only for x72)	Check bit(Data-in/data-out)		

# 128MB, 256MB, 512MB Unbuffered DIMM

# DDR SDRAM

128MB, 16M x 64 Non ECC Module (M368L1624DTM) (Populated as 1 bank of x16 DDR SDRAM Module)

## Functional Block Diagram



BA0 - BA1 → BA0-BA1 : DDR SDRAMs D0 - D3  
 A0 - A12 → A0-A12 : DDR SDRAMs D0 - D3  
 $\overline{\text{RAS}}$  →  $\overline{\text{RAS}}$  : DDR SDRAMs D0 - D3  
 $\overline{\text{CAS}}$  →  $\overline{\text{CAS}}$  : DDR SDRAMs D0 - D3  
 CKE0 → CKE : DDR SDRAMs D0 - D3  
 $\overline{\text{WE}}$  →  $\overline{\text{WE}}$  : DDR SDRAMs D0 - D3

Clock Wiring	
Clock Input	SDRAMs
CK0/ $\overline{\text{CK0}}$	NC
CK1/ $\overline{\text{CK1}}$	2 SDRAMs
CK2/ $\overline{\text{CK2}}$	2 SDRAMs

### Notes :

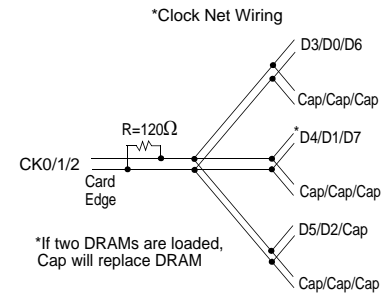
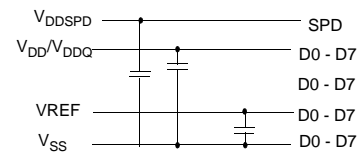
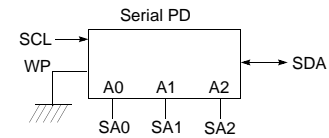
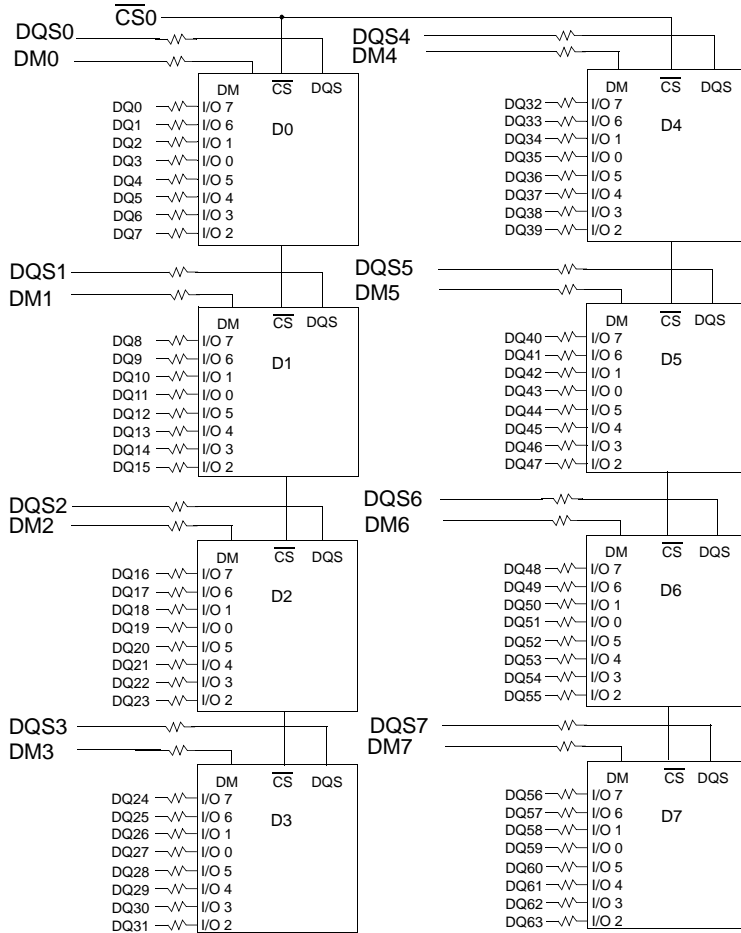
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/CS relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms  $\pm$  5%.
4. BAx, Ax, RAS, CAS, WE resistors: 7.5 Ohms  $\pm$  5%

# 128MB, 256MB, 512MB Unbuffered DIMM

# DDR SDRAM

256MB, 32M x 64 Non ECC Module (M368L3223DTM) (Populated as 1 bank of x8 DDR SDRAM Module)

## Functional Block Diagram



- BA0 - BA1 → BA0-BA1 : DDR SDRAMs D0 - D7
- A0 - A12 → A0-A12 : DDR SDRAMs D0 - D7
- $\overline{\text{RAS}}$  →  $\overline{\text{RAS}}$  : DDR SDRAMs D0 - D7
- $\overline{\text{CAS}}$  →  $\overline{\text{CAS}}$  : DDR SDRAMs D0 - D7
- CKE0 → CKE : DDR SDRAMs D0 - D7
- $\overline{\text{WE}}$  →  $\overline{\text{WE}}$  : DDR SDRAMs D0 - D7

Clock Wiring	
Clock Input	SDRAMs
CK0/ $\overline{\text{CK0}}$	2 SDRAMs
CK1/ $\overline{\text{CK1}}$	3 SDRAMs
CK2/ $\overline{\text{CK2}}$	3 SDRAMs

### Notes :

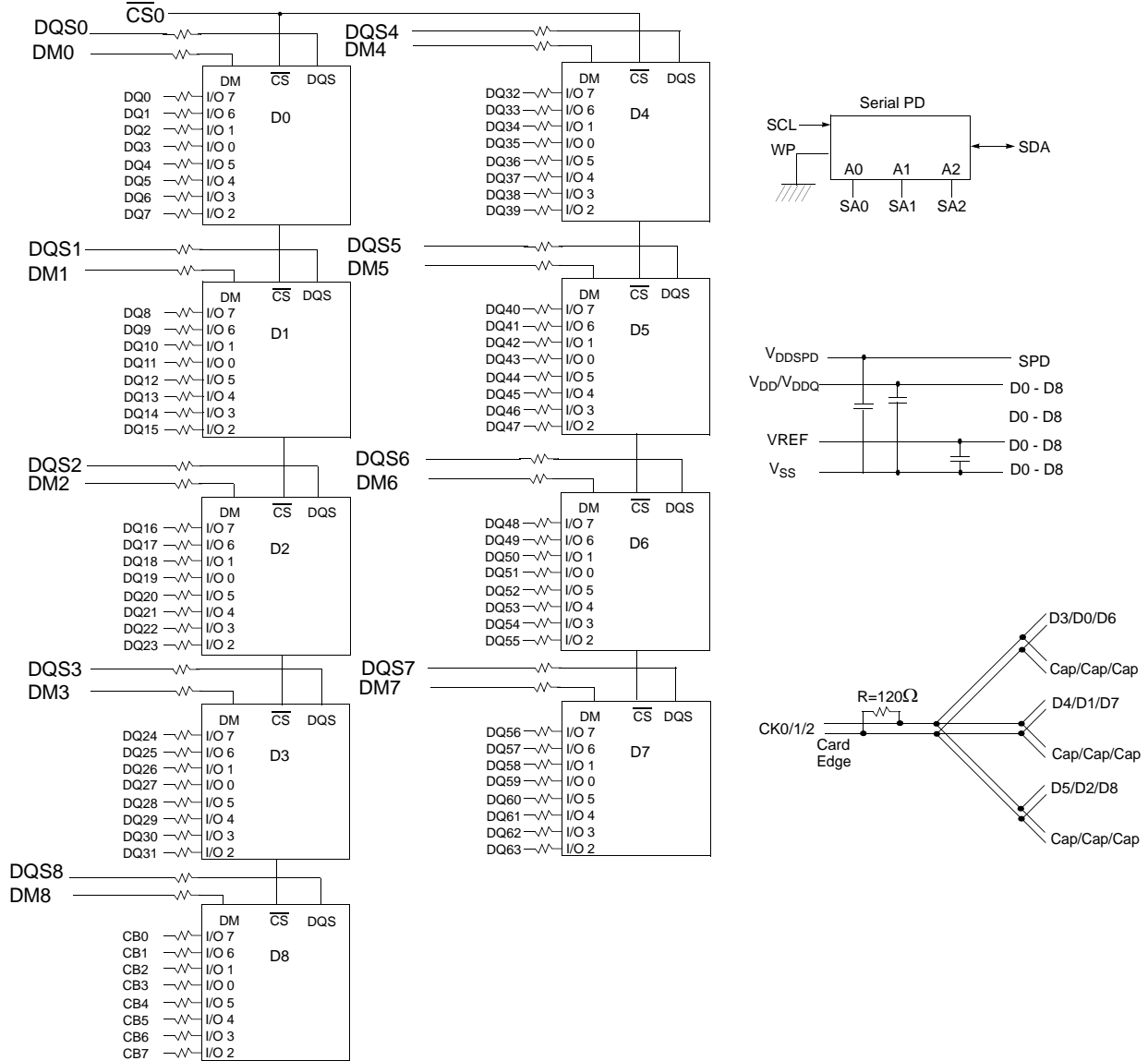
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/CS relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms  $\pm$  5%.
4. BAx, Ax,  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ , WE resistors: 5.1 Ohms  $\pm$  5%

# 128MB, 256MB, 512MB Unbuffered DIMM

# DDR SDRAM

256MB, 32M x 72 ECC Module (M381L3223DTM) (Populated as 1 bank of x8 DDR SDRAM Module)

## Functional Block Diagram



BA0 - BA1 → BA0-BA1 : DDR SDRAMs D0 - D8  
 A0 - A12 → A0-A12 : DDR SDRAMs D0 - D8  
 $\overline{\text{RAS}}$  →  $\overline{\text{RAS}}$  : DDR SDRAMs D0 - D8  
 $\overline{\text{CAS}}$  →  $\overline{\text{CAS}}$  : DDR SDRAMs D0 - D8  
 CKE0 → CKE : DDR SDRAMs D0 - D8  
 $\overline{\text{WE}}$  →  $\overline{\text{WE}}$  : DDR SDRAMs D0 - D8

Clock Wiring	
Clock Input	SDRAMs
CK0/ $\overline{\text{CK0}}$	3 SDRAMs
CK1/ $\overline{\text{CK1}}$	3 SDRAMs
CK2/ $\overline{\text{CK2}}$	3 SDRAMs

### Notes :

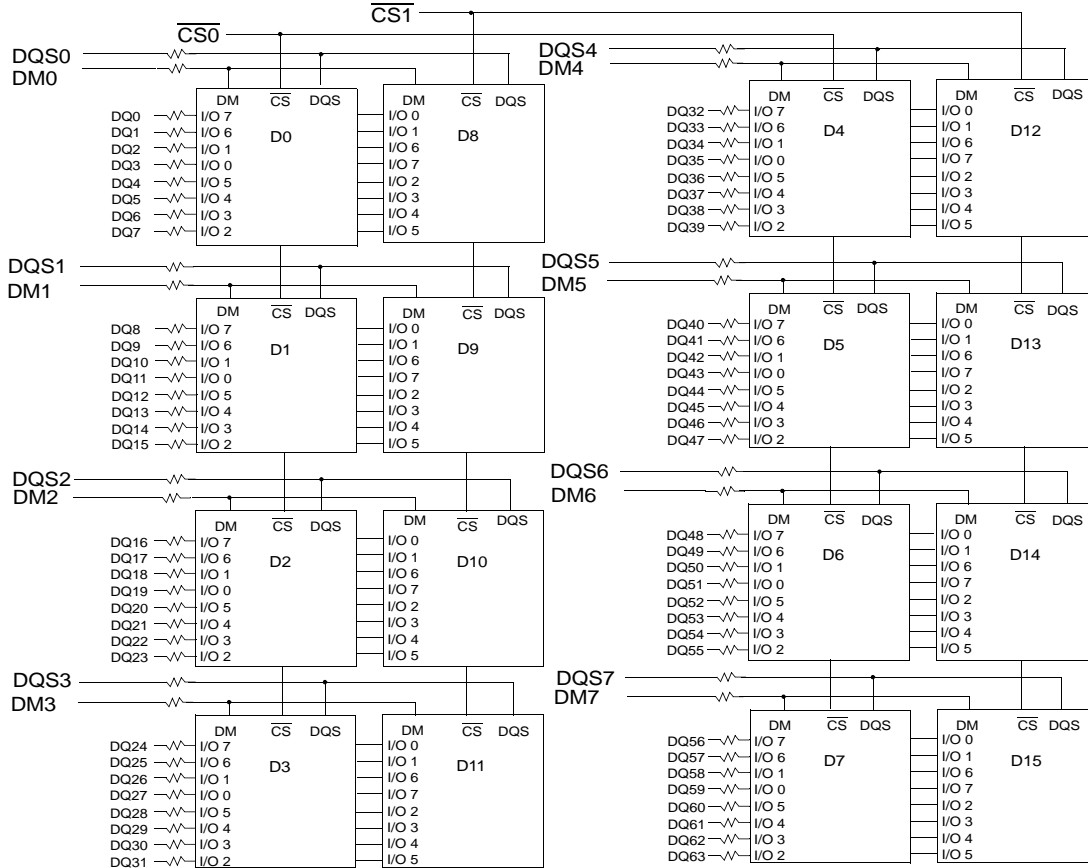
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/CS relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms  $\pm$  5%.
4. BAx, Ax, RAS, CAS, WE resistors: 5.1 Ohms  $\pm$  5%

# 128MB, 256MB, 512MB Unbuffered DIMM

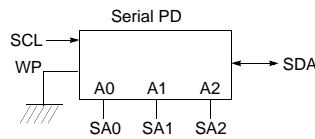
# DDR SDRAM

512MB, 64M x 64 Non ECC Module (M368L6423DTM) (Populated as 2 bank of x8 DDR SDRAM Module)

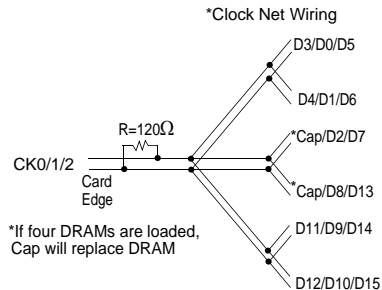
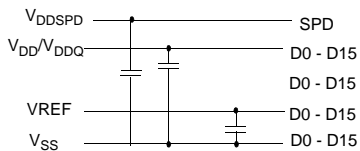
## Functional Block Diagram



- BA0 - BA1 → BA0-BA1 : DDR SDRAMs D0 - D15
- A0 - A12 → A0-A12 : DDR SDRAMs D0 - D15
- $\overline{\text{RAS}}$  →  $\overline{\text{RAS}}$  : DDR SDRAMs D0 - D15
- $\overline{\text{CAS}}$  →  $\overline{\text{CAS}}$  : DDR SDRAMs D0 - D15
- CKE1 → CKE : DDR SDRAMs D8 - D15
- CKE0 → CKE : DDR SDRAMs D0 - D7
- $\overline{\text{WE}}$  →  $\overline{\text{WE}}$  : DDR SDRAMs D0 - D15



Clock Wiring	
Clock Input	SDRAMs
CK0/CK0	4 SDRAMs
CK1/CK1	6 SDRAMs
CK2/CK2	6 SDRAMs



**Notes :**

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/CS relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms  $\pm$  5%.
4. BAX, Ax, RAS, CAS, WE resistors: 3.0 Ohms  $\pm$  5%

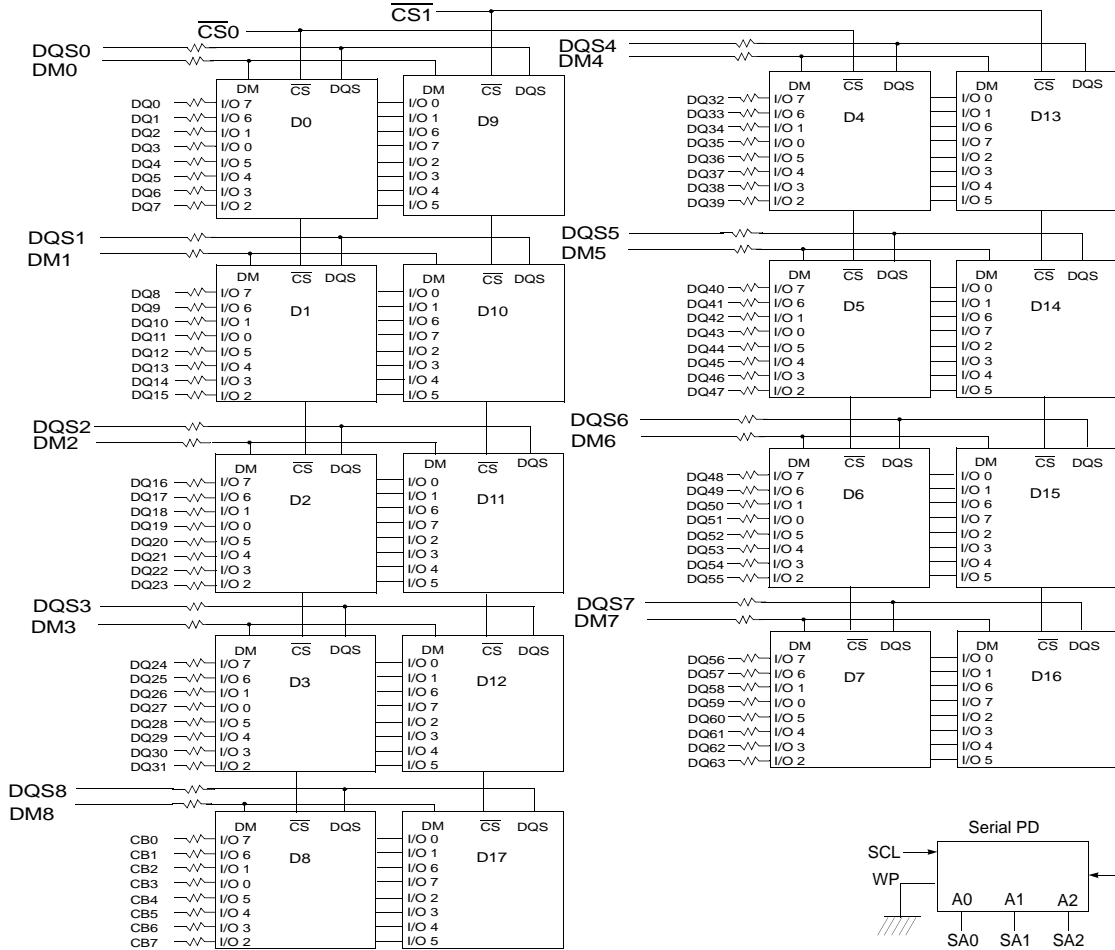


# 128MB, 256MB, 512MB Unbuffered DIMM

# DDR SDRAM

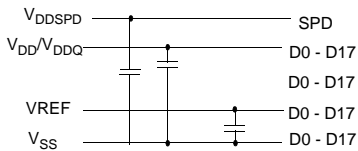
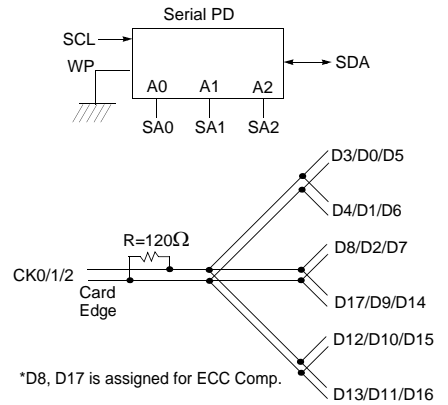
512MB, 64M x 72 ECC Module (M381L6423DTM) (Populated as 2 bank of x8 DDR SDRAM Module)

## Functional Block Diagram



- BA0 - BA1 → BA0-BA1 : DDR SDRAMs D0 - D17
- A0 - A12 → A0-A12 : DDR SDRAMs D0 - D17
- RAS → RAS : DDR SDRAMs D0 - D17
- CAS → CAS : DDR SDRAMs D0 - D17
- CKE1 → CKE : DDR SDRAMs D9 - D17
- CKE0 → CKE : DDR SDRAMs D0 - D8
- WE → WE : DDR SDRAMs D0 - D17

* Clock Wiring	
Clock Input	SDRAMs
CK0/CK0	6 SDRAMs
CK1/CK1	6 SDRAMs
CK2/CK2	6 SDRAMs



### Notes :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/CS relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms ± 5%.
4. BAx, Ax, RAS, CAS, WE resistors: 3.0 Ohms ± 5%.

## Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.5 ~ 3.6	V
Voltage on $V_{DD}$ & $V_{DDQ}$ supply relative to $V_{SS}$	$V_{DD}, V_{DDQ}$	-1.0 ~ 3.6	V
Storage temperature	$T_{STG}$	-55 ~ +150	°C
Power dissipation	$P_D$	1.5 * # of component	W
Short circuit current	$I_{OS}$	50	mA

**Note** : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

Functional operation should be restricted to recommend operation condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

## DC Operating Conditions

Recommended operating conditions(Voltage referenced to  $V_{SS}=0V$ ,  $T_A=0$  to  $70^\circ C$ )

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal $V_{DD}$ of 2.5V)	$V_{DD}$	2.5	2.7		5
I/O Supply voltage	$V_{DDQ}$	2.5	2.7	V	5
I/O Reference voltage	$V_{REF}$	$0.49 \cdot V_{DDQ}$	$0.51 \cdot V_{DDQ}$	V	1
I/O Termination voltage(system)	$V_{TT}$	$V_{REF}-0.04$	$V_{REF}+0.04$	V	2
Input logic high voltage	$V_{IH}(DC)$	$V_{REF}+0.15$	$V_{DDQ}+0.3$	V	
Input logic low voltage	$V_{IL}(DC)$	-0.3	$V_{REF}-0.15$	V	
Input Voltage Level, CK and $\overline{CK}$ inputs	$V_{IN}(DC)$	-0.3	$V_{DDQ}+0.3$	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	$V_{ID}(DC)$	0.36	$V_{DDQ}+0.6$	V	3
V-I Matching: Pullup to Pulldown Current Ratio	$V_I(Ratio)$	0.71	1.4	-	4
Input leakage current	$I_I$	-2	2	uA	
Output leakage current	$I_{OZ}$	-5	5	uA	
Output High Current(Normal strength driver) ; $V_{OUT} = V_{TT} + 0.84V$	$I_{OH}$	-16.8		mA	
Output High Current(Normal strength driver) ; $V_{OUT} = V_{TT} - 0.84V$	$I_{OL}$	16.8		mA	
Output High Current(Half strength driver) ; $V_{OUT} = V_{TT} + 0.45V$	$I_{OH}$	-9		mA	
Output High Current(Half strength driver) ; $V_{OUT} = V_{TT} - 0.45V$	$I_{OL}$	9		mA	

**Note** : 1.  $V_{REF}$  is expected to be equal to  $0.5 \cdot V_{DDQ}$  of the transmitting device, and to track variations in the dc level of same.

Peak-to-peak noise on  $V_{REF}$  may not exceed +/-2% of the dc value.

- $V_{TT}$  is not applied directly to the device.  $V_{TT}$  is a system supply for signal termination resistors, is expected to be set equal to  $V_{REF}$ , and must track variations in the DC level of  $V_{REF}$
- $V_{ID}$  is the magnitude of the difference between the input level on CK and the input level on  $\overline{CK}$ .
- The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages from 0.25V to 1.0V. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation. The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1/7 for device drain to source voltages from 0.1 to 1.0.
- This is the DC voltage supplied at the DRAM and is inclusive of all noise up to 20MHz. Any noise above 20MHz at the DRAM generated from any source other than the DRAM itself may not exceed the DC voltage range of 2.6V +/-100mV.

DDR SDRAM IDD spec table

(V<sub>DD</sub>=2.7V, T = 10×C)

Symbol	M368L1624DTM(Non ECC)		M368L3223DTM (Non ECC)		Unit	Notes	
	CC(DDR400@CL=3)	C4(DDR400@CL=3)	CC(DDR400@CL=3)	C4(DDR400@CL=3)			
IDD0	440	420	840	800	mA		
IDD1	600	580	1040	1040	mA		
IDD2P	16	16	32	32	mA		
IDD2F	120	120	240	240	mA		
IDD2Q	100	100	200	200	mA		
IDD3P	220	220	440	440	mA		
IDD3N	300	300	600	600	mA		
IDD4R	880	880	1480	1480	mA		
IDD4W	1000	1000	1760	1760	mA		
IDD5	800	800	1600	1600	mA		
IDD6	Normal	12	12	24	24	mA	
	Low power	6	6	12	12	mA	Optional
IDD7A	520	1520	2800	2800	mA		

\* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

(V<sub>DD</sub>=2.7V, T = 10×C)

Symbol	M381L3223DTM(ECC)		M368L6423DTM(ECC)		Unit	Notes	
	CC(DDR400@CL=3)	C4(DDR400@CL=3)	CC(DDR400@CL=3)	C4(DDR400@CL=3)			
IDD0	950	900	1440	1400	mA		
IDD1	1170	1170	1640	1640	mA		
IDD2P	40	40	65	65	mA		
IDD2F	270	270	480	480	mA		
IDD2Q	230	230	400	400	mA		
IDD3P	500	500	880	880	mA		
IDD3N	680	680	1200	1200	mA		
IDD4R	1670	1670	2080	2080	mA		
IDD4W	1980	1980	2360	2360	mA		
IDD5	1800	1800	2200	2200	mA		
IDD6	Normal	27	27	48	48	mA	
	Low power	14	14	24	24	mA	Optional
IDD7A	3150	3150	3400	3400	mA		

## DDR SDRAM IDD spec table

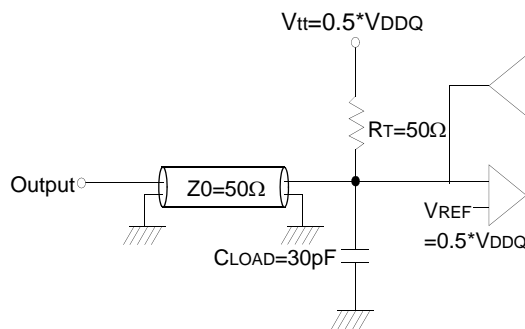
(V<sub>DD</sub>=2.7V, T = 10×C)

Symbol	M381L6423DTM(ECC)		Unit	Notes
	CC(DDR400@CL=3)	C4(DDR400@CL=3)		
IDD0	1620	1580	mA	
IDD1	1850	1850	mA	
IDD2P	75	75	mA	
IDD2F	540	540	mA	
IDD2Q	450	450	mA	
IDD3P	990	990	mA	
IDD3N	1350	1350	mA	
IDD4R	2340	2340	mA	
IDD4W	2660	2660	mA	
IDD5	2480	2480	mA	
IDD6	Normal	54	mA	
	Low power	27	mA	Optional
IDD7A	3830	3830	mA	

AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	V <sub>IH</sub> (AC)	V <sub>REF</sub> + 0.31		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	V <sub>IL</sub> (AC)		V <sub>REF</sub> - 0.31	V	
Input Differential Voltage, CK and CK inputs	V <sub>ID</sub> (AC)	0.7	V <sub>DDQ</sub> +0.6	V	1
Input Crossing Point Voltage, CK and CK inputs	V <sub>IX</sub> (AC)	0.5*V <sub>DDQ</sub> -0.2	0.5*V <sub>DDQ</sub> +0.2	V	2

- Note :**
1. V<sub>ID</sub> is the magnitude of the difference between the input level on CK and the input on  $\overline{CK}$ .
  2. The value of V<sub>IX</sub> is expected to equal 0.5\*V<sub>DDQ</sub> of the transmitting device and must track variations in the DC level of the same.
  3. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. the AC and DC input specificatims are reflation to a V<sub>ref</sub> envelope that has been bandwidth limited 20MHz.



Output Load Circuit (SSTL\_2)

Input/Output Capacitance

(VDD=2.6V, VDDQ=2.6V, TA= 25°C, f=1MHz)

Parameter	Symbol	M368L1624DTM		M368L3223DTM		M381L3223DTM		Unit
		Min	Max	Min	Max	Min	Max	
Input capacitance(A0 ~ A12, BA0 ~ BA1, $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ )	CIN1	41	45	49	57	51	60	pF
Input capacitance(CKE0)	CIN2	34	38	42	50	44	53	pF
Input capacitance( $\overline{CS0}$ )	CIN3	34	38	42	50	44	53	pF
Input capacitance( CLK0, CLK1,CLK2)	CIN4	25	30	25	30	25	30	pF
Input capacitance(DM0~DM7)	CIN5	6	7	6	7	6	7	pF
Data & DQS input/output capacitance(DQ0~DQ63)	Cout1	6	7	6	7	6	7	pF
Data input/output capacitance (CB0~CB7)	Cout2	-	-	-	-	6	7	pF

Parameter	Symbol	M368L6423DTM		M381L6423DTM		Unit
		Min	Max	Min	Max	
Input capacitance(A0 ~ A12, BA0 ~ BA1, $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ )	CIN1	65	81	69	87	pF
Input capacitance(CKE0,CKE1)	CIN2	42	50	44	53	pF
Input capacitance( $\overline{CS0}$ , $\overline{CS1}$ )	CIN3	42	50	44	53	pF
Input capacitance( CLK0, CLK1,CLK2)	CIN4	28	34	28	34	pF
Input capacitance(DM0~DM8)	CIN5	10	12	10	12	pF
Data & DQS input/output capacitance(DQ0~DQ63)	Cout1	10	12	10	12	pF
Data input/output capacitance (CB0~CB7)	Cout2	-	-	10	12	pF

AC Timing Parameters and Specifications

Parameter	Symbol	- CC(DDR400@CL=3)		- C4(DDR400@CL=3)		Unit	Note
		Min	Max	Min	Max		
Row cycle time	tRC	55		60		ns	
Refresh row cycle time	tRFC	70		70		ns	
Row active time	tRAS	40	70K	40	70K	ns	
RAS to CAS delay	tRCD	15		18		ns	
Row precharge time	tRP	15		18		ns	
Row active to Row active delay	tRRD	10		10		ns	
Write recovery time	tWR	15		15		ns	
Internal write to read command delay	tWTR	2		2		tCK	
Clock cycle time	tCK	5	10	5	10	ns	16
		6	12	6	12	ns	
Clock high level width	tCH	0.45	0.55	0.45	0.55	tCK	
Clock low level width	tCL	0.45	0.55	0.45	0.55	tCK	
DQS-out access time from CK/CK	tDQSK	-0.55	+0.55	-0.55	+0.55	ns	
Output data access time from CK/CK	tAC	-0.65	+0.65	-0.65	+0.65	ns	
Data strobe edge to output data edge	tDQSQ	-	0.4	-	0.4	ns	13
Read Preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	
Read Postamble	tRPST	0.4	0.6	0.4	0.6	tCK	
CK to valid DQS-in	tDQSS	0.72	1.28	0.72	1.28	tCK	
Write preamble setup time	tWPRES	0		0		ps	5
Write preamble	tWPRE	0.25		0.25		tCK	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK	4
DQS falling edge to CK rising-setup time	tDSS	0.2		0.2		tCK	
DQS falling edge from CK rising-hold time	tDSH	0.2		0.2		tCK	
DQS-in high level width	tDQSH	0.35		0.35		tCK	
DQS-in low level width	tDQSL	0.35		0.35		tCK	
Address and Control Input setup time	tIS	0.6		0.6		ns	h,7-10
Address and Control Input hold time	tIH	0.6		0.6		ns	h,7-10
Data-out high impedance time from CK/CK	tHZ	-	tAC max	-	tAC max	ns	3
Data-out low impedance time from CK/CK	tLZ	tAC min	tAC max	tAC min	tAC max	ns	3
Mode register set cycle time	tMRD	2		2		tCK	
DQ & DM setup time to DQS, slew rate 0.5V/ns	tDS	0.4		0.4		ns	i, j
DQ & DM hold time to DQS, slew rate 0.5V/ns	tDH	0.4		0.4		ns	i, j
DQ & DM input pulse width	tDIPW	1.75		1.75		ns	9
Control & Address input pulse width for each input	tIPW	2.2		2.2		ns	9
Refresh interval time	Up to 128Mb	15.6		15.6		us	6
	256Mb, 512Mb, 1Gb	7.8		7.8		us	
Output DQS valid window	tQH	tHP -tQHS	-	tHP -tQHS	-	ns	12
Clock half period	tHP	min tCH/tCL	-	min tCH/tCL	-	ns	11, 12

Parameter	Symbol	- CC(DDR400@CL=3)		- C4(DDR400@CL=3)		Unit	Note
		Min	Max	Min	Max		
Data hold skew factor	tQHS		0.5		0.5	ns	12
Auto Precharge write recovery + precharge time	tDAL	-	-	-	-	ns	14
Exit self refresh to non-READ command	tXSNR	75		75		ns	15
Exit self refresh to READ command	tXSRD	200	-	200	-	tCK	

### Component Notes

1.  $V_{id}$  is the magnitude of the difference between the input level on CK and the input level on  $\overline{CK}$ .
2. The value of  $V_{IX}$  is expected to equal  $0.5 \cdot V_{DDQ}$  of the transmitting device and must track variations in the dc level of the same.
3. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. these parameters are not referenced to a specific voltage level but specify when the device output in no longer driving (HZ), or begins driving (LZ).
4. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
5. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. when no writes were previously in progress on the bus, DQS will be transitioning from High- Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
6. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
7. For command/address input slew rate  $\geq 0.5$  V/ns
8. For CK &  $\overline{CK}$  slew rate  $\geq 0.5$  V/ns
9. These parameters guarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.
10. Slew Rate is measured between  $V_{OH}(ac)$  and  $V_{OL}(ac)$ .
11. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH)....For example, tCL and tCH are = 50% of the period, less the half period jitter (tJIT(HP)) of the clock source, and less the half period jitter due to crosstalk (tJIT(crosstalk)) into the clock traces.
12.  $t_{QH} = t_{HP} - t_{QHS}$ , where:  
tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS accounts for 1) The pulse duration distortion of on-chip clock circuits; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
13. tDQSQ  
Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.
14.  $t_{DAL} = (t_{WR}/t_{CK}) + (t_{RP}/t_{CK})$   
For each of the terms above, if not already an integer, round to the next highest integer. Example: For DDR400(CC) at CL=3 and tCK=5ns  $t_{DAL} = (15 \text{ ns} / 5 \text{ ns}) + (15 \text{ ns} / 5 \text{ ns}) = \{(3) + (3)\} \text{CLK}$   
tDAL = 6 clocks
15. In all circumstances, tXSNR can be satisfied using  $t_{XSNR} = t_{RFCmin} + 1 \cdot t_{CK}$
16. The only time that the clock frequency is allowed to change is during self-refresh mode.

## System Characteristics for DDR SDRAM

The following specification parameters are required in systems using DDR400 devices to ensure proper system performance. These characteristics are for system simulation purposes and are guaranteed by design.

**Table 1 : Input Slew Rate for DQ, DQS, and DM**

AC CHARACTERISTICS		DDR400			
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DQ/DM/DQS input slew rate measured between VIH(DC), VIL(DC) and VIL(DC), VIH(DC)	DCSLEW	0.5	4.0	V/ns	a, k

**Table 2 : Input Setup & Hold Time Derating for Slew Rate**

Input Slew Rate	tIS	tIH	UNITS	NOTES
0.5 V/ns	0	0	ps	h
0.4 V/ns	+50	0	ps	h
0.3 V/ns	+100	0	ps	h

**Table 3 : Input/Output Setup & Hold Time Derating for Slew Rate**

Input Slew Rate	tDS	tDH	UNITS	NOTES
0.5 V/ns	0	0	ps	j
0.4 V/ns	+75	+75	ps	j
0.3 V/ns	+150	+150	ps	j

**Table 4 : Input/Output Setup & Hold Derating for Rise/Fall Delta Slew Rate**

Delta Slew Rate	tDS	tDH	UNITS	NOTES
+/- 0.0 V/ns	0	0	ps	i
+/- 0.25 V/ns	+50	+50	ps	i
+/- 0.5 V/ns	+100	+100	ps	i

**Table 5 : Output Slew Rate Characteristic (X8 Devices only)**

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	NOTES
Pullup Slew Rate	1.2 ~ 2.5	1.0	4.5	a,c,d,f,g
Pulldown slew	1.2 ~ 2.5	1.0	4.5	b,c,d,f,g

**Table 6 : Output Slew Rate Characteristic (X16 Devices only)**

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	NOTES
Pullup Slew Rate	1.2 ~ 2.5	0.7	5.0	a,c,d,f,g
Pulldown slew	1.2 ~ 2.5	0.7	5.0	b,c,d,f,g

**Table 7 : Output Slew Rate Matching Ratio Characteristics**

AC CHARACTERISTICS		DDR400		
PARAMETER		MIN	MAX	NOTES
Output Slew Rate Matching Ration (Pullup to Pulldown)		-	-	e,k



**System Notes :**

a. Pullup slew rate is characterized under the test conditions as shown in Figure 1.

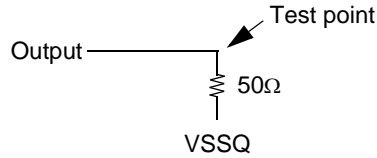


Figure 1 : Pullup slew rate test load

b. Pulldown slew rate is measured under the test conditions shown in Figure 2.

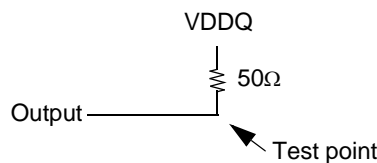


Figure 2 : Pulldown slew rate test load

c. Pullup slew rate is measured between (VDDQ/2 - 320 mV +/- 250 mV)

Pulldown slew rate is measured between (VDDQ/2 + 320 mV +/- 250 mV)

Pullup and Pulldown slew rate conditions are to be met for any pattern of data, including all outputs switching and only one output switching.

Example : For typical slew rate, DQ0 is switching

For minimum slew rate, all DQ bits are switching from either high to low, or low to high.

For Maximum slew rate, only one DQ is switching from either high to low, or low to high.

The remaining DQ bits remain the same as for previous state.

d. Evaluation conditions

Typical : 25 °C (T Ambient), VDDQ = 2.6V, typical process

Minimum : 70 °C (T Ambient), VDDQ = 2.5V, slow - slow process

Maximum : 0 °C (T Ambient), VDDQ = 2.7V, fast - fast process

e. The ratio of pullup slew rate to pulldown slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.

f. Verified under typical conditions for qualification purposes.

g. TSOP package devices only.

h. A derating factor will be used to increase tIS and tIH in the case where the input slew rate is below 0.5

V/ns as shown in Table 2. The Input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions.

i. A derating factor will be used to increase tDS and tDH in the case where DQ, DM, and DQS slew rates differ, as shown in Tables 3 & 4.

Input slew rate is based on the larger of AC-AC delta rise, fall rate and DC-DC delta rise, Input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions.

The delta rise/fall rate is calculated as:

$$\{1/(\text{Slew Rate1})\} - \{1/(\text{Slew Rate2})\}$$

For example : If Slew Rate 1 is 0.5 V/ns and Slew Rate 2 is 0.4 V/ns, then the delta rise, fall rate is - 0.5ns/V . Using the table given, this would result in the need for an increase in tDS and tDH of 100 ps.

- j. Table 3 is used to increase  $t_{DS}$  and  $t_{DH}$  in the case where the I/O slew rate is below 0.5 V/ns. The I/O slew rate is based on the lesser of the AC ~ AC slew rate and the DC- DC slew rate. The input slew rate is based on the lesser of the slew rates determined by either  $V_{IH}(ac)$  to  $V_{IL}(ac)$  or  $V_{IH}(DC)$  to  $V_{IL}(DC)$ , and similarly for rising transitions.
- k. DQS, DM, and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.

Command Truth Table

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

COMMAND		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0,1	A10/AP	A0 ~ A9 A11, A12	Note	
Register	Extended MRS	H	X	L	L	L	L	OP CODE			1, 2	
Register	Mode Register Set	H	X	L	L	L	L	OP CODE			1, 2	
Refresh	Auto Refresh		H	H	L	L	L	H	X		3	
	Self Refresh	Entry		L							3	
		Exit	L	H	L	H	H	H	X		3	
	H		X	X	X	3						
Bank Active & Row Addr.		H	X	L	L	H	H	V	Row Address (A0~A9, A11, A12)			
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	L	Column Address	4	
	Auto Precharge Enable								H		4	
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	L	Column Address	4	
	Auto Precharge Enable								H		4, 6	
Burst Stop		H	X	L	H	H	L	X			7	
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	
	All Banks								X	H		5
Active Power Down	Entry	H	L	H	X	X	X	X				
				L	V	V	V					
				L	H	X	X			X	X	
Precharge Power Down Mode	Entry	H	L	H	X	X	X	X				
				L	H	H	H					
	Exit	L	H	H	X	X	X					
				L	V	V	V					
DM		H	X					X		8		
No operation (NOP) : Not defined		H	X	H	X	X	X	X		9		
				L	H	H	H			9		

**Note** : 1. OP Code : Operand Code. A0 ~ A12 & BA0 ~ BA1 : Program keys. (@EMRS/MRS)

- EMRS/ MRS can be issued only at all banks precharge state.  
A new command can be issued 2 clock cycles after EMRS or MRS.
- Auto refresh functions are same as the CBR refresh of DRAM.  
The automatical precharge without row precharge command is meant by "Auto".  
Auto/self refresh can be issued only at all banks precharge state.
- BA0 ~ BA1 : Bank select addresses.  
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.  
If BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.  
If BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected.  
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
- If A10/AP is "High" at row precharge, BA0 and BA1 are ignored and all banks are selected.
- During burst write with auto precharge, new read/write command can not be issued.  
Another bank read/write command can be issued after the end of burst.  
New row active of the associated bank can be issued at tRP after the end of burst.
- Burst stop command is valid at every burst length.
- DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).
- This combination is not defined for any function, which means "No Operation(NOP)" in DDR SDRAM.

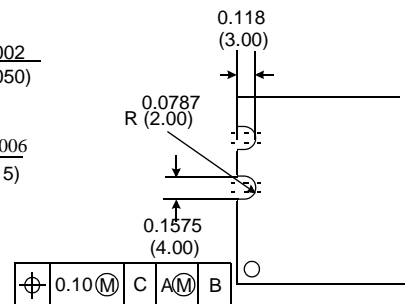
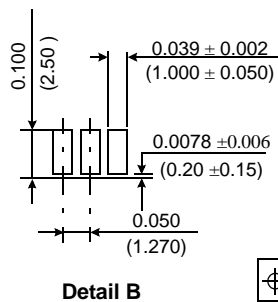
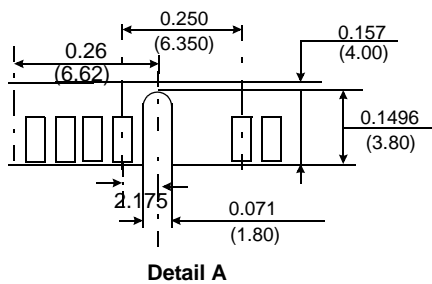
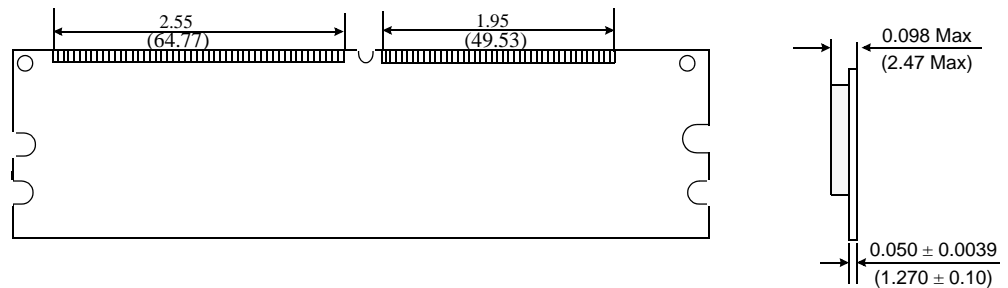
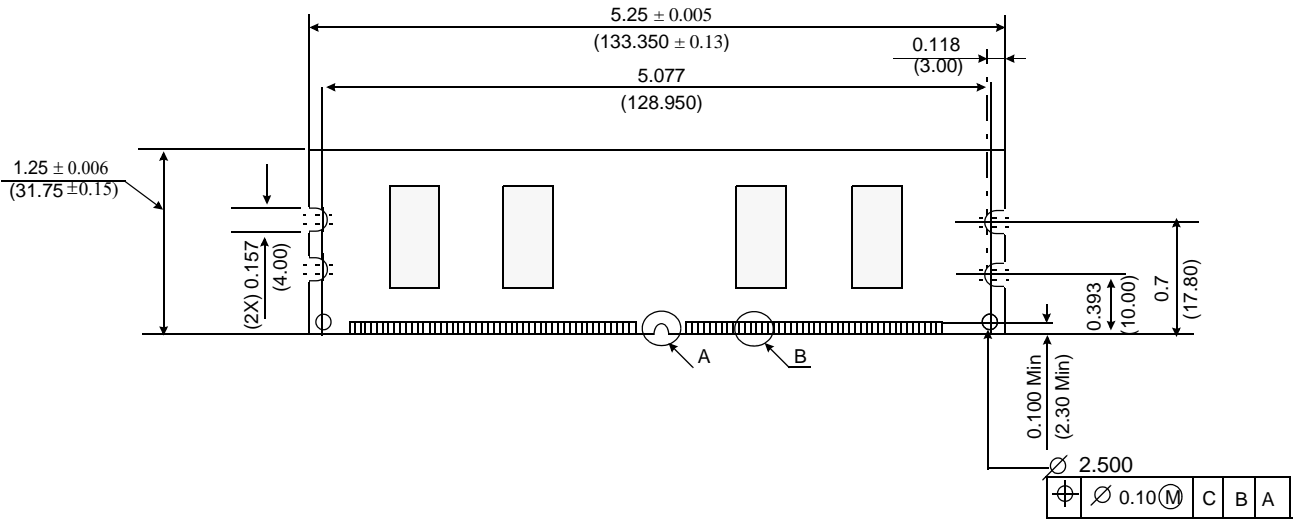
# 128MB, 256MB, 512MB Unbuffered DIMM

# DDR SDRAM

## Physical Dimensions : 16M x 64 (M368L1624DTM)

### PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : ± 0.005(.13) unless otherwise specified.  
 The used device is 16Mx16 DDR SDRAM, TSOP.  
 DDR SDRAM Part NO : K4H561638D

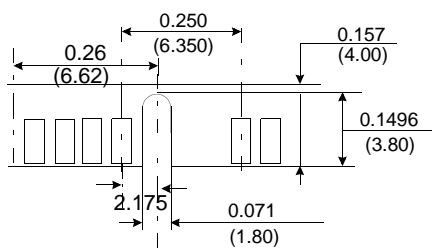
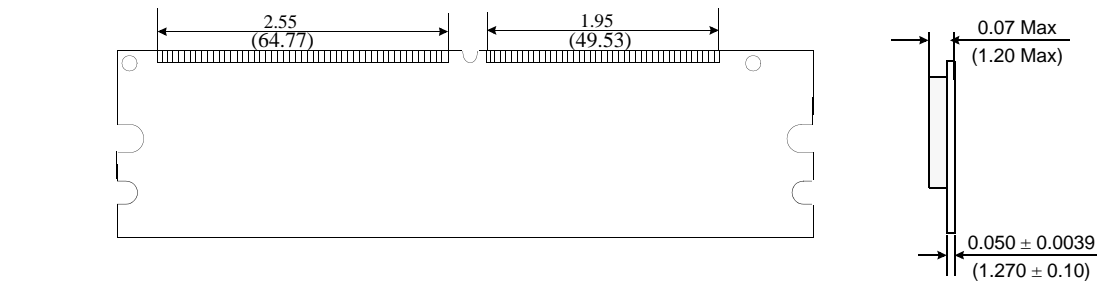
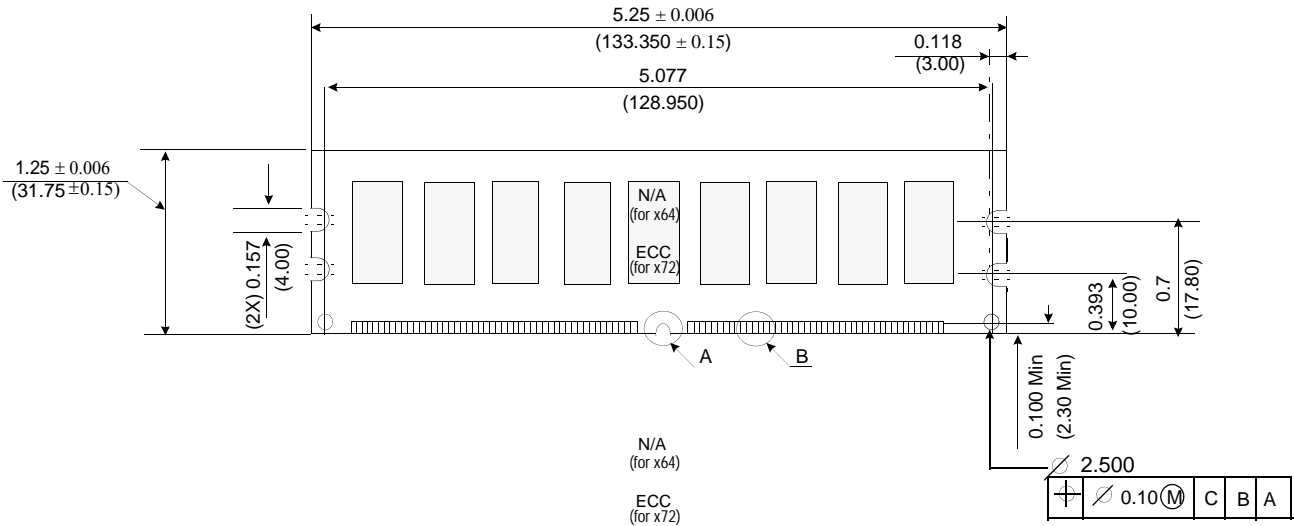
# 128MB, 256MB, 512MB Unbuffered DIMM

# DDR SDRAM

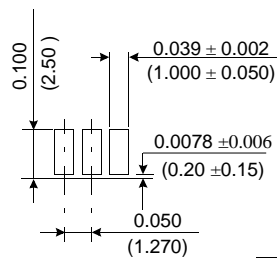
Physical Dimensions : 32M x 64 (M368L3223DTM), 32M x 72 (M381L3223DTM)

## PACKAGE DIMENSIONS

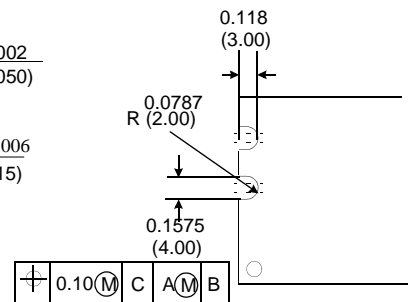
Units : Inches (Millimeters)



Detail A



Detail B



Tolerances :  $\pm 0.005$ (.13) unless otherwise specified.  
 The used device is 32Mx8 DDR SDRAM, TSOP.  
 DDR SDRAM Part NO : K4H560838D.

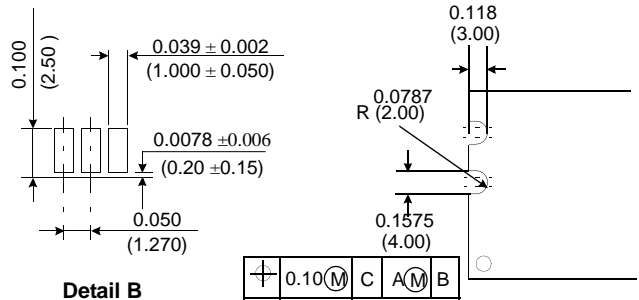
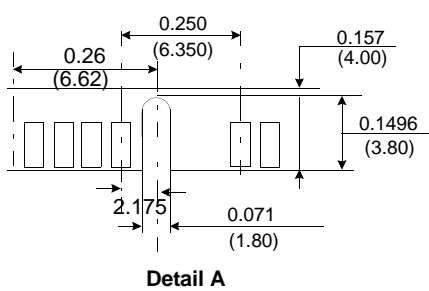
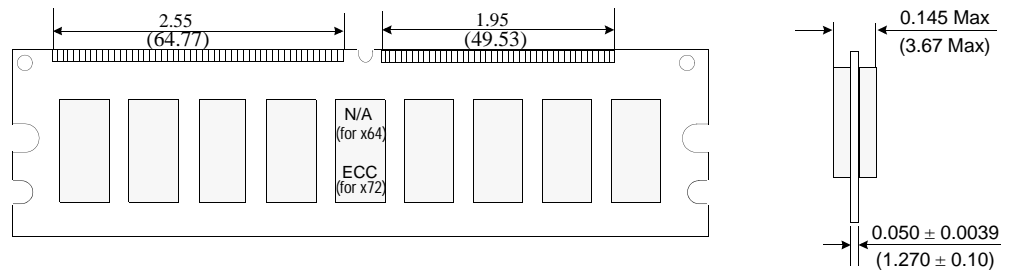
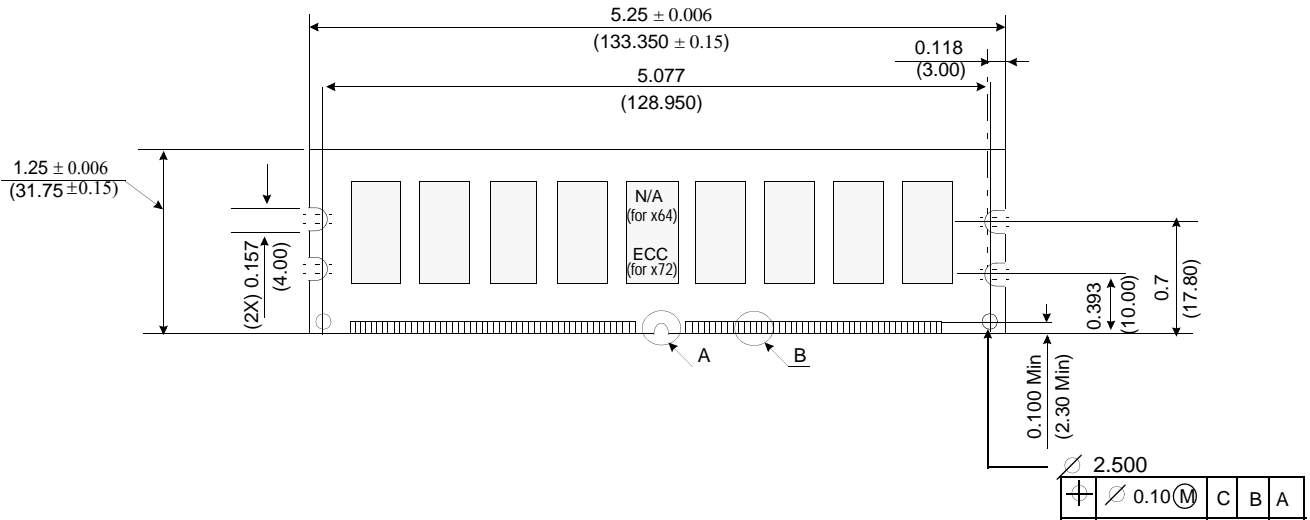
# 128MB, 256MB, 512MB Unbuffered DIMM

# DDR SDRAM

Physical Dimensions : 64M x 64 (M368L6423DTM), 64M x 72 (M381L6423DTM)

## PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : ± 0.005(.13) unless otherwise specified.  
 The used device is 32Mx8 DDR SDRAM, TSOP.  
 DDR SDRAM Part NO : K4H560838D